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### Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

|                                 |                                                                                                                                     |
|---------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                  | Obsolete                                                                                                                            |
| Core Processor                  | Z8S180                                                                                                                              |
| Number of Cores/Bus Width       | 1 Core, 8-Bit                                                                                                                       |
| Speed                           | 10MHz                                                                                                                               |
| Co-Processors/DSP               | -                                                                                                                                   |
| RAM Controllers                 | DRAM                                                                                                                                |
| Graphics Acceleration           | No                                                                                                                                  |
| Display & Interface Controllers | -                                                                                                                                   |
| Ethernet                        | -                                                                                                                                   |
| SATA                            | -                                                                                                                                   |
| USB                             | -                                                                                                                                   |
| Voltage - I/O                   | 5.0V                                                                                                                                |
| Operating Temperature           | -40°C ~ 100°C (TA)                                                                                                                  |
| Security Features               | -                                                                                                                                   |
| Package / Case                  | 80-BQFP                                                                                                                             |
| Supplier Device Package         | 80-QFP                                                                                                                              |
| Purchase URL                    | <a href="https://www.e-xfl.com/product-detail/zilog/z8s18010fec00tr">https://www.e-xfl.com/product-detail/zilog/z8s18010fec00tr</a> |

GENERAL DESCRIPTION (Continued)

Power connections follow the conventional descriptions below:

| Connection | Circuit         | Device          |
|------------|-----------------|-----------------|
| Power      | V <sub>CC</sub> | V <sub>DD</sub> |
| Ground     | GND             | V <sub>SS</sub> |

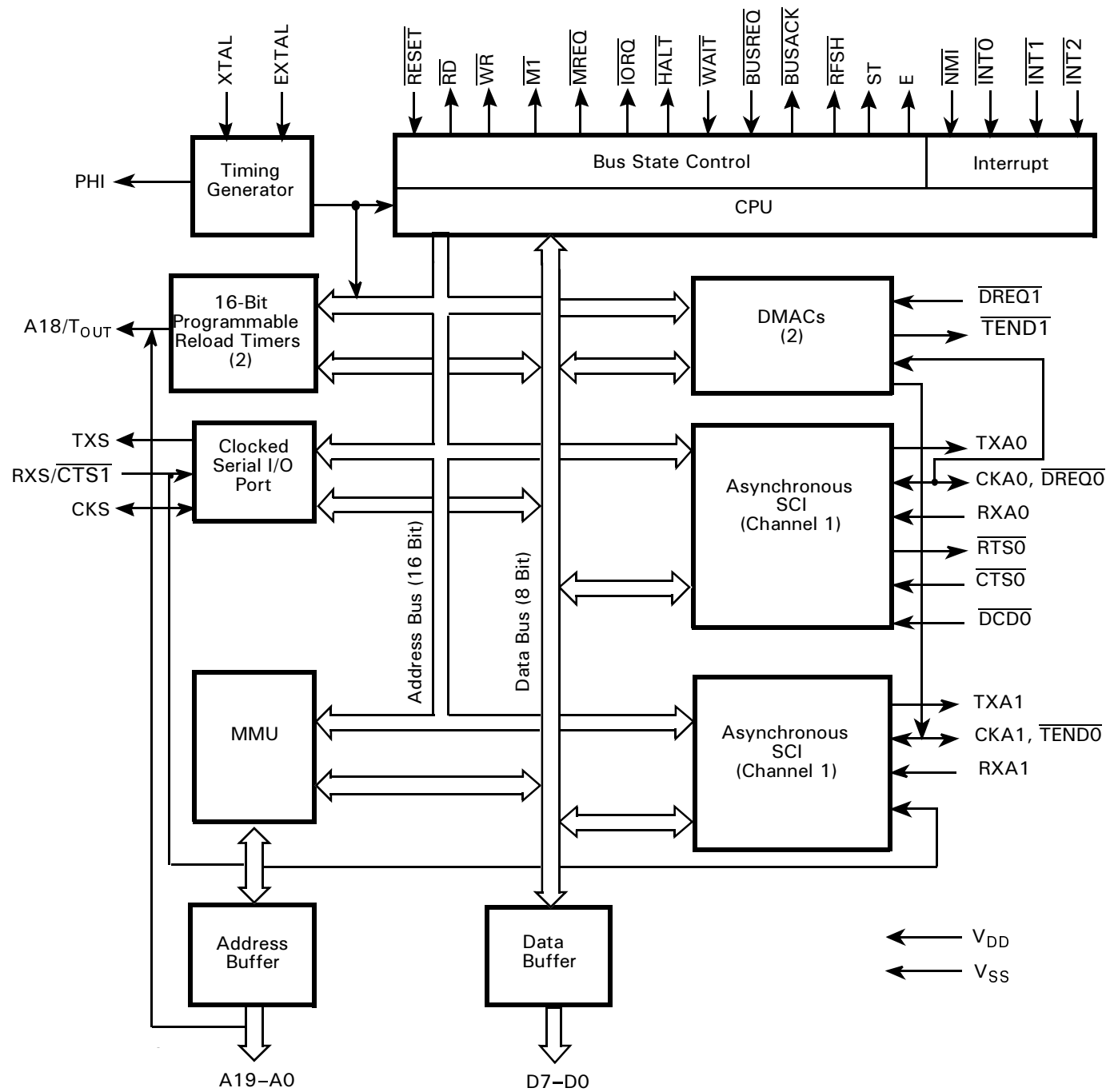


Figure 1. Z8S180/Z8L180 Functional Block Diagram

## PIN IDENTIFICATION (Continued)

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes

| Pin Number and Package Type |      |     |                          |                    | Pin Status |          |          |
|-----------------------------|------|-----|--------------------------|--------------------|------------|----------|----------|
| QFP                         | PLCC | DIP | Default Function         | Secondary Function | RESET      | BUSACK   | SLEEP    |
| 1                           | 9    | 8   | $\overline{\text{NMI}}$  |                    | IN         | IN       | IN       |
| 2                           |      |     | NC                       |                    |            |          |          |
| 3                           |      |     | NC                       |                    |            |          |          |
| 4                           | 10   | 9   | $\overline{\text{INT0}}$ |                    | IN         | IN       | IN       |
| 5                           | 11   | 10  | $\overline{\text{INT1}}$ |                    | IN         | IN       | IN       |
| 6                           | 12   | 11  | $\overline{\text{INT2}}$ |                    | IN         | IN       | IN       |
| 7                           | 13   | 12  | ST                       |                    | High       | High     | High     |
| 8                           | 14   | 13  | A0                       |                    | 3T         | 3T       | High     |
| 9                           | 15   | 14  | A1                       |                    | 3T         | 3T       | High     |
| 10                          | 16   | 15  | A2                       |                    | 3T         | 3T       | High     |
| 11                          | 17   | 16  | A3                       |                    | 3T         | 3T       | High     |
| 12                          | 18   |     | $V_{SS}$                 |                    | $V_{SS}$   | $V_{SS}$ | $V_{SS}$ |
| 13                          | 19   | 17  | A4                       |                    | 3T         | 3T       | High     |
| 14                          |      |     | NC                       |                    |            |          |          |
| 15                          | 20   | 18  | A5                       |                    | 3T         | 3T       | High     |
| 16                          | 21   | 19  | A6                       |                    | 3T         | 3T       | High     |
| 17                          | 22   | 20  | A7                       |                    | 3T         | 3T       | High     |
| 18                          | 23   | 21  | A8                       |                    | 3T         | 3T       | High     |
| 19                          | 24   | 22  | A9                       |                    | 3T         | 3T       | High     |
| 20                          | 25   | 23  | A10                      |                    | 3T         | 3T       | High     |
| 21                          | 26   | 24  | A11                      |                    | 3T         | 3T       | High     |
| 22                          |      |     | NC                       |                    |            |          |          |
| 23                          |      |     | NC                       |                    |            |          |          |
| 24                          | 27   | 25  | A12                      |                    | 3T         | 3T       | High     |
| 25                          | 28   | 26  | A13                      |                    | 3T         | 3T       | High     |
| 26                          | 29   | 27  | A14                      |                    | 3T         | 3T       | High     |
| 27                          | 30   | 28  | A15                      |                    | 3T         | 3T       | High     |
| 28                          | 31   | 29  | A16                      |                    | 3T         | 3T       | High     |
| 29                          | 32   | 30  | A17                      |                    | 3T         | 3T       | High     |
| 30                          |      |     | NC                       |                    |            |          |          |
| 31                          | 33   | 31  | A18                      |                    | 3T         | 3T       | High     |
|                             |      |     | $T_{OUT}$                |                    | N/A        | OUT      | OUT      |
| 32                          | 34   | 32  | $V_{DD}$                 |                    | $V_{DD}$   | $V_{DD}$ | $V_{DD}$ |
| 33                          | 35   |     | A19                      |                    | 3T         | 3T       | High     |
| 34                          | 36   | 33  | $V_{SS}$                 |                    | $V_{SS}$   | $V_{SS}$ | $V_{SS}$ |
| 35                          | 37   | 34  | D0                       |                    | 3T         | 3T       | 3T       |
| 36                          | 38   | 35  | D1                       |                    | 3T         | 3T       | 3T       |
| 37                          | 39   | 36  | D2                       |                    | 3T         | 3T       | 3T       |
| 38                          | 40   | 37  | D3                       |                    | 3T         | 3T       | 3T       |

Table 4. Multiplexed Pin Descriptions

|                                 |                                                                                                                                                                                                                                               |
|---------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A18/TOUT                        | During RESET, this pin is initialized as A18. If either the TOC1 or the TOC0 bit of the Timer Control register (TCR) is set to 1, the T <sub>OUT</sub> function is selected. If TOC1 and TOC0 are cleared to 0, the A18 function is selected. |
| CKA0/ $\overline{\text{DREQ0}}$ | During RESET, this pin is initialized as CKA0. If either DM1 or SM1 in the DMA Mode register (DMODE) is set to 1, the $\overline{\text{DREQ0}}$ function is selected.                                                                         |
| CKA1/ $\overline{\text{TEND0}}$ | During RESET, this pin is initialized as CKA1. If the CKA1D bit in ASCI control register ch1 (CNTLA1) is set to 1, the $\overline{\text{TEND0}}$ function is selected. If the CKA1D bit is set to 0, the CKA1 function is selected.           |
| RXS/ $\overline{\text{CTS1}}$   | During RESET, this pin is initialized as RXS. If the CTS1E bit in the ASCI status register ch1 (STAT1) is set to 1, the $\overline{\text{CTS1}}$ function is selected. If the CTS1E bit is set to 0, the RXS function is selected.            |

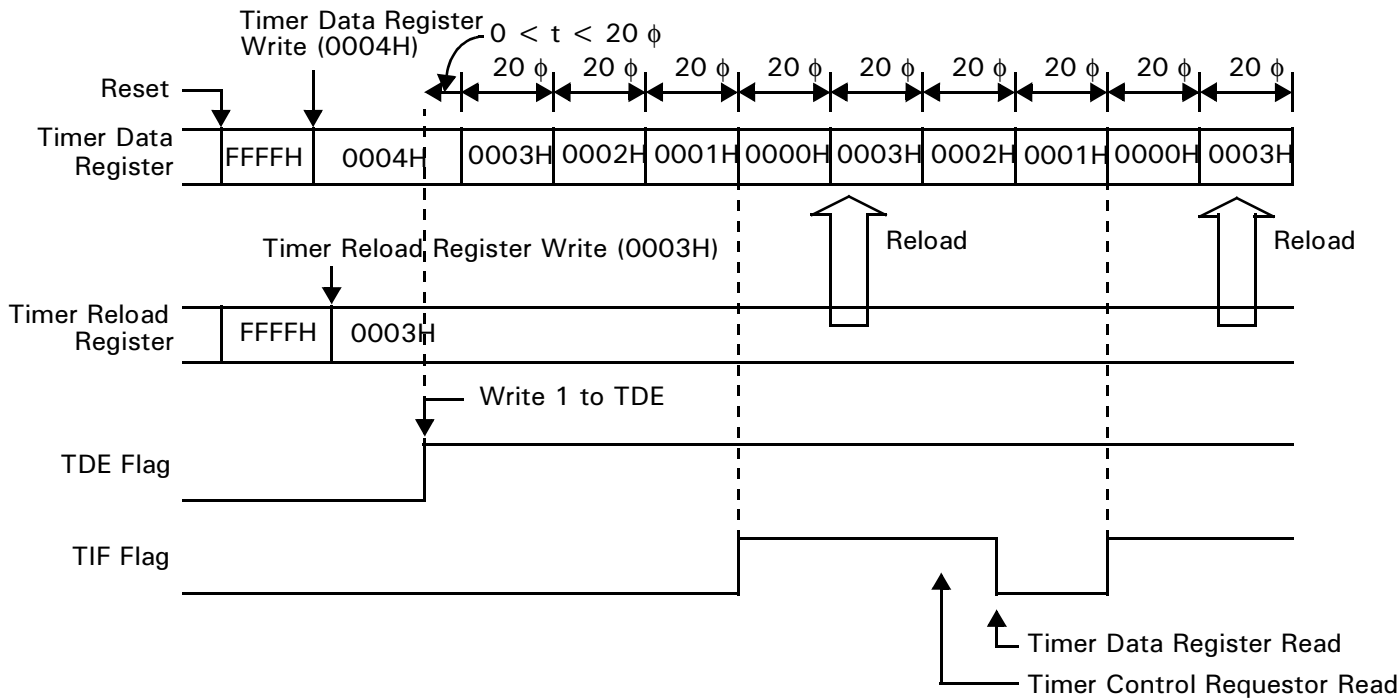


Figure 5. Timer Initialization, Count Down, and Reload Timing

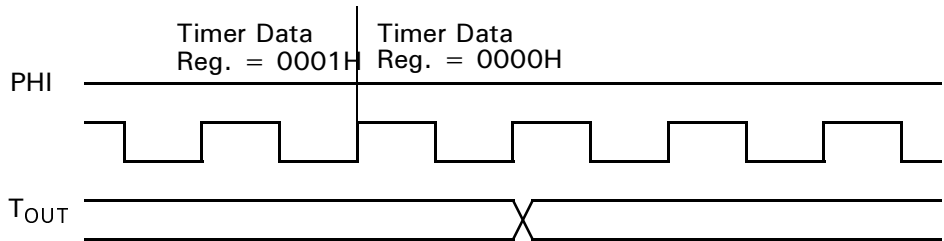


Figure 6. Timer Output Timing

**Clocked Serial I/O (CSI/O).** The CSI/O channel provides a half-duplex serial transmitter and receiver. This channel can be used for simple high-speed data connection to another microprocessor or microcomputer. TRDR is used for both CSI/O transmission and reception. Thus, the system design must ensure that the constraints of half-duplex operation are met (Transmit and Receive operation cannot occur simultaneously). For example, if a CSI/O transmission is attempted while the CSI/O is receiving data, a CSI/O does not work.

**Note:** TRDR is not buffered. Performing a CSI/O transmit while the previous transmission is still in progress causes the data to be immediately updated and corrupts the transmit operation. Similarly, reading TRDR while a transmit or receive is in progress should be avoided.



STANDARD TEST CONDITIONS

The following standard test conditions apply to [DC Characteristics](#), unless otherwise noted. All voltages are referenced to  $V_{SS}$  (0V). Positive current flows into the referenced pin.

All AC parameters assume a load capacitance of 100 pF. Add a 10-ns delay for each 50-pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to  $V_{OL\ MAX}$  or  $V_{OL\ MIN}$  as indicated in Figures 20 through 30 (except for CLOCK, which is referenced to the 10% and 90% points). [Ordering Information](#) lists temperature ranges and product numbers. Find package drawings in [Package Information](#).

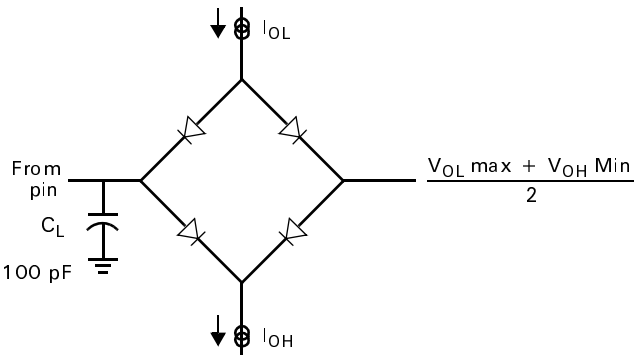
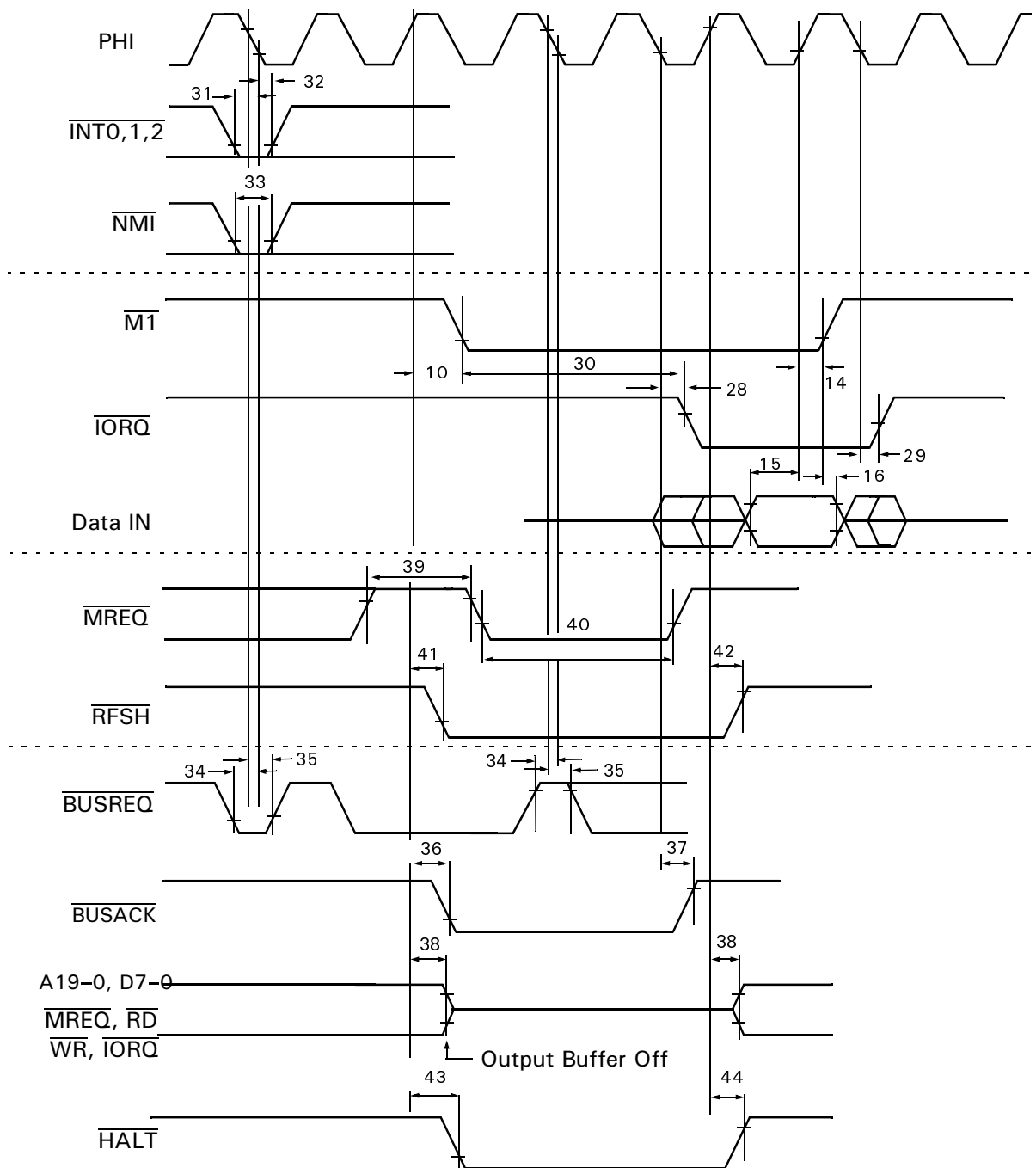


Figure 19. AC Parameter Test Circuit

ABSOLUTE MAXIMUM RATINGS

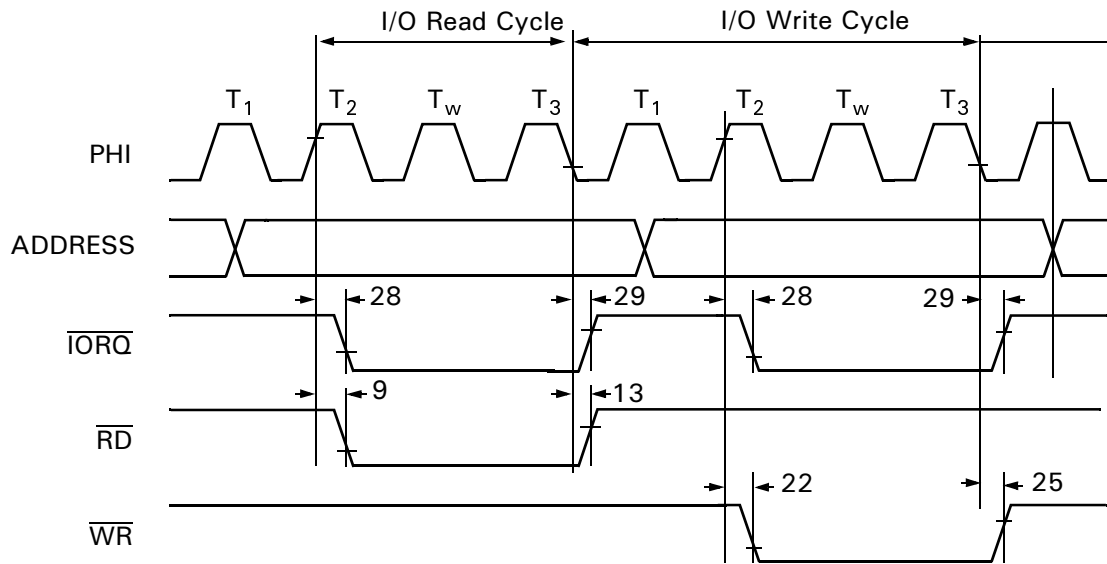
| Item                  | Symbol    | Value                 | Unit |
|-----------------------|-----------|-----------------------|------|
| Supply Voltage        | $V_{DD}$  | -0.3 ~ +7.0           | V    |
| Input Voltage         | $V_{IN}$  | -0.3 ~ $V_{CC} + 0.3$ | V    |
| Operating Temperature | $T_{OPR}$ | 0 ~ 70                | °C   |
| Extended Temperature  | $T_{EXT}$ | -40 ~ 85              | °C   |
| Storage Temperature   | $T_{STG}$ | -55 ~ +150            | °C   |

**Note:** Permanent damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability.



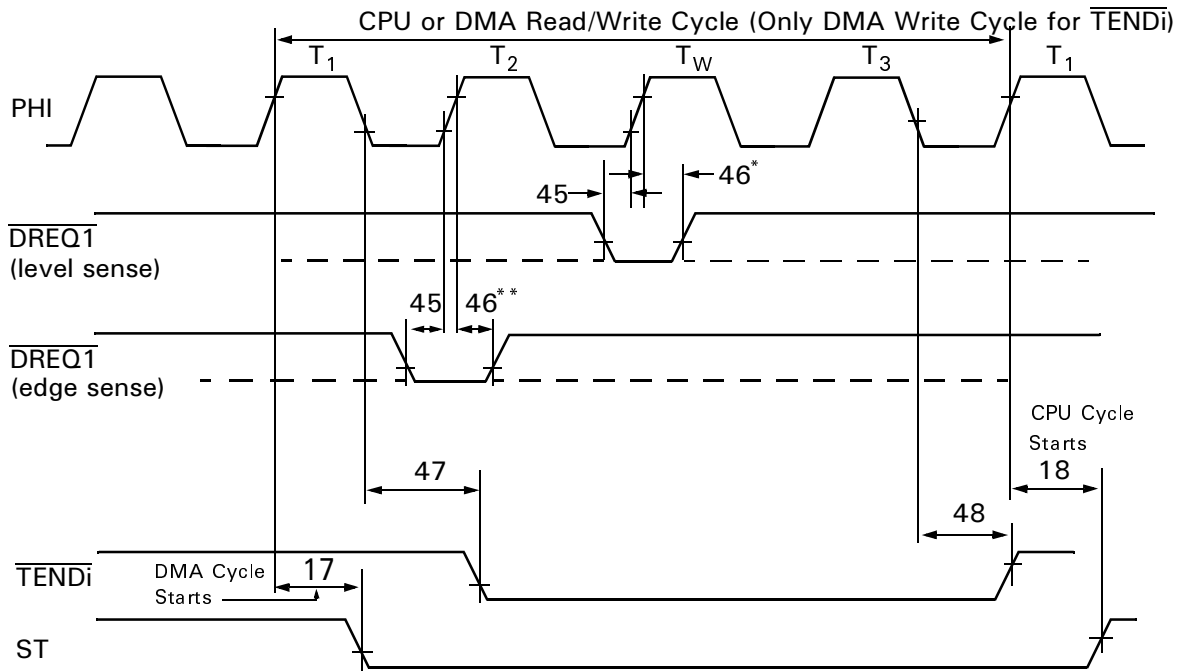
**Figure 21. CPU Timing**  
 ( $\overline{\text{INT0}}$  Acknowledge Cycle, Refresh Cycle, BUS RELEASE Mode,  
 HALT Mode, SLEEP Mode, SYSTEM STOP Mode)

## TIMING DIAGRAMS (Continued)



CPU Timing ( $\overline{I/O} = 0$ )

Figure 22. CPU Timing ( $\overline{I/O} = 0$ )  
(I/O Read Cycle, I/O Write Cycle)



### Notes:

\* $T_{DRQS}$  and  $T_{DRQH}$  are specified for the rising edge of the clock followed by  $T_3$ .

\*\* $T_{DRQS}$  and  $T_{DRQH}$  are specified for the rising edge of the clock.

Figure 23. DMA Control Signals

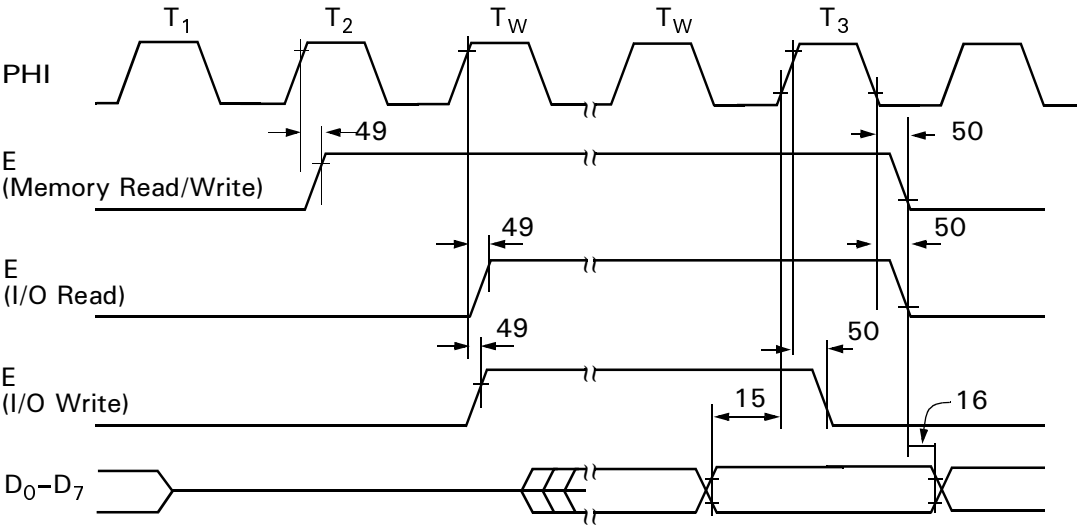


Figure 24. E Clock Timing  
(Memory Read/Write Cycle, I/O Read/Write Cycle)

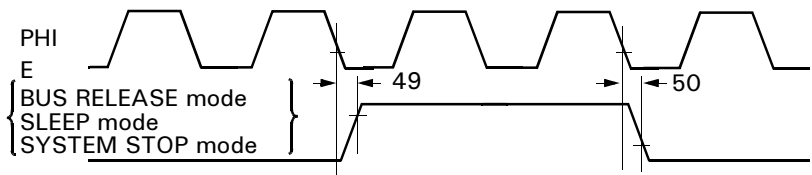


Figure 25. E Clock Timing  
(BUS RELEASE Mode, SLEEP Mode, SYSTEM STOP Mode)

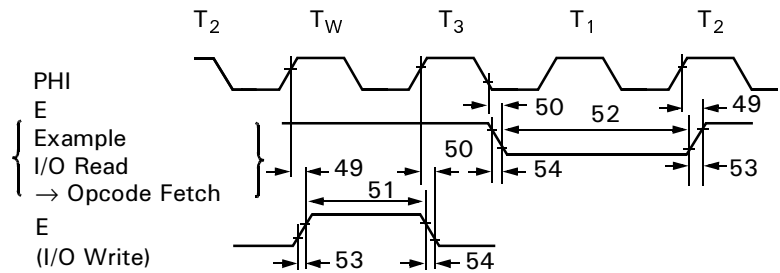


Figure 26. E Clock Timing  
(Minimum Timing Example of  $\text{P}_\text{WEL}$  and  $\text{P}_\text{WEH}$ )

CPU CONTROL REGISTER

**CPU Control Register (CCR).** This register controls the basic clock rate, certain aspects of Power-Down modes, and output drive/low-noise options (Figure 31).

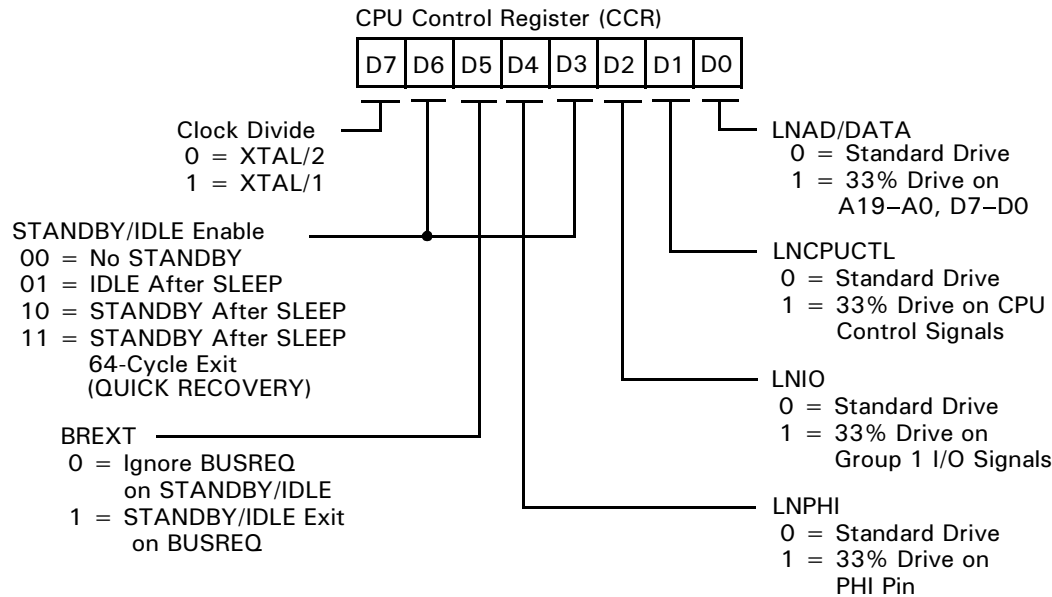


Figure 31. CPU Control Register (CCR) Address 1FH

**Bit 7.** Clock Divide Select. If this bit is 0, as it is after a RESET, the Z8S180/Z8L180 divides the frequency on the XTAL pin(s) by two to obtain its Master clock PHI. If this bit is programmed as 1, the part uses the XTAL frequency as PHI without division.

If an external oscillator is used in divide-by-one mode, the minimum pulse width requirement provided in the AC Characteristics must be satisfied.

**Bits 6 and 3.** STANDBY/IDLE Control. When these bits are both 0, a SLP instruction makes the Z8S180/Z8L180 enter SLEEP or SYSTEM STOP mode, depending on the IOSTOP bit (ICR5).

When D6 is 0 and D3 is 1, setting the IOSTOP bit (ICR5) and executing a SLP instruction puts the Z8S180/Z8L180 into IDLE mode in which the on-chip oscillator runs, but its output is blocked from the rest of the part, including PHI out.

When D6 is 1 and D3 is 0, setting IOSTOP (ICR5) and executing a SLP instruction puts the part into STANDBY mode, in which the on-chip oscillator is stopped and the part allows 2<sup>17</sup> (128K) clock cycles for the oscillator to stabilize when it restarts.

When D6 and D3 are both 1, setting IOSTOP (ICR5) and executing a SLP instruction puts the part into QUICK RECOVERY STANDBY mode, in which the on-chip oscillator is stopped, and the part allows only 64 clock cycles for the oscillator to stabilize when it restarts.

The latter section, HALT and LOW POWER modes, describes the subject more fully.

**Bit 5 BREXT.** This bit controls the ability of the Z8S180/Z8L180 to honor a bus request during STANDBY mode. If this bit is set to 1 and the part is in STANDBY mode, a BUSREQ is honored after the clock stabilization timer is timed out.

**Bit 4 LNPHI.** This bit controls the drive capability on the PHI Clock output. If this bit is set to 1, the PHI Clock output is reduced to 33 percent of its drive capability.

Data can be written into and read from the ASCII Transmit Data Register. If data is read from the ASCII Transmit Data Register, the ASCII data transmit operation is not affected by this READ operation.

**ASCII Receive Shift Register 0,1 (RSR0,1).** This register receives data shifted in on the RXA pin. When full, data is automatically transferred to the ASCII Receive Data Register (RDR) if it is empty. If RSR is not empty when the next incoming data byte is shifted in, an overrun error occurs. This register is not program accessible.

**ASCII Receive Data FIFO 0,1 (RDR0, 1:I/O Address = 08H, 09H).** The ASCII Receive Data Register is a read-only register. When a complete incoming data byte is assembled in RSR, it is automatically transferred to the 4 character Receive Data First-In First-Out (FIFO) memory. The oldest character in the FIFO (if any) can be read from the Receive Data Register (RDR). The next incoming data byte can be shifted into RSR while the FIFO is full. Thus, the ASCII receiver is well buffered.

ASCII STATUS FIFO

This four-entry FIFO contains Parity Error, Framing Error, Rx Overrun, and Break status bits associated with each char-

acter in the receive data FIFO. The status of the oldest character (if any) can be read from the ASCII status registers.

ASCII CHANNEL CONTROL REGISTER A

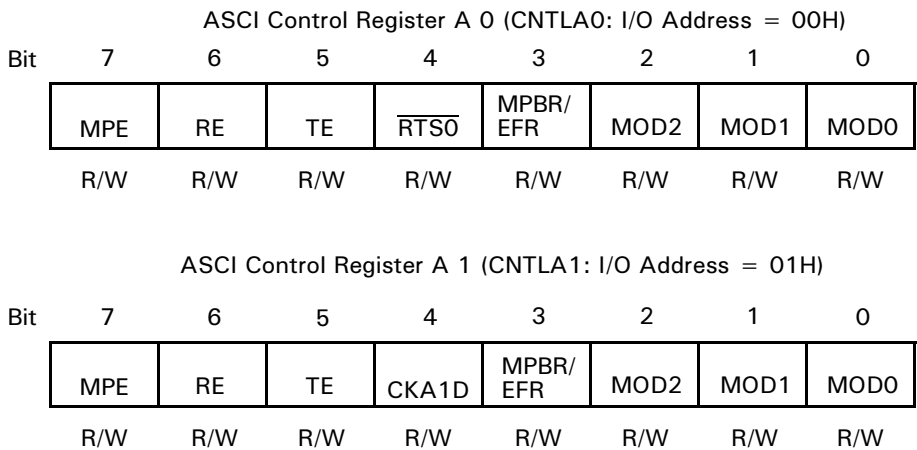


Figure 33. ASCII Channel Control Register A

**MPE: Multi-Processor Mode Enable (Bit 7).** The ASCII features a multiprocessor communication mode that utilizes an extra data bit for selective communication when a number of processors share a common serial bus. Multiprocessor data format is selected when the MP bit in CNTLB is set to 1. If multiprocessor mode is not selected (MP bit in CNTLB = 0), MPE has no effect. If multiprocessor mode is selected, MPE enables or disables the *wake-up* feature as follows. If MBE is set to 1, only received bytes in which the multiprocessor bit (MPB) = 1 can affect the RDRF and error flags. Effectively, other bytes (with MPB = 0) are *ignored* by the ASCII. If MPE is reset to 0, all bytes, regardless of

the state of the MPB data bit, affect the REDR and error flags. MPE is cleared to 0 during RESET.

**RE: Receiver Enable (Bit 6).** When RE is set to 1, the ASCII transmitter is enabled. When RE is reset to 0, the transmitter is disabled and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the previous contents of TDRE are held. RE is cleared to 0 in IOSTOP mode during RESET.

**TE: Transmitter Enable (Bit 5).** When TE is set to 1, the ASCII receiver is enabled. When TE is reset to 0, the transmitter is disabled and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the pre-

ASCI STATUS REGISTER 0,1

Each ASCI channel status register (STAT0,1) allows interrogation of ASCI communication, error and modem control signal status, and the enabling or disabling of ASCI interrupts.

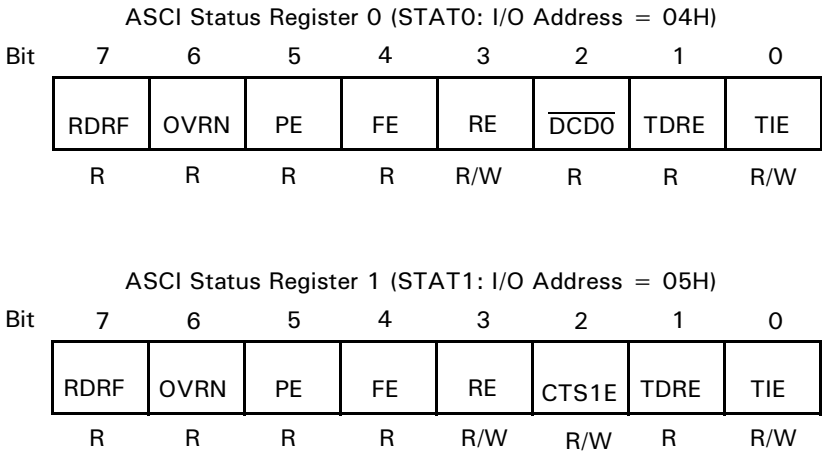


Figure 35. ASCI Status Registers

**RDRF: Receive Data Register Full (Bit 7).** RDRF is set to 1 when an incoming data byte is loaded into an empty Rx FIFO. If a framing or parity error occurs, RDRF is still set and the receive data (which generated the error) is still loaded into the FIFO. RDRF is cleared to 0 by reading RDR and most recently received character in the FIFO from IOSTOP mode, during RESET and for ASCIO if the  $\overline{\text{DCD0}}$  input is auto-enabled and is negated (High).

**OVRN: Overrun Error (Bit 6).** An overrun condition occurs if the receiver finishes assembling a character but the Rx FIFO is full so there is no room for the character. However, this status bit is not set until the most recent character received before the overrun becomes the oldest byte in the FIFO. This bit is cleared when software writes a 1 to the EFR bit in the CNTLA register. The bit may also be cleared by RESET in IOSTOP mode or ASCIO if the  $\overline{\text{DCD0}}$  pin is auto enabled and is negated (High).

**Note:** When an overrun occurs, the receiver does not place the character in the shift register into the FIFO, nor any subsequent characters, until the most recent good character enters the top of the FIFO so that OVRN is set. Software then writes a 1 to EFR to clear it.

**PE: Parity Error (Bit 5).** A parity error is detected when parity checking is enabled. When the MOD1 bit in the

CNTLA register is 1, a character is assembled in which the parity does not match the PEO bit in the CNTLB register. However, this status bit is not set until or unless the error character becomes the oldest one in the Rx FIFO. PE is cleared when software writes a 1 to the EFR bit in the CNTLA register. PE is also cleared by RESET in IOSTOP mode, or on ASCIO, if the  $\overline{\text{DCD0}}$  pin is auto-enabled and is negated (High).

**FE: Framing Error (Bit 4).** A framing error is detected when the stop bit of a character is sampled as 0/SPACE. However, this status bit is not set until/unless the error character becomes the oldest one in the Rx FIFO. FE is cleared when software writes a 1 to the EFR bit in the CNTLA register. FE is also cleared by RESET in IOSTOP mode, or on ASCIO, if the  $\overline{\text{DCD0}}$  pin is auto-enabled and is negated (High).

**REI: Receive Interrupt Enable (Bit 3).** RIE should be set to 1 to enable ASCI receive interrupt requests. When RIE is 1, the Receiver requests an interrupt when a character is received and RDRF is set, but only if neither DMA channel requires its request-routing field to be set to receive data from this ASCI. That is, if SM1–0 are 11 and SAR17–16 are 10, or DIM1 is 1 and IAR17–16 are 10, then ASCI1 does not request an interrupt for RDRF. If RIE is 1, either ASCI requests an interrupt when OVRN, PE or FE is set, and

ASCI0 requests an interrupt when  $\overline{\text{DCD0}}$  goes High. RIE is cleared to 0 by RESET.

**$\overline{\text{DCD0}}$ : Data Carrier Detect (Bit 2 STAT0).** This bit is set to 1 when the pin is High. It is cleared to 0 on the first READ of STAT0 following the pin's transition from High to Low and during RESET. When bit 6 of the ASEXTO register is 0 to select auto-enabling, and the pin is negated (High), the receiver is reset and its operation is inhibited.

**$\overline{\text{CTS1E}}$ : Clear To Send (Bit 2 STAT1).** Channel 1 features an external  $\overline{\text{CTS1}}$  input, which is multiplexed with the receive data pin RSX for the CSI/O. Setting this bit to 1 selects the CTS1 function; clearing the bit to 0 selects the RXS function.

**TDRE: Transmit Data Register Empty (Bit 1).** TDRE = 1 indicates that the TDR is empty and the next transmit data byte is written to TDR. After the byte is written to TDR, TDRE is cleared to 0 until the ASCI transfers the byte from TDR to the TSR and then TDRE is again set to 1. TDRE is set to 1 in IOSTOP mode and during RESET. On ASCI0, if the  $\overline{\text{CTS0}}$  pin is auto-enabled in the ASEXTO register and the pin is High, TDRE is reset to 0.

**TIE: Transmit Interrupt Enable (Bit 0).** TIE should be set to 1 to enable ASCI transmit interrupt requests. If TIE = 1, an interrupt is requested when TDRE = 1. TIE is cleared to 0 during RESET.

ASCI TRANSMIT DATA REGISTERS

Register addresses 06H and 07H hold the ASCI transmit data for channel 0 and channel 1, respectively.

ASCI Transmit Data Registers Channel 0

Mnemonic TDR0  
Address 06H

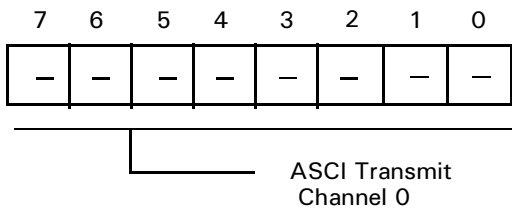


Figure 36. ASCII Register

ASCI Transmit Data Registers Channel 1

Mnemonic TDR1  
Address 07H

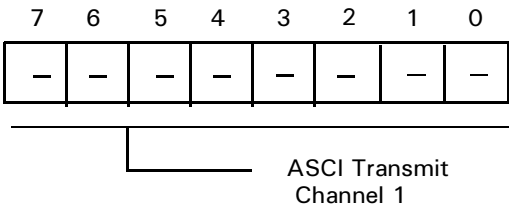


Figure 37. ASCII Register

ASCI EXTENSION CONTROL REGISTER CHANNEL 0 AND CHANNEL 1 (Continued)

Timer Data Register Channel 1 Low

Mnemonic TMDR1L  
Address 14H

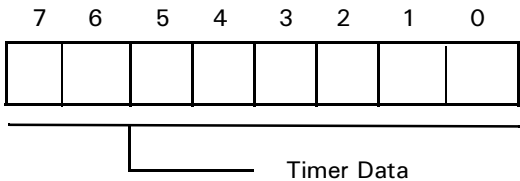


Figure 48. Timer Data Register 1 Low

Timer Reload Register Channel 1 High

Mnemonic RLDR1H  
Address 17H

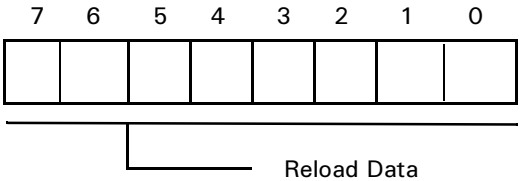


Figure 51. Timer Reload Register Channel 1 High

Timer Data Register Channel 1 High

Mnemonic TMDR1H  
Address 15H

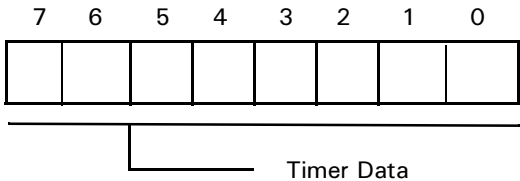


Figure 49. Timer Data Register 1 High

Free Running Counter (Read Only)

Mnemonic FRC  
Address 18H

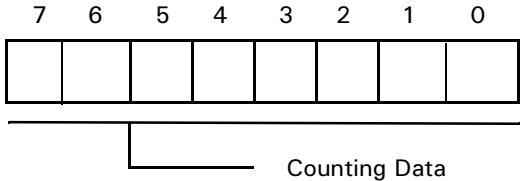


Figure 52. Free Running Counter

Timer Reload Register Channel 1 Low

Mnemonic RLDR1L  
Address 16

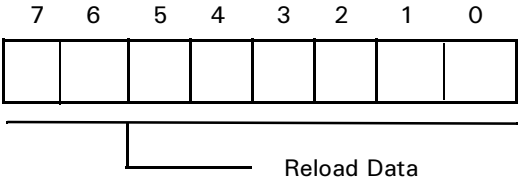


Figure 50. Timer Reload Channel 1 Low

DMA SOURCE ADDRESS REGISTER CHANNEL 0

The DMA Source Address Register Channel 0 specifies the physical source address for channel 0 transfers. The register contains 20 bits and can specify up to 1024 KB memory addresses or up to 64-KB I/O addresses. Channel 0 source can be memory, I/O, or memory mapped I/O. For I/O, bits 17–16 of this register identify the Request Handshake signal.

DMA Source Address Register, Channel 0 Low

Mnemonic SAR0L  
Address 20H

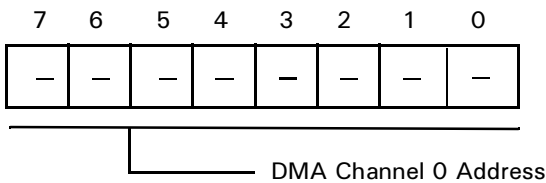


Figure 55. DMA Source Address Register 0 Low

DMA Source Address Register, Channel 0 High

Mnemonic SAR0H  
Address 21H

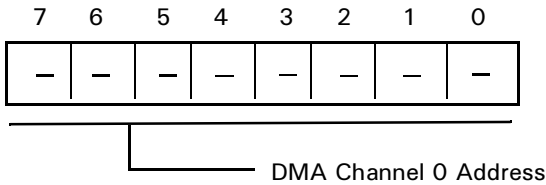


Figure 56. DMA Source Address Register 0 High

DMA Source Address Register Channel 0B

Mnemonic SAR0B  
Address 22H

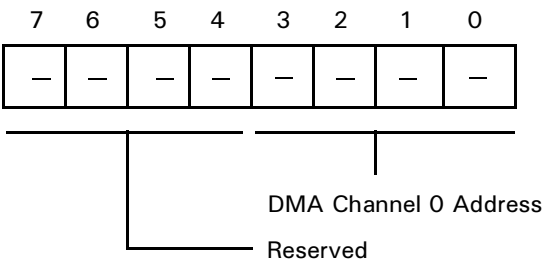


Figure 57. DMA Source Address Register 0B

If the source is in I/O space, bits 1–0 of this register select the DMA request signal for DMA0, as follows:

| Bit 1<br>(A17) | Bit 0<br>(A16) | DMA Transfer Request |
|----------------|----------------|----------------------|
| 0              | 0              | DREQ0 (external)     |
| 0              | 1              | RDRF (ASCIO)         |
| 1              | 0              | RDRF (ASC11)         |
| 1              | 1              | Reserved             |

DMA BYTE COUNT REGISTER CHANNEL 0

The DMA Byte Count Register Channel 0 specifies the number of bytes to be transferred. This register contains 16 bits and may specify up to 64-KB transfers. When one byte is transferred, the register is decremented by one. If n bytes should be transferred, n must be stored before the DMA operation.

**Note:** All DMA Count Register channels are undefined during RESET.

DMA Byte Count Register Channel 0 Low

Mnemonic BCR0L  
Address 26H



Figure 61. DMA Byte Count Register 0 Low

DMA Byte Count Register Channel 0 High

Mnemonic BCR0H  
Address 27H



Figure 62. DMA Byte Count Register 0 High

DMA Byte Count Register Channel 1 Low

Mnemonic BCR1L  
Address 2EH

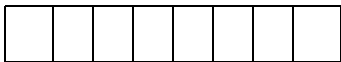


Figure 63. DMA Byte Count Register 1 Low

DMA Byte Count Register Channel 1 High

Mnemonic BCR1H  
Address 2FH



Figure 64. DMA Byte Count Register 1 High

DMA I/O ADDRESS REGISTER

The DMA I/O Address Register specifies the I/O device for channel 1 transfers. This address may be a destination or source I/O device. IAR1L and IAR1H each contain 8 address bits. The most significant byte identifies the Request Handshake signal and controls the Alternating Channel feature.

DMA I/O Address Register Channel 1 Low

Mnemonic IAR1L  
Address 2BH



Figure 68. DMA I/O Address Register Channel 1 Low

DMA I/O Address Register Channel 1 High

Mnemonic IAR1H  
Address 2CH



Figure 69. DMA I/O Address Register Channel 1 High

DMA I/O Address Register Channel 1 B

Mnemonic IAR1B  
Address 2DH

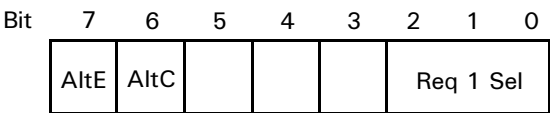


Figure 70. DMA I/O Address Register Channel 1 B

**AltE.** The AltE bit should be set only when both DMA channels are programmed for the same I/O source or I/O destination. In this case, a *channel end* condition (byte count = 0) on channel 0 sets bit 6 (AltC), which subsequently enables the channel 1 request and blocks the channel 0 request. Similarly, a channel end condition on channel 1 clears bit 6 (AltC), which then enables the channel 0 request and blocks the channel 1 request. For external requests, the request from the device must be routed or connected to both the DREQ0 and DREQ1 pins.

**AltC.** If bit (AltE) is 0, the AltC bit has no effect. When bit 7 (AltE) is 1 and the AltC bit is 0, the request signal selected by bits 2–0 is not presented to channel 1; however, the channel 0 request operates normally. When AltE is 1 and AltC is 1, the request selected by SAR18–16 or DAR18–16 is not presented to channel 0; however, the channel 1 request operates normally. The AltC bit can be written by software to select which channel should operate first; however, this operation should be executed only when both channels are stopped (both DE1 and DE0 are 0).

**Req1Sel.** If bit DIM1 in the DCNTL register is 1, indicating an I/O source, the following bits select which source handshake signal should control the transfer:

- 000 DREQ1 pin
- 001 ASCIO RDRF
- 010 ASCI1 RDRF
- Other Reserved, do not program

If DIM1 is 0, indicating an I/O destination, the following bits select which destination handshake signal should control the transfer:

- 000 DREQ1 pin
- 001 ASCIO TDRE
- 010 ASCI1 TDRE
- Other Reserved, do not program

**CA3–CA0:CA (Bits 7–4).** CA specifies the start (Low) address (on 4-KB boundaries) for Common Area 1. This condition also determines the most recent address of the Bank Area. All bits of CA are set to 1 during RESET.

**BA3–BA0 (Bits 3–0).** BA specifies the start (Low) address (on 4-KB boundaries) for the Bank Area. This condition also determines the most recent address of Common Area 0. All bits of BA are set to 1 during RESET.

OPERATION MODE CONTROL REGISTER

The Z8S180/Z8L180 is descended from two different ancestor processors, ZiLOG’s original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR) can be programmed to select between certain differences between the Z80 and the 64180.

Operation Mode Control Register

Mnemonic OMCR  
Address 3EH

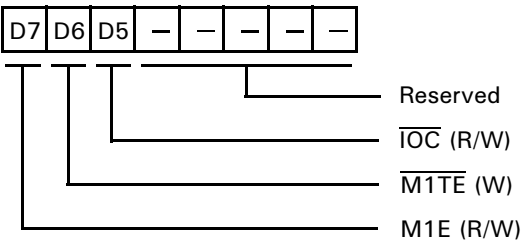


Figure 81. Operating Control Register  
(OMCR: I/O Address = 3EH)

**M1E ( $\overline{M1}$  Enable).** This bit controls the  $\overline{M1}$  output and is set to a 1 during reset.

When M1E = 1, the  $\overline{M1}$  output is asserted Low during the opcode fetch cycle, the  $\overline{INT0}$  acknowledge cycle, and the first machine cycle of the  $\overline{NMI}$  acknowledge.

On the Z8S180/Z8L180, this choice makes the processor fetch one RETI instruction. When fetching a RETI from zero-wait-state memory, the processor uses three clock machine cycles that are not fully Z80-timing-compatible.

When M1E = 0, the processor does not drive  $\overline{M1}$  Low during instruction fetch cycles. After fetching one RETI instruction with normal timing, the processor returns and refetches the instruction using Z80-compatible cycles that drive  $\overline{M1}$  Low. This timing compatibility may be required by external Z80 peripherals to properly decode the RETI instruction.

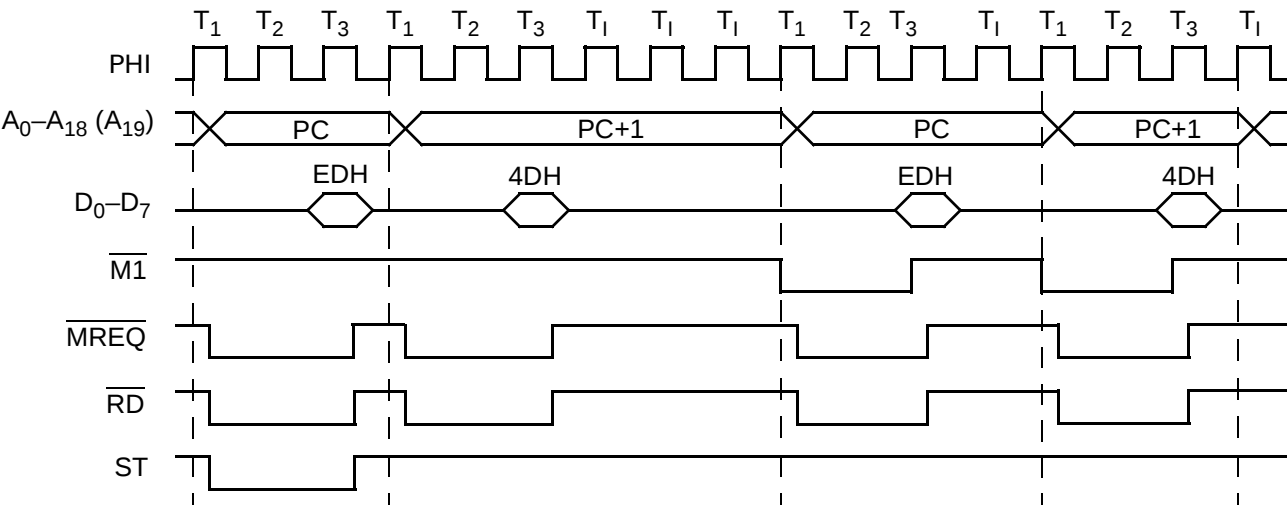


Figure 82. RETI Instruction Sequence with M1E = 0

I/O CONTROL REGISTER

The I/O Control Register (ICR) allows relocation of the internal I/O addresses. ICR also controls the enabling and disabling of IOSTOP mode (Figure 83).

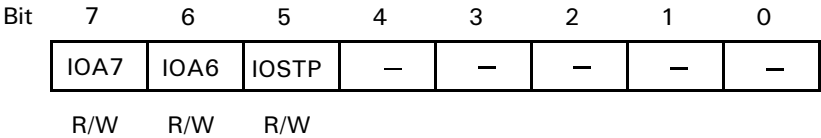


Figure 83. I/O Control Register (ICR: I/O Address = 3FH)

**IOA7, 6: I/O Address Relocation (Bits 7,6).** IOA7 and IOA6 relocate internal I/O as indicated in Figure 84.

**Note:** The high-order 8 bits of 16-bit internal I/O address are always 0. IOA7 and IOA6 are cleared to 0 during RESET.

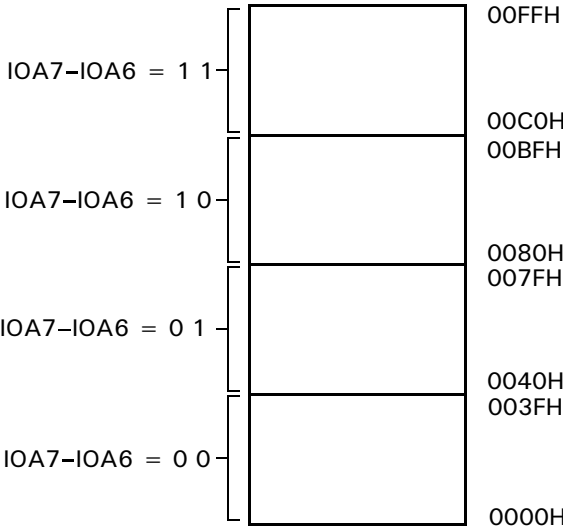


Figure 84. I/O Address Relocation

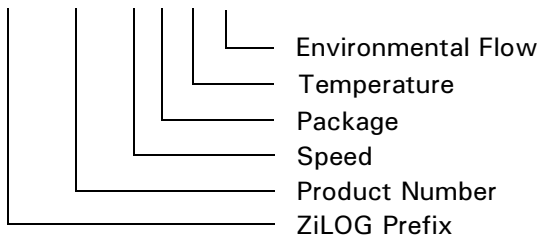
**IOSTP: IOSTOP Mode (Bit 5).** IOSTOP mode is enabled when IOSTP is set to 1. Normal I/O operation resumes when IOSTP is reprogrammed or RESET to 0.

ORDERING INFORMATION

| Codes         |                        |
|---------------|------------------------|
| Speed         | 10 = 10 MHz            |
|               | 20 = 20 MHz            |
|               | 33 = 33 MHz            |
| Package       | P = 60-Pin Plastic DIP |
|               | V = 68-Pin PLCC        |
|               | F = 80-Pin QFP         |
| Temperature   | S = 0°C to +70°C       |
|               | E = -40°C to +85°C     |
| Environmental | C = Plastic Standard   |

For fast results, contact your local ZiLOG sales office for assistance in ordering the part(s) required.

Example:  
Z 8S180 10 P S C is a Z8S180 10-MHz 60-Pin DIP, 0° to +70°C, Plastic Standard Flow



Pre-Characterization Product

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or non-conformance

with some aspects of the document may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

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