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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	64-DIP (0.750", 19.05mm)
Supplier Device Package	64-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8s18010pec

PIN IDENTIFICATION

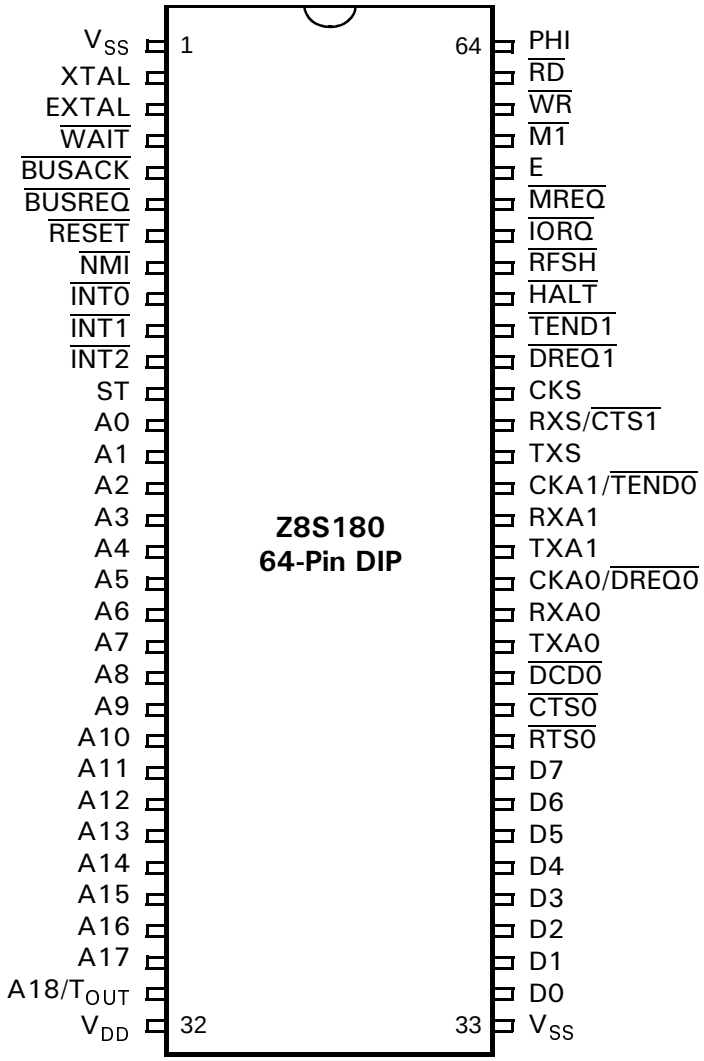


Figure 2. Z8S180 64-Pin DIP Pin Configuration

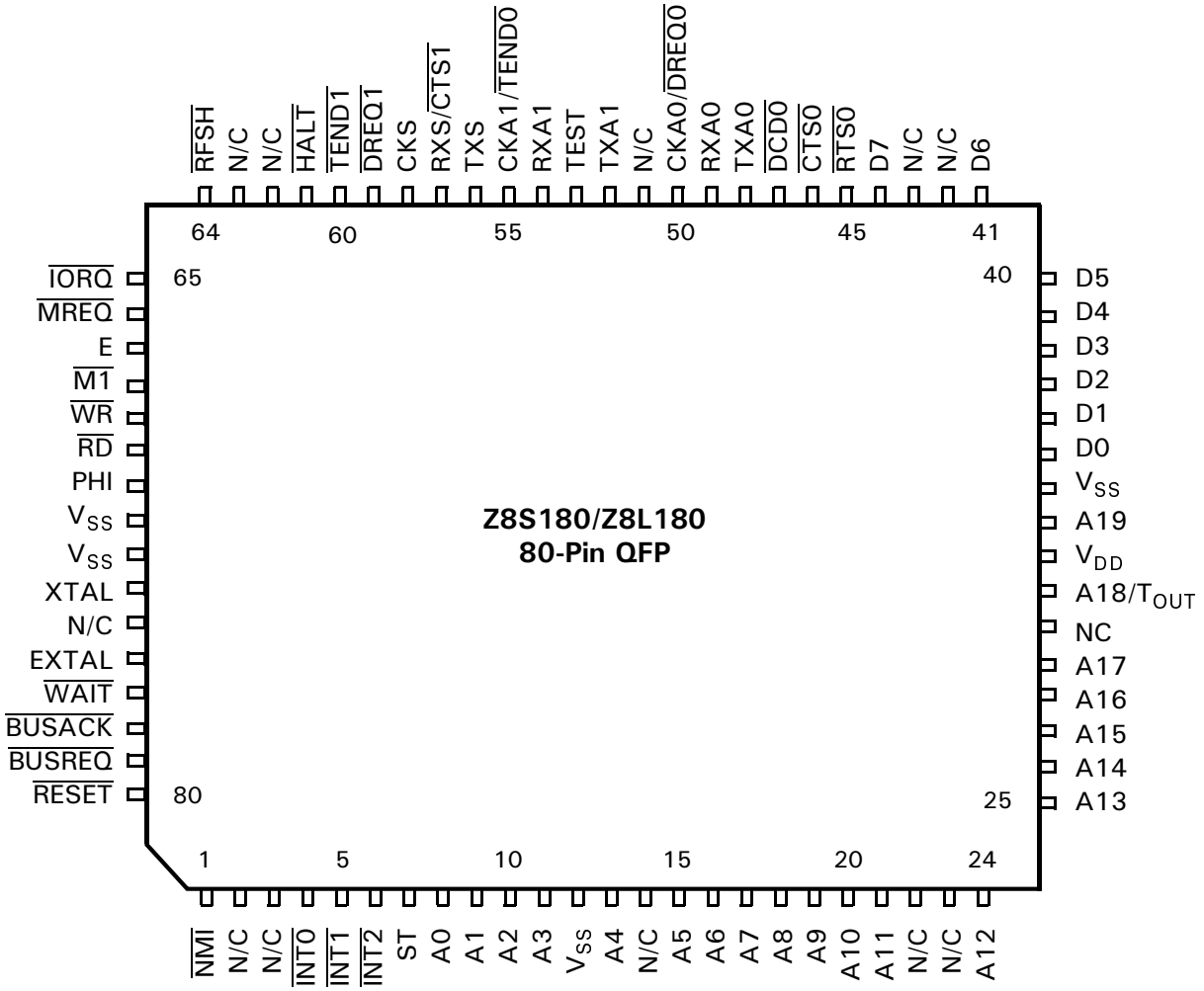


Figure 4. Z8S180/Z8L180 80-Pin QFP Pin Configuration

Table 1. Z8S180/Z8L180 Pin Identification

Pin Number and Package Type			Default	Secondary	
QFP	PLCC	DIP	Function	Function	Control
1	9	8	$\overline{NMI}$		
2			NC		
3			NC		
4	10	9	$\overline{INT0}$		
5	11	10	$\overline{INT1}$		
6	12	11	$\overline{INT2}$		
7	13	12	ST		
8	14	13	A0		
9	15	14	A1		
10	16	15	A2		
11	17	16	A3		
12	18		V_{SS}		

Table 1. Z8S180/Z8L180 Pin Identification (Continued)

Pin Number and Package Type			Default	Secondary	
QFP	PLCC	DIP	Function	Function	Control
53	52		TEST		
54	53	49	RXA1		
55	54	50	CKA1	$\overline{\text{TEND0}}$	Bit 4 of CNTLA1
56	55	51	TXS		
57	56	52	RXS	$\overline{\text{CTS1}}$	Bit 2 of STAT1
58	57	53	CKS		
59	58	54	$\overline{\text{DREQ1}}$		
60	59	55	$\overline{\text{TEND1}}$		
61	60	56	$\overline{\text{HALT}}$		
62			NC		
63			NC		
64	61	57	$\overline{\text{RFSH}}$		
65	62	58	$\overline{\text{IORQ}}$		
66	63	59	$\overline{\text{MREQ}}$		
67	64	60	E		
68	65	61	$\overline{\text{M1}}$		
69	66	62	$\overline{\text{WR}}$		
70	67	63	$\overline{\text{RD}}$		
71	68	64	PHI		
72	1	1	V_{SS}		
73	2		V_{SS}		
74	3	2	XTAL		
75			NC		
76	4	3	EXTAL		
77	5	4	$\overline{\text{WAIT}}$		
78	6	5	$\overline{\text{BUSACK}}$		
79	7	6	$\overline{\text{BUSREQ}}$		
80	8	7	$\overline{\text{RESET}}$		

PIN IDENTIFICATION (Continued)

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
1	9	8	$\overline{NMI}$		IN	IN	IN
2			NC				
3			NC				
4	10	9	$\overline{INT0}$		IN	IN	IN
5	11	10	$\overline{INT1}$		IN	IN	IN
6	12	11	$\overline{INT2}$		IN	IN	IN
7	13	12	ST		High	High	High
8	14	13	A0		3T	3T	High
9	15	14	A1		3T	3T	High
10	16	15	A2		3T	3T	High
11	17	16	A3		3T	3T	High
12	18		V_{SS}		V_{SS}	V_{SS}	V_{SS}
13	19	17	A4		3T	3T	High
14			NC				
15	20	18	A5		3T	3T	High
16	21	19	A6		3T	3T	High
17	22	20	A7		3T	3T	High
18	23	21	A8		3T	3T	High
19	24	22	A9		3T	3T	High
20	25	23	A10		3T	3T	High
21	26	24	A11		3T	3T	High
22			NC				
23			NC				
24	27	25	A12		3T	3T	High
25	28	26	A13		3T	3T	High
26	29	27	A14		3T	3T	High
27	30	28	A15		3T	3T	High
28	31	29	A16		3T	3T	High
29	32	30	A17		3T	3T	High
30			NC				
31	33	31	A18		3T	3T	High
			T_{OUT}		N/A	OUT	OUT
32	34	32	V_{DD}		V_{DD}	V_{DD}	V_{DD}
33	35		A19		3T	3T	High
34	36	33	V_{SS}		V_{SS}	V_{SS}	V_{SS}
35	37	34	D0		3T	3T	3T
36	38	35	D1		3T	3T	3T
37	39	36	D2		3T	3T	3T
38	40	37	D3		3T	3T	3T

PIN IDENTIFICATION (Continued)

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
76	4	3	EXTAL		IN	IN	IN
77	5	4	$\overline{\text{WAIT}}$		IN	IN	IN
78	6	5	$\overline{\text{BUSACK}}$		High	OUT	OUT
79	7	6	$\overline{\text{BUSREQ}}$		IN	IN	IN
80	8	7	$\overline{\text{RESET}}$		IN	IN	IN

PIN DESCRIPTIONS (Continued)

ways recognized at the end of an instruction, regardless of the state of the interrupt-enable flip-flops. This signal forces CPU execution to continue at location 0066H.

PHI. System Clock (Output). The output is used as a reference clock for the MPU and the external system. The frequency of this output may be one-half, equal to, or twice the crystal or input clock frequency.

$\overline{RD}$. Read (Output, active Low, 3-state). $\overline{RD}$ indicates that the CPU wants to read data from either memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus.

$\overline{RFSH}$. Refresh (Output, active Low). Together with $\overline{MREQ}$, $\overline{RFSH}$ indicates that the current CPU machine cycle and the contents of the address bus should be used for refresh of dynamic memories. The low-order 8 bits of the address bus (A7–A0) contain the refresh address. *This signal is analogous to the $\overline{REF}$ signal of the Z64180.*

$\overline{RTS0}$. Request to Send 0 (Output, active Low); a programmable MODEM control signal for ASCI channel 0.

RXA0, RXA1. Receive Data 0 and 1 (Input). These signals are the receive data for the ASCI channels.

RXS. Clocked Serial Receive Data (Input). This line is the receive data for the CSI/O channel. RXS is multiplexed with the $\overline{CTS1}$ signal for ASCI channel 1.

ST. Status (Output). This signal is used with the $\overline{M1}$ and $\overline{HALT}$ output to decode the status of the CPU machine cycle. See Table 3.

Table 3. Status Summary

ST	$\overline{HALT}$	$\overline{M1}$	Operation
0	1	0	CPU Operation (1st Opcode Fetch)
1	1	0	CPU Operation (2nd Opcode and 3rd Opcode Fetch)
1	1	1	CPU Operation (MC Except Opcode Fetch)
0	X	1	DMA Operation
0	0	0	HALT Mode
1	0	1	SLEEP Mode (Including SYSTEM STOP Mode)

Notes:
X = Do not care.
MC = Machine Cycle.

$\overline{TEND0}$, $\overline{TEND1}$. Transfer End 0 and 1 (Outputs, active Low). This output is asserted active during the most recent WRITE cycle of a DMA operation. It is used to indicate the end of the block transfer. $\overline{TEND0}$ is multiplexed with CKA1.

TEST. Test (Output, not in DIP version). This pin is for test and should be left open.

T_{OUT}. Timer Out (Output). T_{OUT} is the output from PRT channel 1. This line is multiplexed with A18 of the address bus.

TXA0, TXA1. Transmit Data 0 and 1 (Outputs). These signals are the transmitted data from the ASCI channels. Transmitted data changes are with respect to the falling edge of the transmit clock.

TXS. Clocked Serial Transmit Data (Output). This line is the transmitted data from the CSI/O channel.

$\overline{WAIT}$. Wait (Input, active Low). $\overline{WAIT}$ indicates to the MPU that the addressed memory or I/O devices are not ready for data transfer. This input is sampled on the falling edge of T2 (and subsequent WAIT states). If the input is sampled Low, then the additional WAIT states are inserted until the $\overline{WAIT}$ input is sampled High, at which time execution continues.

$\overline{WR}$. WRITE (Output, active Low, 3-state). $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

XTAL. Crystal Oscillator Connection (Input). This pin should be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (see DC Characteristics).

Several pins are used for different conditions, depending on the circumstance.

ARCHITECTURE (Continued)

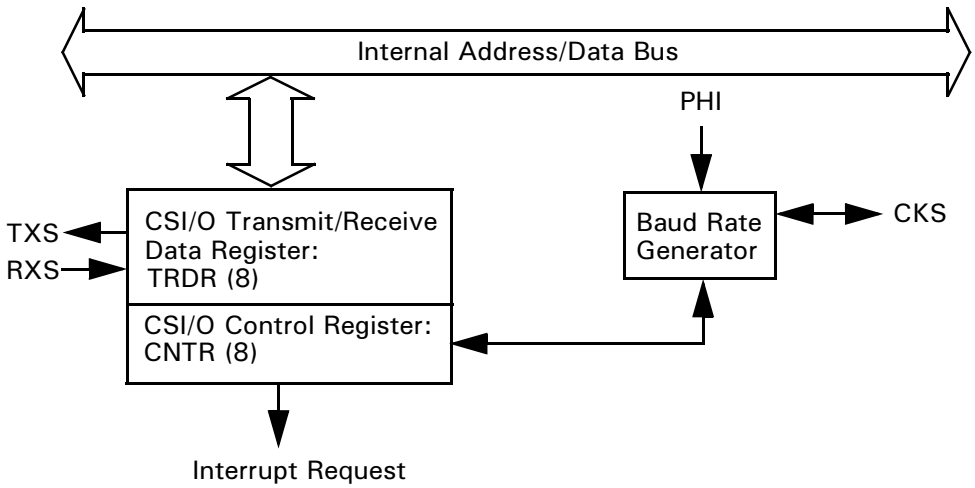


Figure 7. CSI/O Block Diagram

OPERATION MODES

Z80 versus 64180 Compatibility. The Z8S180/Z8L180 is descended from two different "ancestor" processors, ZiLOG's original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR), illustrated in Figure 8, can be programmed to select between certain Z80 and 64180 differences.

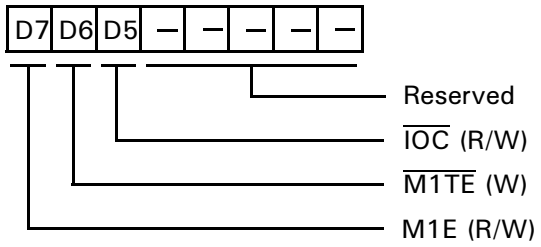


Figure 8. Operating Control Register (OMCR: I/O Address = 3EH)

M1E ($\overline{M1}$ Enable). This bit controls the $\overline{M1}$ output and is set to a 1 during RESET.

When M1E = 1, the $\overline{M1}$ output is asserted Low during opcode fetch cycles, Interrupt Acknowledge cycles, and the first machine cycle of an $\overline{NMI}$ acknowledge.

On the Z8S180/Z8L180, this choice makes the processor fetch a RETI instruction one time. When fetching a RETI from a zero-wait-state memory location, the processor uses three clock bus cycles. These bus cycles are not fully Z80-timing compatible.

When M1E = 0, the processor does not drive $\overline{M1}$ Low during the instruction fetch cycles. After fetching a RETI instruction with normal timing, the processor goes back and refetches the instruction using fully Z80-compatible cycles that include driving $\overline{M1}$ Low. This option may be required by some external Z80 peripherals to properly decode the RETI instruction. Figure 9 and Table 5 show the RETI sequence when M1E is 0.

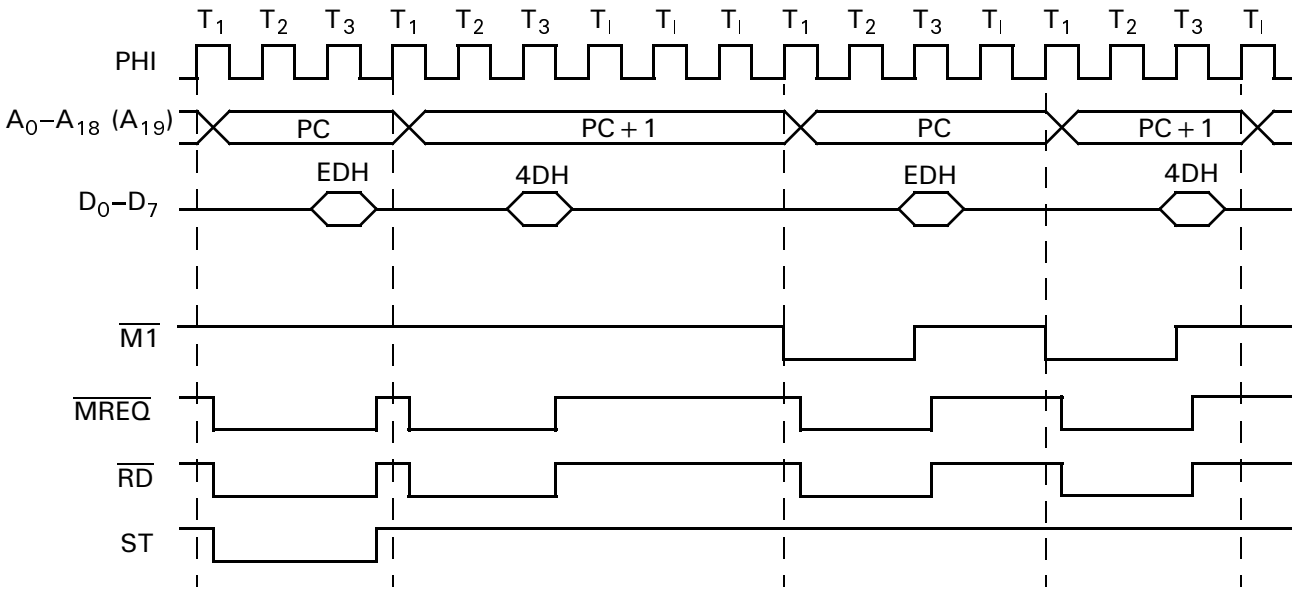


Figure 9. RETI Instruction Sequence with M1E = 0

OPERATION MODES (Continued)

Table 5. RETI Control Signal States

Machine Cycle	States	Address	Data	$\overline{RD}$	$\overline{WR}$	$\overline{MREQ}$	$\overline{IORQ}$	$\overline{M1}$ M1E = 1	$\overline{M1}$ M1E = 0	$\overline{HALT}$	ST
1	T1–T3	1st Opcode	EDH	0	1	0	1	0	1	1	0
2	T1–T3	2nd Opcode	4DH	0	1	0	1	0	1	1	0
	Ti	NA	3-state	1	1	1	1	1	1	1	1
	Ti	NA	3-state	1	1	1	1	1	1	1	1
	Ti	NA	3-state	1	1	1	1	1	1	1	1
3	T1–T3	1st Opcode	EDH	0	1	0	1	0	0	1	1
	Ti	NA	3-state	1	1	1	1	1	1	1	1
4	T1–T3	2nd Opcode	4DH	0	1	0	1	0	1	1	1
5	T1–T3	SP	Data	0	1	0	1	1	1	1	1
6	T1–T3	SP + 1	Data	0	1	0	1	1	1	1	1

$\overline{M1TE}$ ($\overline{M1}$ Temporary Enable). This bit controls the temporary assertion of the $\overline{M1}$ signal. It is always read back as a 1 and is set to 1 during RESET.

When M1E is set to 0 to accommodate certain external Z80 peripheral(s), those same device(s) may require a pulse on $\overline{M1}$ after programming certain of their registers to complete the function being programmed.

For example, when a control word is written to the Z80 PIO to enable interrupts, no enable actually takes place until the PIO sees an active $\overline{M1}$ signal. When $\overline{M1TE}$ = 1, there is no change in the operation of the $\overline{M1}$ signal, and M1E controls its function. When $\overline{M1TE}$ = 0, the $\overline{M1}$ output is asserted during the next opcode fetch cycle regardless of the state programmed into the M1E bit. This condition is only momentary (one time) and it is not necessary to preprogram a 1 to disable the function (see Figure 10).

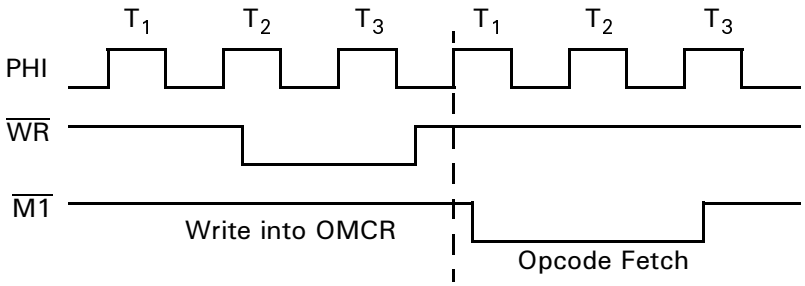


Figure 10. M1 Temporary Enable Timing

IOC (I/O Compatibility). This bit controls the timing of the $\overline{IORQ}$ and $\overline{RD}$ signals. The bit is set to 1 by RESET.

When $\overline{IOC}$ = 1, the $\overline{IORQ}$ and $\overline{RD}$ signals function the same as the Z64180 (Figure 11).

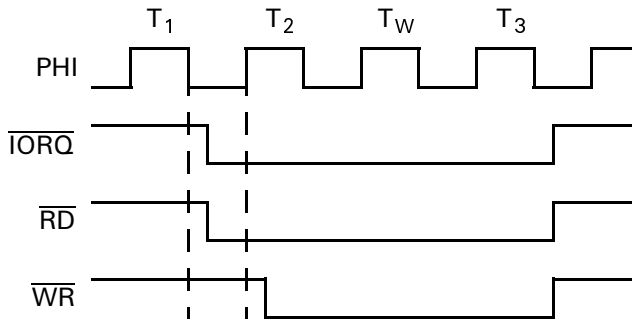


Figure 11. I/O Read and Write Cycles with $\overline{IOC}$ = 1

When $\overline{IOC}$ = 0, the timing of the $\overline{IORQ}$ and $\overline{RD}$ signals match the timing of the Z80. The $\overline{IORQ}$ and $\overline{RD}$ signals go active as a result of the rising edge of T2. (Figure 12.)

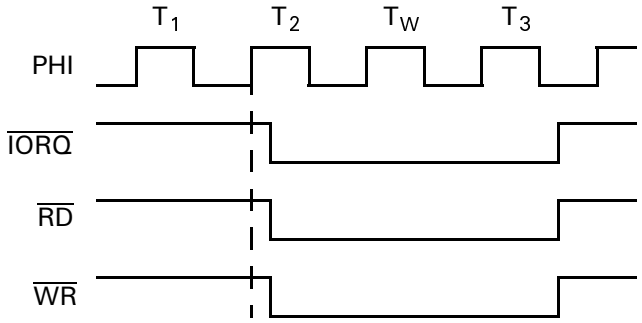


Figure 12. I/O Read and Write Cycles with $\overline{IOC}$ = 0

HALT and Low-Power Operating Modes. The Z8S180/Z8L180 can operate in seven modes with respect to activity and power consumption:

- Normal Operation
- HALT Mode
- IOSTOP Mode
- SLEEP Mode
- SYSTEM STOP Mode
- IDLE Mode
- STANDBY Mode (with or without QUICK RECOVERY)

Normal Operation. In this state, the Z8S180/Z8L180 processor is fetching and running a program. All enabled functions and portions of the device are active, and the $\overline{HALT}$ pin is High.

HALT Mode. This mode is entered by the HALT instruction. Thereafter, the Z8S180/Z8L180 processor continually fetches the following opcode but does not execute it and drives the $\overline{HALT}$, ST and $\overline{M1}$ pins all Low. The oscillator and PHI pin remain Active. Interrupts and bus granting to external Masters, and DRAM refresh can occur, and all on-chip I/O devices continue to operate including the DMA channels.

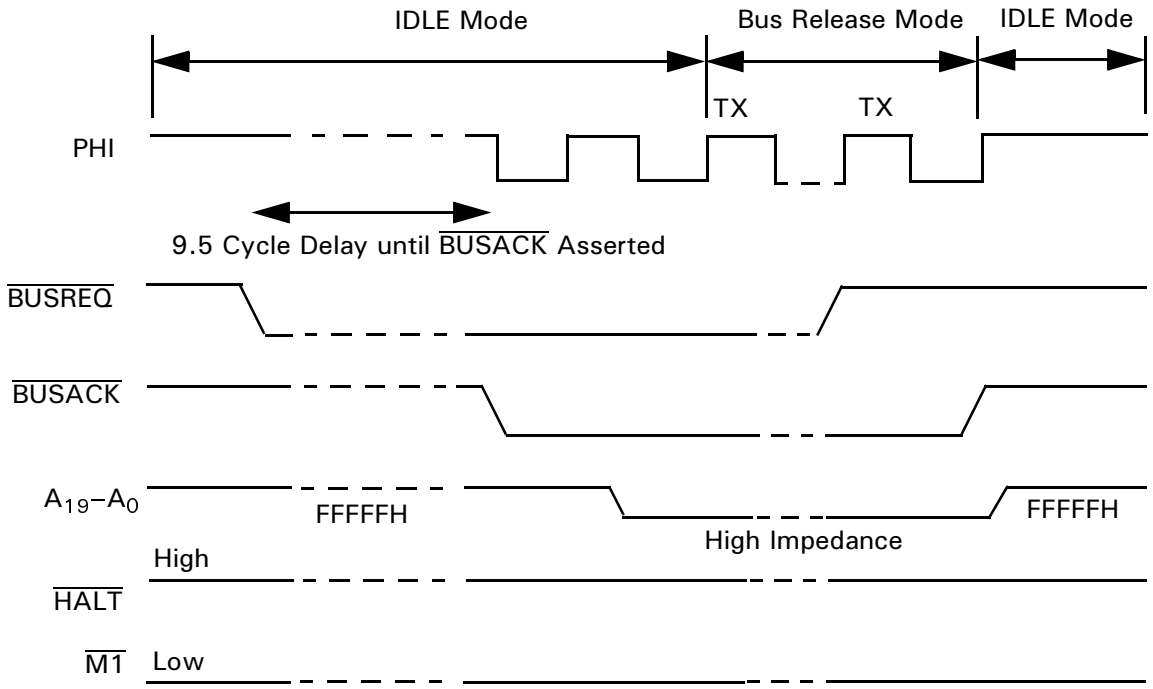


Figure 16. Bus Granting to External Master in IDLE Mode

STANDBY Mode (With or Without QUICK RECOVERY).

Software can put the Z8S180/Z8L180 into this mode by setting the IOSTOP bit (ICR5) to 1, CCR6 to 1, and executing the SLP instruction. This mode stops the on-chip oscillator and thus draws the least power of any mode, less than 10µA.

As with IDLE mode, the Z8S180/Z8L180 leaves STANDBY mode in response to a Low on $\overline{\text{RESET}}$, on $\overline{\text{NMI}}$, or a Low on $\overline{\text{INT0–2}}$ that is enabled by a 1 in the corresponding bit in the INT/TRAP Control Register. This action grants the bus to an external Master if the BREXT bit in the CPU Control Register (CCR5) is 1. The time required for all of these operations is greatly increased by the necessity for restarting the on-chip oscillator, and ensuring that it stabilizes to square-wave operation.

When an external clock is connected to the EXTAL pin rather than a crystal to the XTAL and EXTAL pins and the external clock runs continuously, there is little necessity to use STANDBY mode because no time is required to restart the oscillator, and other modes restart faster. However, if external logic stops the clock during STANDBY mode (for example, by decoding $\overline{\text{HALT}}$ Low and $\overline{\text{M1}}$ High for several clock cycles), then STANDBY mode can be useful to allow the external clock source to stabilize after it is re-enabled.

When external logic drives $\overline{\text{RESET}}$ Low to bring the device out of STANDBY mode, and a crystal is in use or an external clock source is stopped, the external logic must hold $\overline{\text{RESET}}$ Low until the on-chip oscillator or external clock source is restarted and stabilized.

The clock-stability requirements of the Z8S180/Z8L180 are much less in the divide-by-two mode that is selected by a RESET sequence and controlled by the Clock Divide bit in the CPU Control Register (CCR7). As a result, software performs the following actions:

1. Sets CCR7 to 0 for divide-by-two mode before an SLP instruction and STANDBY mode.
2. Delays setting CCR7 back to 1 for divide-by-one mode as long as possible to allow additional clock stabilization time after a RESET, interrupt, or in-line RESTART after an SLP 01 instruction.

If CCR6 is set to 1 before the SLP instruction places the MPU in STANDBY mode, the value of the CCR3 bit determines the length of the delay before the oscillator restarts and stabilizes when it leaves STANDBY mode due to an external interrupt request. When CCR3 is 0, the Z8S180/Z8L180 waits 2^{17} (131,072) clock cycles. When CCR3 is 1, it waits 64 clock cycles. This state is called QUICK RECOVERY mode. The same delay applies to grant-

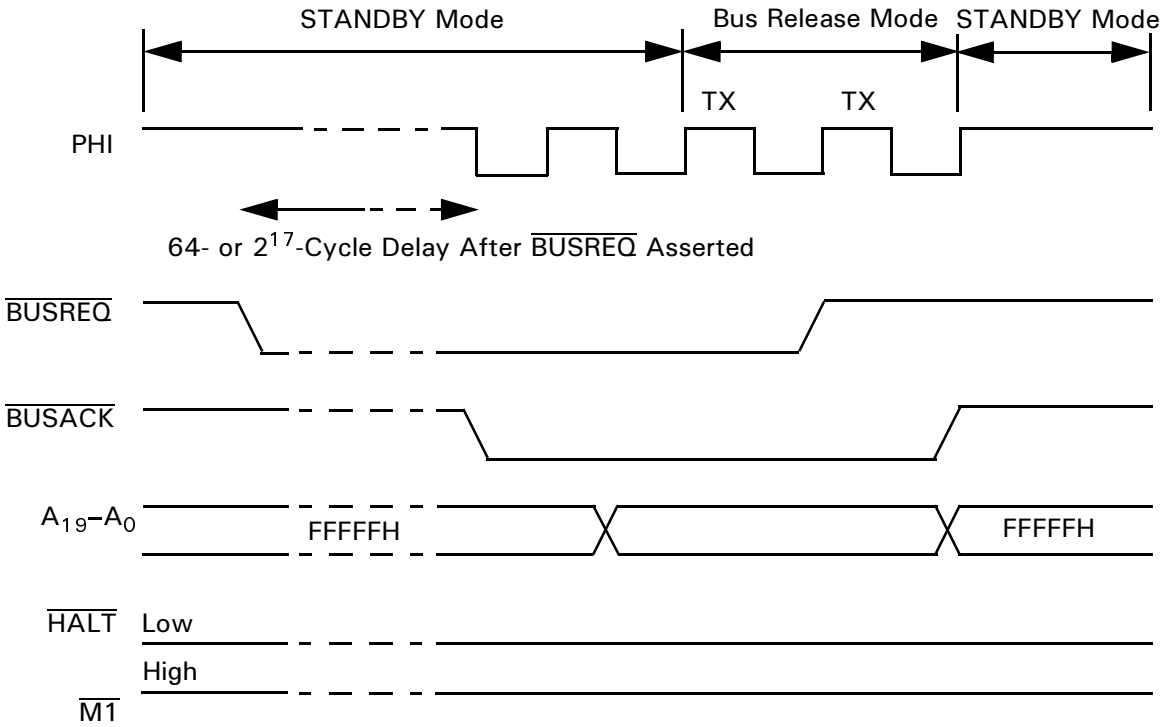


Figure 18. Bus Granting to External Master During STANDBY Mode

Table 8. Z8S180 AC Characteristics (Continued)
V_{DD} = 5V ±10% or V_{DD} = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation

			Z8S180—20 MHz		Z8S180—33 MHz		
Number	**Symbol**	**Item**	**Min**	**Max**	**Min**	**Max**	**Unit**
63	t_{REH}	$\overline{RESET}$ Hold Time from PHI Fall	25	—	15	—	ns
64	t_{OSC}	Oscillator Stabilization Time	—	20	—	20	ns
65	t_{EXR}	External Clock Rise Time (EXTAL)	—	5	—	5	ns
66	t_{EXF}	External Clock Fall Time (EXTAL)	—	5	—	5	ns
67	t_{RR}	$\overline{RESET}$ Rise Time	—	50	—	50	ms
68	t_{RF}	$\overline{RESET}$ Fall Time	—	50	—	50	ms
69	t_{IR}	Input Rise Time (except EXTAL, $\overline{RESET}$)	—	50	—	50	ns
70	t_{IF}	Input Fall Time (except EXTAL, $\overline{RESET}$)	—	50	—	50	ns

CPU CONTROL REGISTER

CPU Control Register (CCR). This register controls the basic clock rate, certain aspects of Power-Down modes, and output drive/low-noise options (Figure 31).

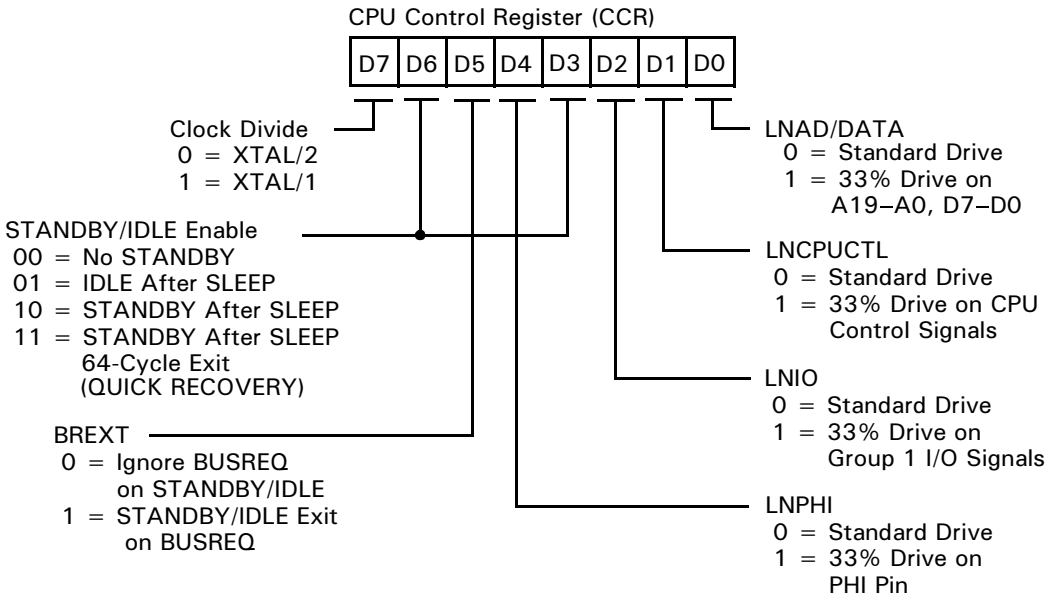


Figure 31. CPU Control Register (CCR) Address 1FH

Bit 7. Clock Divide Select. If this bit is 0, as it is after a RESET, the Z8S180/Z8L180 divides the frequency on the XTAL pin(s) by two to obtain its Master clock PHI. If this bit is programmed as 1, the part uses the XTAL frequency as PHI without division.

If an external oscillator is used in divide-by-one mode, the minimum pulse width requirement provided in the AC Characteristics must be satisfied.

Bits 6 and 3. STANDBY/IDLE Control. When these bits are both 0, a SLP instruction makes the Z8S180/Z8L180 enter SLEEP or SYSTEM STOP mode, depending on the IOSTOP bit (ICR5).

When D6 is 0 and D3 is 1, setting the IOSTOP bit (ICR5) and executing a SLP instruction puts the Z8S180/Z8L180 into IDLE mode in which the on-chip oscillator runs, but its output is blocked from the rest of the part, including PHI out.

When D6 is 1 and D3 is 0, setting IOSTOP (ICR5) and executing a SLP instruction puts the part into STANDBY mode, in which the on-chip oscillator is stopped and the part allows 2^{17} (128K) clock cycles for the oscillator to stabilize when it restarts.

When D6 and D3 are both 1, setting IOSTOP (ICR5) and executing a SLP instruction puts the part into QUICK RECOVERY STANDBY mode, in which the on-chip oscillator is stopped, and the part allows only 64 clock cycles for the oscillator to stabilize when it restarts.

The latter section, HALT and LOW POWER modes, describes the subject more fully.

Bit 5 BREXT. This bit controls the ability of the Z8S180/Z8L180 to honor a bus request during STANDBY mode. If this bit is set to 1 and the part is in STANDBY mode, a BUSREQ is honored after the clock stabilization timer is timed out.

Bit 4 LNPHI. This bit controls the drive capability on the PHI Clock output. If this bit is set to 1, the PHI Clock output is reduced to 33 percent of its drive capability.

ASCI CHANNEL CONTROL REGISTER B

ASCI Control Register B 0 (CNTLB0: I/O Address = 02H)
ASCI Control Register B 1 (CNTLB1: I/O Address = 03H)

Bit	7	6	5	4	3	2	1	0
	MPBT	MP	$\overline{CTS}$/PS	PEO	DR	SS2	SS1	SS0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 34. ASCI Channel Control Register B

MPBT: Multiprocessor Bit Transmit (Bit 7). When multiprocessor communication format is selected (MP bit = 1), MPBT is used to specify the MPB data bit for transmission. If MPBT = 1, then MPB = 1 is transmitted. If MPBT = 0, then MPB = 0 is transmitted. The MPBT state is undefined during and after RESET.

MP: Multiprocessor Mode (Bit 6). When MP is set to 1, the data format is configured for multiprocessor mode based on MOD2 (number of data bits) and MOD0 (number of stop bits) in CNTLA. The format is as follows:

Start bit + 7 or 8 data bits + MPB bit + 1 or 2 stop bits

Multiprocessor (MP = 1) format offers no provision for parity. If MP = 0, the data format is based on MOD0, MOD1, MOD2, and may include parity. The MP bit is cleared to 0 during RESET.

$\overline{CTS}$/PS: Clear to Send/Prescale (Bit 5). When read, $\overline{CTS}$/PS reflects the state of the external $\overline{CTS}$ input. If the $\overline{CTS}$ input pin is High, $\overline{CTS}$/PS is read as 1.

Note: When the $\overline{CTS}$ input pin is High, the TDRE bit is inhibited (that is, held at 0).

For channel 1, the $\overline{CTS}$ input is multiplexed with RXS pin (Clocked Serial Receive Data). Thus, $\overline{CTS}$/PS is only valid when read if the channel 1 CTS1E bit = 1 and the $\overline{CTS}$ input pin function is selected. The READ data of $\overline{CTS}$/PS is not affected by $\overline{RESET}$.

If the SS2–0 bits in this register are not 111, and the BRG mode bit in the ASEXT register is 0, then writing to this bit sets the prescale (PS) control. Under those circumstances, a 0 indicates a divide-by-10 prescale function while a 1 indicates divide-by-30. The bit resets to 0.

PEO: Parity Even Odd (Bit 4) . PEO selects oven or odd parity. PEO does not affect the enabling/disabling of parity (MOD1 bit of CNTLA). If PEO is cleared to 0, even parity is selected. If PEO is set to 1, odd parity is selected. PEO is cleared to 0 during RESET.

DR: Divide Ratio (Bit 3). If the X1 bit in the ASEXT register is 0, this bit specifies the divider used to obtain baud rate from the data sampling clock. If DR is reset to 0, divide-by-16 is used, while if DR is set to 1, divide-by-64 is used. DR is cleared to 0 during RESET.

SS2,1,0: Source/Speed Select 2,1,0 (Bits 2–0). First, if these bits are 111, as they are after a RESET, the CKA pin is used as a clock input, and is divided by 1, 16, or 64 depending on the DR bit and the X1 bit in the ASEXT register.

If these bits are not 111 and the BRG mode bit is ASEXT is 0, then these bits specify a power-of-two divider for the PHI clock as indicated in Table 10.

Setting or leaving these bits as 111 makes sense for a channel only when its CKA pin is selected for the CKA function. CKAO/CKS offers the CKAO function when bit 4 of the System Configuration Register is 0. $\overline{DCD0}$/CKA1 offers the CKA1 function when bit 0 of the Interrupt Edge register is 1.

Table 10. Divide Ratio

SS2	SS1	SS0	Divide Ratio
0	0	0	÷1
0	0	1	÷2
0	1	0	÷4
0	1	1	÷8
1	0	0	÷16
1	0	1	÷32
1	1	0	÷64
1	1	1	External Clock

ASCI0 requests an interrupt when $\overline{DCD0}$ goes High. RIE is cleared to 0 by RESET.

$\overline{DCD0}$: Data Carrier Detect (Bit 2 STAT0). This bit is set to 1 when the pin is High. It is cleared to 0 on the first READ of STAT0 following the pin's transition from High to Low and during RESET. When bit 6 of the ASEXT0 register is 0 to select auto-enabling, and the pin is negated (High), the receiver is reset and its operation is inhibited.

$\overline{CTS1E}$: Clear To Send (Bit 2 STAT1). Channel 1 features an external $\overline{CTS1}$ input, which is multiplexed with the receive data pin RSX for the CSI/O. Setting this bit to 1 selects the CTS1 function; clearing the bit to 0 selects the RXS function.

TDRE: Transmit Data Register Empty (Bit 1). TDRE = 1 indicates that the TDR is empty and the next transmit data byte is written to TDR. After the byte is written to TDR, TDRE is cleared to 0 until the ASCI transfers the byte from TDR to the TSR and then TDRE is again set to 1. TDRE is set to 1 in IOSTOP mode and during RESET. On ASCI0, if the $\overline{CTS0}$ pin is auto-enabled in the ASEXT0 register and the pin is High, TDRE is reset to 0.

TIE: Transmit Interrupt Enable (Bit 0). TIE should be set to 1 to enable ASCI transmit interrupt requests. If TIE = 1, an interrupt is requested when TDRE = 1. TIE is cleared to 0 during RESET.

ASCI TRANSMIT DATA REGISTERS

Register addresses 06H and 07H hold the ASCI transmit data for channel 0 and channel 1, respectively.

ASCI Transmit Data Registers Channel 0

Mnemonic TDR0
Address 06H

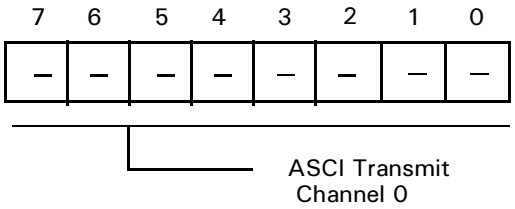


Figure 36. ASCI Register

ASCI Transmit Data Registers Channel 1

Mnemonic TDR1
Address 07H

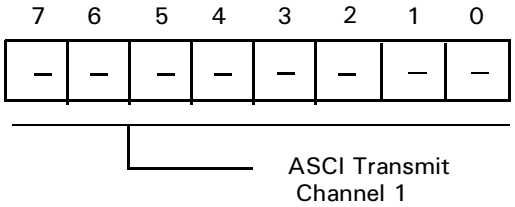


Figure 37. ASCI Register

DMA DESTINATION ADDRESS REGISTER CHANNEL 0

The DMA Destination Address Register Channel 0 specifies the physical destination address for channel 0 transfers. The register contains 20 bits and can specify up to 1024-KB memory addresses or up to 64-KB I/O addresses. Channel 0 destination can be memory, I/O, or memory mapped I/O. For I/O, the MS bits of this register identify the Request Handshake signal for channel 0.

DMA Destination Address Register Channel 0 Low

Mnemonic DAR0L
Address 23H

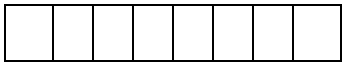


Figure 58. DMA Destination Address Register Channel 0 Low

DMA Destination Address Register Channel 0 High

Mnemonic DAR0H
Address 24H

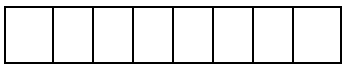


Figure 59. DMA Destination Address Register Channel 0 High

DMA Destination Address Register Channel 0B

Mnemonic DAR0B
Address 25H

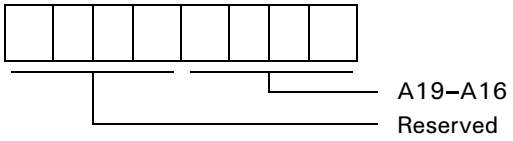


Figure 60. DMA Destination Address Register Channel 0B

If the DMA destination is in I/O space, bits 1–0 of this register select the DMA request signal for DMA0, as follows:

Bit 1 (A17)	Bit 0 (A16)	DMA Transfer Request
0	0	DREQ0 (external)
0	1	TDR0 (ASCI0)
1	0	TDR1 (ASCI1)
1	1	Not Used

CA3–CA0:CA (Bits 7–4). CA specifies the start (Low) address (on 4-KB boundaries) for Common Area 1. This condition also determines the most recent address of the Bank Area. All bits of CA are set to 1 during RESET.

BA3–BA0 (Bits 3–0). BA specifies the start (Low) address (on 4-KB boundaries) for the Bank Area. This condition also determines the most recent address of Common Area 0. All bits of BA are set to 1 during RESET.

OPERATION MODE CONTROL REGISTER

The Z8S180/Z8L180 is descended from two different ancestor processors, ZiLOG's original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR) can be programmed to select between certain differences between the Z80 and the 64180.

Operation Mode Control Register

Mnemonic OMCR
Address 3EH

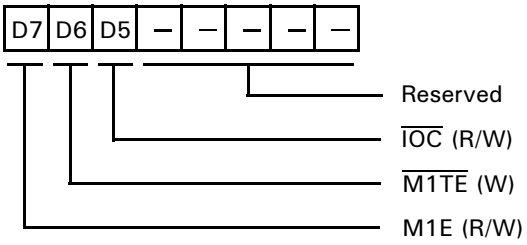


Figure 81. Operating Control Register (OMCR: I/O Address = 3EH)

M1E ($\overline{M1}$ Enable). This bit controls the $\overline{M1}$ output and is set to a 1 during reset.

When M1E = 1, the $\overline{M1}$ output is asserted Low during the opcode fetch cycle, the $\overline{INT0}$ acknowledge cycle, and the first machine cycle of the $\overline{NMI}$ acknowledge.

On the Z8S180/Z8L180, this choice makes the processor fetch one RETI instruction. When fetching a RETI from zero-wait-state memory, the processor uses three clock machine cycles that are not fully Z80-timing-compatible.

When M1E = 0, the processor does not drive $\overline{M1}$ Low during instruction fetch cycles. After fetching one RETI instruction with normal timing, the processor returns and refetches the instruction using Z80-compatible cycles that drive $\overline{M1}$ Low. This timing compatibility may be required by external Z80 peripherals to properly decode the RETI instruction.

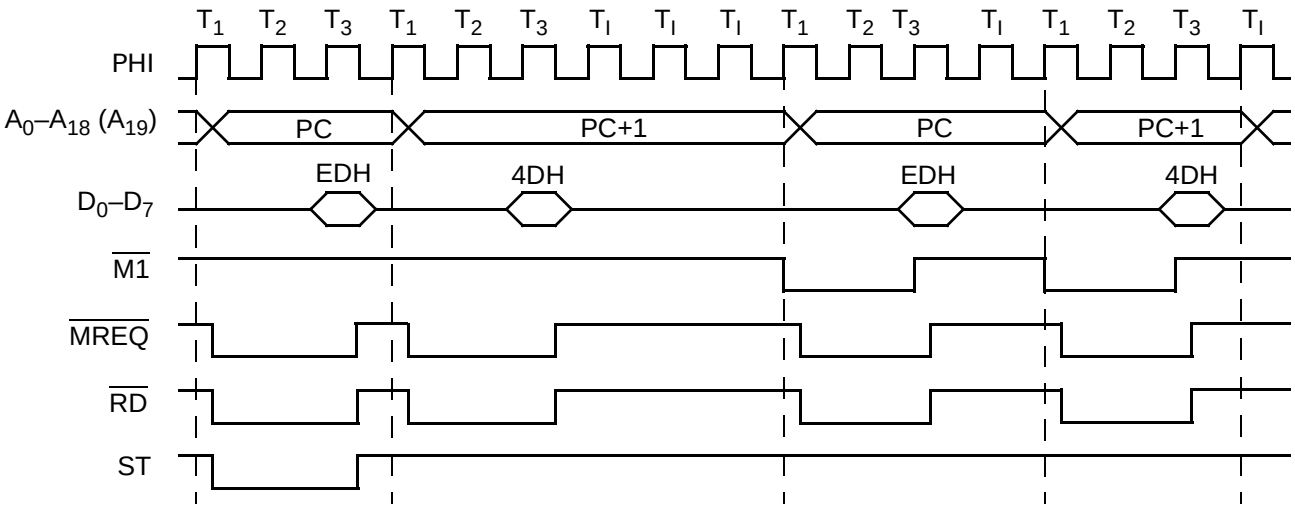
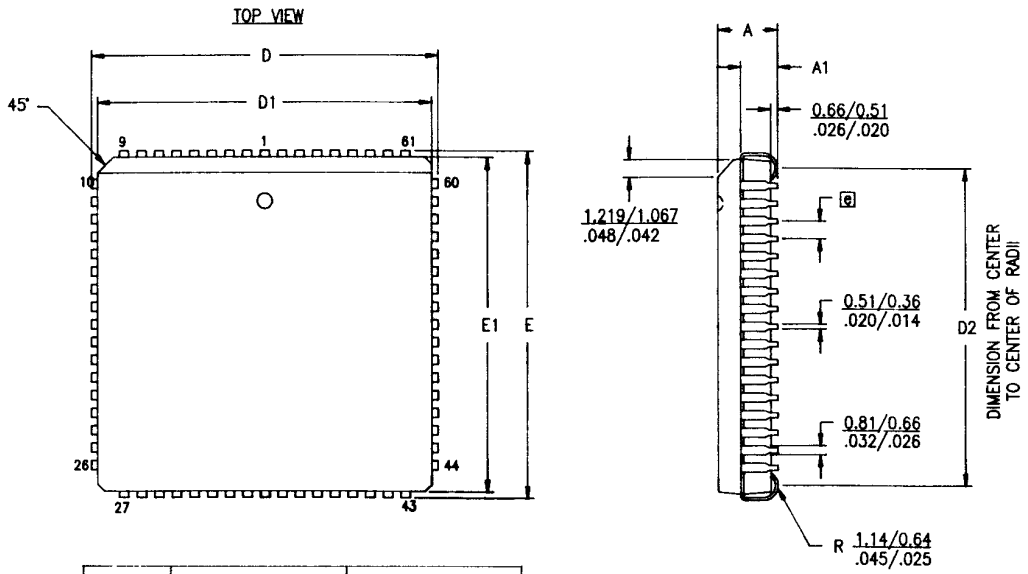


Figure 82. RETI Instruction Sequence with M1E = 0



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.32	4.57	.170	.180
A1	2.43	2.92	.095	.115
D/E	25.02	25.40	.985	1.000
D1/E1	24.13	24.33	.950	.958
D2	22.86	23.62	.900	.930
e	1.27 TYP		.050 TYP	

NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN RANGE.
3. DIMENSION : MM / INCH

Figure 87. 68-Pin PLCC Package Diagram

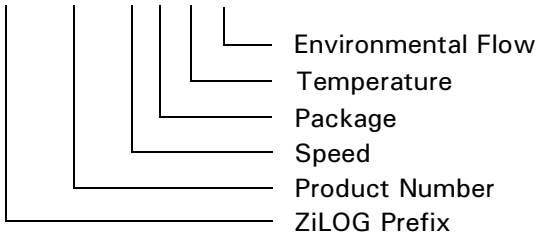
ORDERING INFORMATION

Codes	
Speed	10 = 10 MHz
	20 = 20 MHz
	33 = 33 MHz
Package	P = 60-Pin Plastic DIP
	V = 68-Pin PLCC
	F = 80-Pin QFP
Temperature	S = 0°C to +70°C
	E = –40°C to +85°C
Environmental	C = Plastic Standard

For fast results, contact your local ZiLOG sales office for assistance in ordering the part(s) required.

Example:

Z 8S180 10 P S C is a Z8S180 10-MHz 60-Pin DIP, 0° to +70°C, Plastic Standard Flow



Pre-Characterization Product

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or non-conformance with some aspects of the document may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

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