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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	64-DIP (0.750", 19.05mm)
Supplier Device Package	64-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8s18010peg

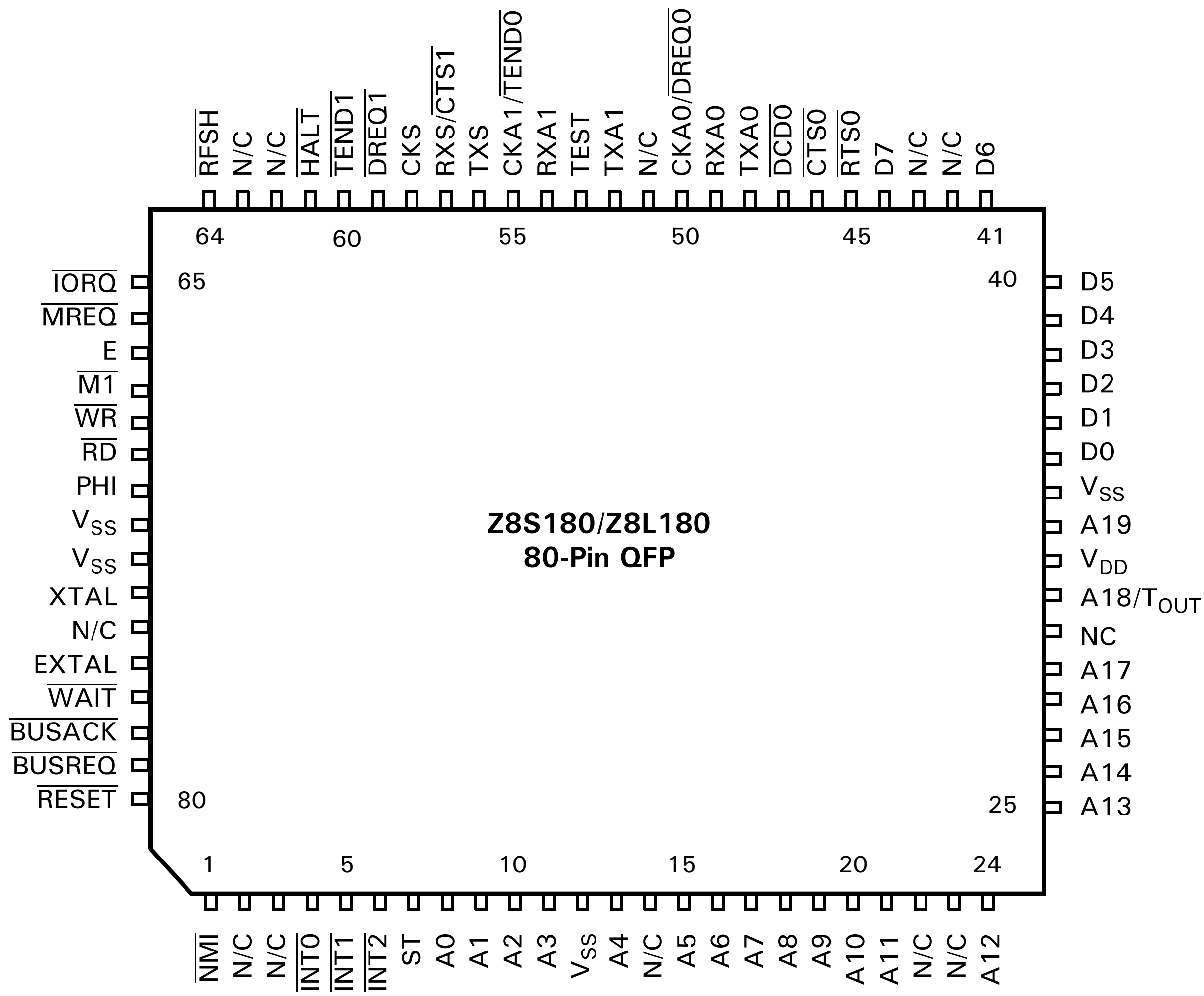

Figure 4. Z8S180/Z8L180 80-Pin QFP Pin Configuration

Table 1. Z8S180/Z8L180 Pin Identification

Pin Number and Package Type			Default	Secondary	
QFP	**PLCC**	**DIP**	**Function**	**Function**	**Control**
1	9	8	$\overline{\text{NMI}}$		
2			NC		
3			NC		
4	10	9	$\overline{\text{INT0}}$		
5	11	10	$\overline{\text{INT1}}$		
6	12	11	$\overline{\text{INT2}}$		
7	13	12	ST		
8	14	13	A0		
9	15	14	A1		
10	16	15	A2		
11	17	16	A3		
12	18		V_{SS}		

PIN IDENTIFICATION (Continued)

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
1	9	8	$\overline{NMI}$		IN	IN	IN
2			NC				
3			NC				
4	10	9	$\overline{INT0}$		IN	IN	IN
5	11	10	$\overline{INT1}$		IN	IN	IN
6	12	11	$\overline{INT2}$		IN	IN	IN
7	13	12	ST		High	High	High
8	14	13	A0		3T	3T	High
9	15	14	A1		3T	3T	High
10	16	15	A2		3T	3T	High
11	17	16	A3		3T	3T	High
12	18		V_{SS}		V_{SS}	V_{SS}	V_{SS}
13	19	17	A4		3T	3T	High
14			NC				
15	20	18	A5		3T	3T	High
16	21	19	A6		3T	3T	High
17	22	20	A7		3T	3T	High
18	23	21	A8		3T	3T	High
19	24	22	A9		3T	3T	High
20	25	23	A10		3T	3T	High
21	26	24	A11		3T	3T	High
22			NC				
23			NC				
24	27	25	A12		3T	3T	High
25	28	26	A13		3T	3T	High
26	29	27	A14		3T	3T	High
27	30	28	A15		3T	3T	High
28	31	29	A16		3T	3T	High
29	32	30	A17		3T	3T	High
30			NC				
31	33	31	A18		3T	3T	High
			T_{OUT}		N/A	OUT	OUT
32	34	32	V_{DD}		V_{DD}	V_{DD}	V_{DD}
33	35		A19		3T	3T	High
34	36	33	V_{SS}		V_{SS}	V_{SS}	V_{SS}
35	37	34	D0		3T	3T	3T
36	38	35	D1		3T	3T	3T
37	39	36	D2		3T	3T	3T
38	40	37	D3		3T	3T	3T

PIN DESCRIPTIONS

A0–A19. Address Bus (Output, 3-state). A0–A19 form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 1 MB) and I/O data bus exchanges (up to 64 KB). The address bus enters a high–impedance state during reset and external bus acknowledge cycles. Address line A18 is multiplexed with the output of PRT channel 1 (T_{OUT}, selected as address output on reset), and address line A19 is not available in DIP versions of the Z8S180.

BUSACK. Bus Acknowledge (Output, active Low). BUSACK indicates that the requesting device, the MPU address and data bus, and some control signals enter their high-impedance state.

BUSREQ. Bus Request (Input, active Low). This input is used by external devices (such as DMA controllers) to request access to the system bus. This request demands a higher priority than NMI and is always recognized at the end of the current machine cycle. This signal stops the CPU from executing further instructions, places addresses, data buses, and other control signals into the high-impedance state.

CKA0, CKA1. Asynchronous Clock 0 and 1 (bidirectional). When in output mode, these pins are the transmit and receive clock outputs from the ASCI baud rate generators. When in input mode, these pins serve as the external clock inputs for the ASCI baud rate generators. CKA0 is multiplexed with DREQ0, and CKA1 is multiplexed with TEND0.

CKS. Serial Clock (bidirectional). This line is the clock for the CSI/O channel.

CTS0–CTS1. Clear to send 0 and 1 (Inputs, active Low). These lines are modem control signals for the ASCI channels. CTS1 is multiplexed with RXS.

D0–D7. Data Bus = (bidirectional, 3-state). D0–D7 constitute an 8-bit bidirectional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high-impedance state during reset and external bus acknowledge cycles.

DCD0. Data Carrier Detect 0 (Input, active Low); a programmable modem control signal for ASCI channel 0.

DREQ0, DREQ1. DMA Request 0 and 1 (Input, active Low). DREQ is used to request a DMA transfer from one of the on-chip DMA channels. The DMA channels monitor these inputs to determine when an external device is ready for a READ or WRITE operation. These inputs can be programmed to be either level or edge sensed. DREQ0 is multiplexed with CKA0.

E. Enable Clock (Output). This pin functions as a synchronous, machine-cycle clock output during bus transactions.

EXTAL. External Clock Crystal (Input). Crystal oscillator connections. An external clock can be input to the Z8S180/Z8L180 on this pin when a crystal is not used. This input is Schmitt triggered.

HALT. HALT/SLEEP (Output, active Low). This output is asserted after the CPU executes either the HALT or SLEEP instruction and is waiting for either a nonmaskable or a maskable interrupt before operation can resume. It is also used with the M1 and ST signals to decode the status of the CPU machine cycle.

INT0. Maskable Interrupt Request 0 (Input, active Low). This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the NMI and BUSREQ signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the M1 and IORQ signals become active.

INT1, INT2. Maskable Interrupt Request 1 and 2 (Inputs, active Low). This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the NMI, BUSREQ, and INT0 signals are inactive. The CPU acknowledges these requests with an interrupt acknowledge cycle. Unlike the acknowledgment for INT0, neither the M1 or IORQ signals become active during this cycle.

IORQ. I/O Request (Output, active Low, 3-state). IORQ indicates that the address bus contains a valid I/O address for an I/O READ or I/O WRITE operation. IORQ is also generated, along with M1, during the acknowledgment of the INT0 input signal to indicate that an interrupt response vector can be place onto the data bus. This signal is analogous to the IOE signal of the Z64180.

M1. Machine Cycle 1 (Output, active Low). Together with MREQ, M1 indicates that the current cycle is the opcode-fetch cycle of instruction execution. Together with IORQ, M1 indicates that the current cycle is for interrupt acknowledgment. It is also used with the HALT and ST signal to decode the status of the CPU machine cycle. This signal is analogous to the LIR signal of the Z64180.

MREQ. Memory Request (Output, active Low, 3-state). MREQ indicates that the address bus holds a valid address for a memory READ or memory WRITE operation. This signal is analogous to the ME signal of Z64180.

NMI. Nonmaskable Interrupt (Input, negative edge triggered). NMI demands a higher priority than INT and is al-

ARCHITECTURE

The Z180 combines a high-performance CPU core with a variety of system and I/O resources useful in a broad range of applications. The CPU core consists of five functional blocks: clock generator, bus state controller, Interrupt controller, memory management unit (MMU), and the central processing unit (CPU). The integrated I/O resources make up the remaining four functional blocks: direct memory access (DMA) control (2 channels), asynchronous serial communication interface (ASCI, 2 channels) programmable reload timers (PRT, 2 channels), and a clock serial I/O (CSI/O) channel.

Clock Generator. This logic generates a system clock from an external crystal or clock input. The external clock is divided by 2 or 1 and provides the timing for both internal and external devices.

Bus State Controller. This logic performs all of the status and bus-control activity associated with the CPU and some on-chip peripherals. Also includes wait-state timing, reset cycles, DRAM refresh, and DMA bus exchanges.

Interrupt Controller. This logic monitors and prioritizes the variety of internal and external interrupts and traps to provide the correct responses from the CPU. To maintain compatibility with the Z80 CPU, three different interrupts modes are supported.

Memory Management Unit. The MMU allows the user to map the memory used by the CPU (logically only 64KB) into the 1-MB addressing range supported by the Z8S180/Z8L180. The organization of the MMU object code maintains compatibility with the Z80 CPU, while offering access to an extended memory space. Accomplished by using an effective common-area/banked-area scheme.

Central Processing Unit. The CPU is microcoded to provide a core that is object-code compatible with the Z80 CPU. It also provides a superset of the Z80 instruction set, including 8-bit multiplication. The core is modified to allow many of the instructions to execute in fewer clock cycles.

DMA Controller. The DMA controller provides high-speed transfers between memory and I/O devices. Transfer operations supported are memory-to-memory, memory to/from I/O, and I/O-to-I/O. Transfer modes supported are request, burst, and cycle steal. DMA transfers can access the full 1-MB address range with a block length up to 64 KB, and can cross over 64K boundaries.

Asynchronous Serial Communication Interface (ASCI).

The ASCI logic provides two individual full-duplex UARTs. Each channel includes a programmable baud rate generator and modem control signals. The ASCI channels can also support a multiprocessor communication format as well as break detection and generation

Programmable Reload Timers (PRT). This logic consists of two separate channels, each containing a 16-bit counter (timer) and count reload register. The time base for the counters is derived from the system clock (divided by 20) before reaching the counter. PRT channel 1 provides an optional output to allow for waveform generation.

OPERATION MODES

Z80 versus 64180 Compatibility. The Z8S180/Z8L180 is descended from two different “ancestor” processors, ZiLOG’s original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR), illustrated in Figure 8, can be programmed to select between certain Z80 and 64180 differences.

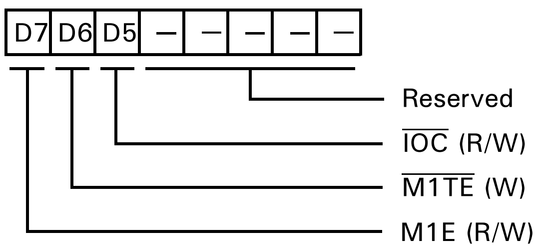

Figure 8. Operating Control Register (OMCR: I/O Address = 3EH)

M1E ($\overline{M1}$ Enable). This bit controls the $\overline{M1}$ output and is set to a 1 during RESET.

When M1E = 1, the $\overline{M1}$ output is asserted Low during opcode fetch cycles, Interrupt Acknowledge cycles, and the first machine cycle of an $\overline{NMI}$ acknowledge.

On the Z8S180/Z8L180, this choice makes the processor fetch a RETI instruction one time. When fetching a RETI from a zero-wait-state memory location, the processor uses three clock bus cycles. These bus cycles are not fully Z80-timing compatible.

When M1E = 0, the processor does not drive $\overline{M1}$ Low during the instruction fetch cycles. After fetching a RETI instruction with normal timing, the processor goes back and refetches the instruction using fully Z80-compatible cycles that include driving $\overline{M1}$ Low. This option may be required by some external Z80 peripherals to properly decode the RETI instruction. Figure 9 and Table 5 show the RETI sequence when M1E is 0.

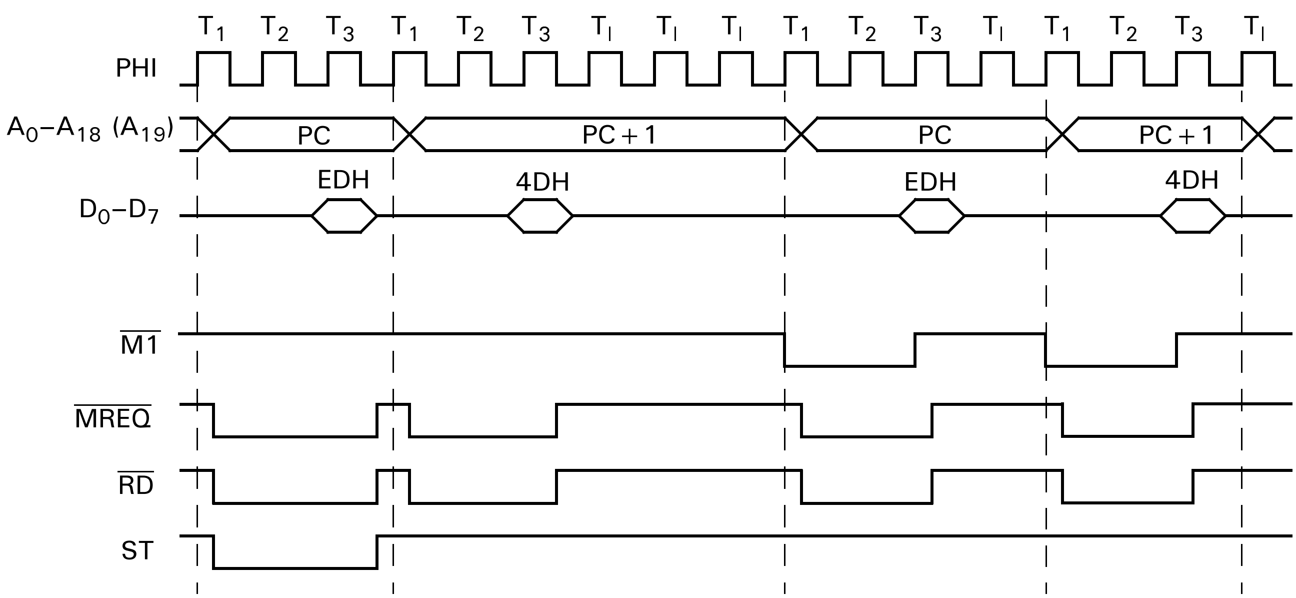

Figure 9. RETI Instruction Sequence with M1E = 0

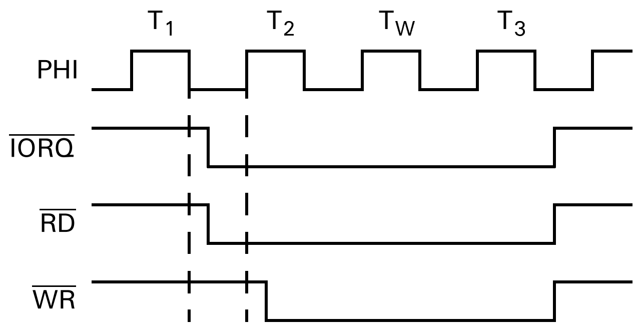

Figure 11. I/O Read and Write Cycles with $\overline{IOC}$ = 1

When $\overline{IOC}$ = 0, the timing of the $\overline{IORQ}$ and $\overline{RD}$ signals match the timing of the Z80. The $\overline{IORQ}$ and $\overline{RD}$ signals go active as a result of the rising edge of T2. (Figure 12.)

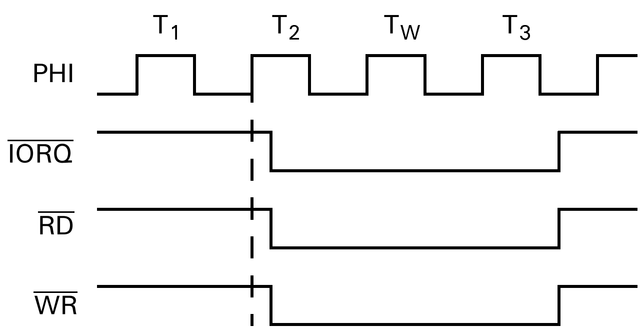

Figure 12. I/O Read and Write Cycles with $\overline{IOC}$ = 0

HALT and Low-Power Operating Modes. The Z8S180/Z8L180 can operate in seven modes with respect to activity and power consumption:

- Normal Operation
- HALT Mode
- IOSTOP Mode
- SLEEP Mode
- SYSTEM STOP Mode
- IDLE Mode
- STANDBY Mode (with or without QUICK RECOVERY)

Normal Operation. In this state, the Z8S180/Z8L180 processor is fetching and running a program. All enabled functions and portions of the device are active, and the $\overline{HALT}$ pin is High.

HALT Mode. This mode is entered by the HALT instruction. Thereafter, the Z8S180/Z8L180 processor continually fetches the following opcode but does not execute it and drives the $\overline{HALT}$, ST and $\overline{M1}$ pins all Low. The oscillator and PHI pin remain Active. Interrupts and bus granting to external Masters, and DRAM refresh can occur, and all on-chip I/O devices continue to operate including the DMA channels.

ing the bus to an external Master during STANDBY mode, when the BREXT bit in the CPU Control Register (CCR5) is 1.

As described previously for SLEEP and IDLE modes, when the MPU leaves STANDBY mode due to $\overline{\text{NMI}}$ Low or an enabled $\overline{\text{INT0}}$–$\overline{\text{INT2}}$ Low when the IEF, flag is 1 due to an IE instruction, it starts by performing the interrupt with the return address being that of the instruction following the SLP instruction. If the Z8S180/Z8L180 leaves STANDBY mode due to an external interrupt request that's enabled in the INT/TRAP Control Register, but the IEF, bit is 0 due to a DI instruction, the processor restarts by executing the instruction(s) following the SLP instruction. If $\overline{\text{INT0}}$, or $\overline{\text{INT1}}$ or $\overline{\text{INT2}}$ goes inactive before the end of the clock stabilization delay, the Z8S180/Z8L180 stays in STANDBY mode.

Figure 17 indicates the timing for leaving STANDBY mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes either 64 or 2^{17} (131,072) clocks to restart, depending on the CCR3 bit.

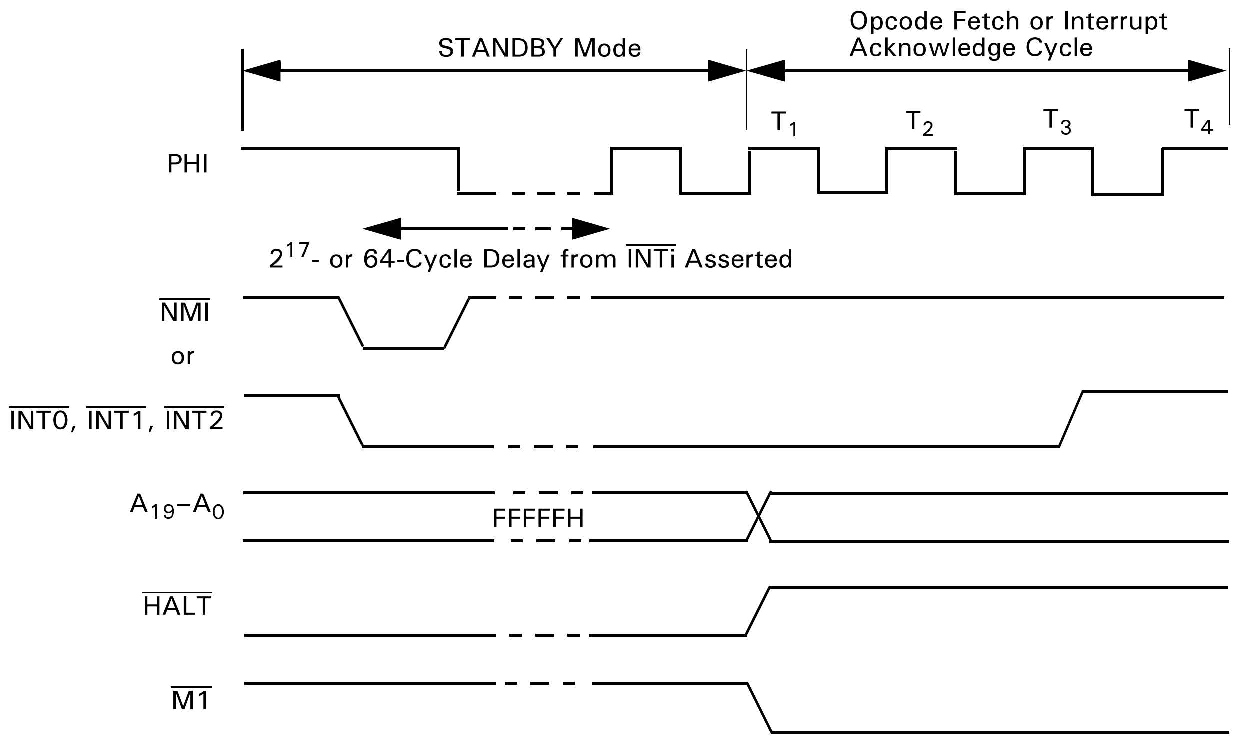

Figure 17. Z8S180/Z8L180 STANDBY Mode Exit Due to External Interrupt

While the Z8S180/Z8L180 is in STANDBY mode, it grants the bus to an external Master if the BREXT bit (CCR5) is 1. Figure 18 indicates the timing of this sequence. The device takes 64 or 2^{17} (131,072) clock cycles to grant the bus depending on the CCR3 bit. The latter (not the QUICK RECOVERY) case may be prohibitive for many demand-driven external Masters. If so, QUICK RECOVERY or IDLE mode can be used.

STANDARD TEST CONDITIONS

The following standard test conditions apply to DC Characteristics, unless otherwise noted. All voltages are referenced to V_{SS} (0V). Positive current flows into the referenced pin.

All AC parameters assume a load capacitance of 100 pF. Add a 10-ns delay for each 50-pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to V_{OL} MAX or V_{OL} MIN as indicated in Figures 20 through 30 (except for CLOCK, which is referenced to the 10% and 90% points). Ordering Information lists temperature ranges and product numbers. Find package drawings in Package Information.

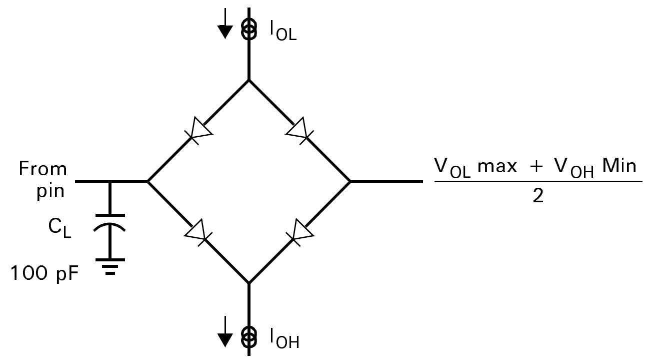

Figure 19. AC Parameter Test Circuit

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 ~ +7.0	V
Input Voltage	V_{IN}	–0.3 ~ V_{cc} +0.3	V
Operating Temperature	T_{OPR}	0 ~ 70	°C
Extended Temperature	T_{EXT}	–40 ~ 85	°C
Storage Temperature	T_{STG}	–55 ~ +150	°C

Note: Permanent damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability.

AC CHARACTERISTICS—Z8S180 (Continued)

Table 8. Z8S180 AC Characteristics (Continued)
V_{DD} = 5V ±10% or V_{DD} = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation

			Z8S180—20 MHz		Z8S180—33 MHz		
Number	**Symbol**	**Item**	**Min**	**Max**	**Min**	**Max**	**Unit**
32	t_{INTH}	$\overline{INT}$ Hold Time from PHI Fall	10	—	10	—	ns
33	t_{NMIW}	$\overline{NMI}$ Pulse Width	35	—	25	—	ns
34	t_{BRS}	$\overline{BUSREQ}$ Set-up Time to PHI Fall	10	—	10	—	ns
35	t_{BRH}	$\overline{BUSREQ}$ Hold Time from PHI Fall	10	—	10		ns
36	t_{BAD1}	PHI Rise to $\overline{BUSACK}$ Fall Delay	—	25	—	15	ns
37	t_{BAD2}	PHI Fall to $\overline{BUSACK}$ Rise Delay	—	25	—	15	ns
38	t_{BZD}	PHI Rise to Bus Floating Delay Time	—	40	—	30	ns
39	t_{MEWH}	$\overline{MREQ}$ Pulse Width (High)	35	—	25	—	ns
40	t_{MEWL}	$\overline{MREQ}$ Pulse Width (Low)	35	—	25	—	ns
41	t_{RFD1}	PHI Rise to $\overline{RFSH}$ Fall Delay	—	20	—	15	ns
42	t_{RFD2}	PHI Rise to $\overline{RFSH}$ Rise Delay	—	20	—	15	ns
43	t_{HAD1}	PHI Rise to $\overline{HALT}$ Fall Delay	—	15	—	15	ns
44	t_{HAD2}	PHI Rise to $\overline{HALT}$ Rise Delay	—	15	—	15	ns
45	t_{DRQS}	$\overline{DREQ1}$ Set-up Time to PHI Rise	20	—	15	—	ns
46	t_{DRQH}	$\overline{DREQ1}$ Hold Time from PHI Rise	20	—	15	—	ns
47	t_{TED1}	PHI Fall to $\overline{TENDi}$ Fall Delay	—	25	—	15	ns
48	t_{TED2}	PHI Fall to $\overline{TENDi}$ Rise Delay	—	25	—	15	ns
49	t_{ED1}	PHI Rise to E Rise Delay	—	30	—	15	ns
50	t_{ED2}	PHI Fall or Rise to E Fall Delay	—	30	—	15	ns
51	P_{WEH}	E Pulse Width (High)	25	—	20	—	ns
52	P_{WEL}	E Pulse Width (Low)	50	—	40	—	ns
53	t_{Er}	Enable Rise Time	—	10	—	10	ns
54	t_{Ef}	Enable Fall Time	—	10	—	10	ns
55	t_{TOD}	PHI Fall to Timer Output Delay	—	75	—	50	ns
56	t_{STDI}	CSI/O Transmit Data Delay Time (Internal Clock Operation)	—	2	—	2	tcyc
57	t_{STDE}	CSI/O Transmit Data Delay Time (External Clock Operation)	—	7.5 t_{CYC} +75	—	75 t_{CYC} +60	ns
58	t_{SRSI}	CSI/O Receive Data Set-up Time (Internal Clock Operation)	1	—	1	—	tcyc
59	t_{SRHI}	CSI/O Receive Data Hold Time (Internal Clock Operation)	1	—	1	—	tcyc
60	t_{SRSE}	CSI/O Receive Data Set-up Time (External Clock Operation)	1	—	1	—	tcyc
61	t_{SRHE}	CSI/O Receive Data Hold Time (External Clock Operation)	1	—	1	—	tcyc
62	t_{RES}	$\overline{RESET}$ Set-up Time to PHI Fall	40	—	25	—	ns

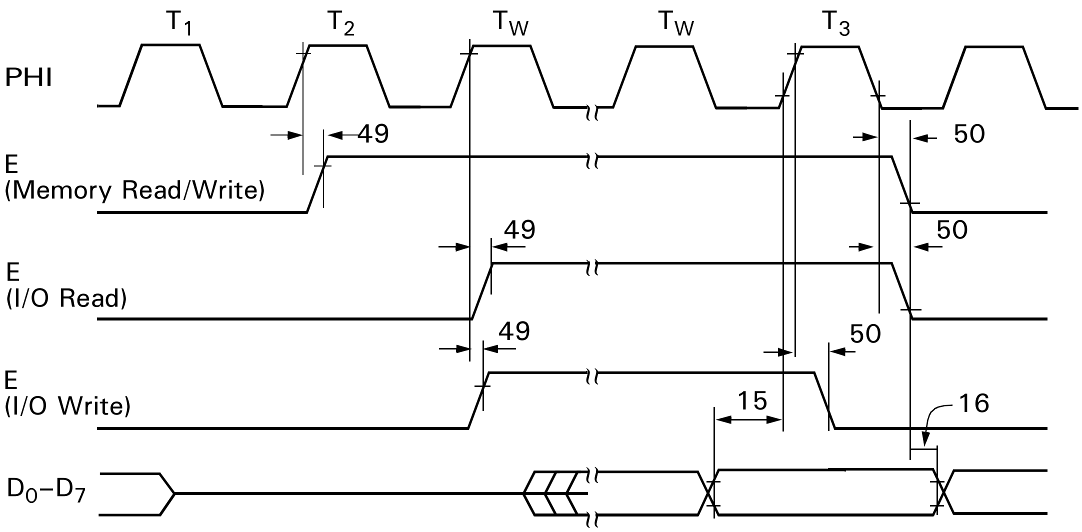

Figure 24. E Clock Timing (Memory Read/Write Cycle, I/O Read/Write Cycle)

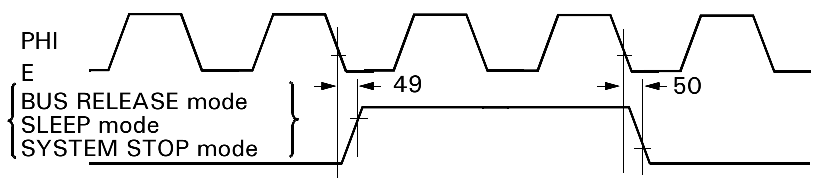

Figure 25. E Clock Timing (BUS RELEASE Mode, SLEEP Mode, SYSTEM STOP Mode)

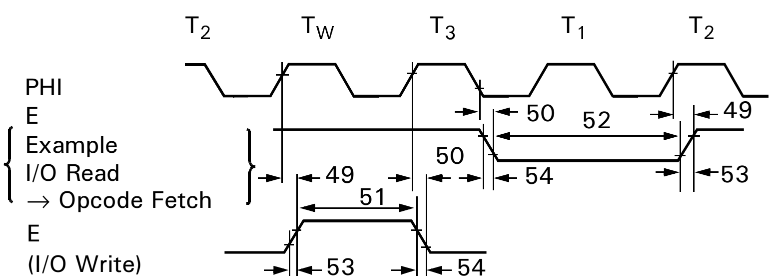

Figure 26. E Clock Timing (Minimum Timing Example of P_{WEL} and P_{WEH})

ASCI CHANNEL CONTROL REGISTER A (Continued)

vious contents of TDRE are held. TE is cleared to 0 in IOSTOP mode during RESET.

$\overline{\text{RTS0}}$: Request to Send Channel 0 (Bit 4 in CNTLA0 Only). If bit 4 of the System Configuration Register is 0, the $\overline{\text{RTS0}}$/TXS pin exhibits the $\overline{\text{RTS0}}$ function. $\overline{\text{RTS0}}$ allows the ASCI to control (start/stop) another communication devices transmission (for example, by connecting to that device's $\overline{\text{CTS}}$ input). $\overline{\text{RTS0}}$ is essentially a 1-bit output port, having no side effects on other ASCI registers or flags.

Bit 4 in CNTLA1 is used.

CKA1D = 1, CKA1/$\overline{\text{TEND0}}$ pin = $\overline{\text{TEND0}}$

CKA1D = 0, CKA1/$\overline{\text{TEND0}}$ pin = CKA1

These bits are cleared to 0 on reset.

MPBR/EFR: Multiprocessor Bit Receive/Error Flag Reset (Bit 3). When multiprocessor mode is enabled (MP in CNTLB = 1), MPBR, when read, contains the value of the MPB bit for the most recent receive operation. When written to 0, the EFR function is selected to reset all error flags (OVRN, FE, PE and BRK in the ASEXT Register) to 0. MPBR/EFR is undefined during RESET.

MOD2, 1, 0: ASCI Data Format Mode 2,1,0 (bits 2–0).

These bits program the ASCI data format as follows.

MOD2

= 0→7 bit data

= 1→8 bit data

MOD1

= 0→No parity

= 1→Parity enabled

MOD0

= 0→1 stop bit

= 1→2 stop bits

The data formats available based on all combinations of MOD2, MOD1, and MOD0 are indicated in Table 9.

Table 9. Data Formats

MOD2	MOD1	MOD0	Data Format
0	0	0	Start + 7 bit data + 1 stop
0	0	1	Start + 7 bit data + 2 stop
0	1	0	Start + 7 bit data + parity + 1 stop
0	1	1	Start + 7 bit data + parity + 2 stop
1	0	0	Start + 8 bit data + 1 stop
1	0	1	Start + 8 bit data + 2 stop
1	1	0	Start + 8 bit data + parity + 1 stop
1	1	1	Start + 8 bit data + parity + 2 stop

ASCI CHANNEL CONTROL REGISTER B

ASCI Control Register B 0 (CNTLB0: I/O Address = 02H)
ASCI Control Register B 1 (CNTLB1: I/O Address = 03H)

Bit	7	6	5	4	3	2	1	0
	MPBT	MP	$\overline{\text{CTS}}$/PS	PEO	DR	SS2	SS1	SS0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 34. ASCI Channel Control Register B

MPBT: Multiprocessor Bit Transmit (Bit 7). When multiprocessor communication format is selected (MP bit = 1), MPBT is used to specify the MPB data bit for transmission. If MPBT = 1, then MPB = 1 is transmitted. If MPBT = 0, then MPB = 0 is transmitted. The MPBT state is undefined during and after RESET.

MP: Multiprocessor Mode (Bit 6). When MP is set to 1, the data format is configured for multiprocessor mode based on MOD2 (number of data bits) and MOD0 (number of stop bits) in CNTLA. The format is as follows:

Start bit + 7 or 8 data bits + MPB bit + 1 or 2 stop bits

Multiprocessor (MP = 1) format offers no provision for parity. If MP = 0, the data format is based on MOD0, MOD1, MOD2, and may include parity. The MP bit is cleared to 0 during RESET.

$\overline{\text{CTS}}$/PS: Clear to Send/Prescale (Bit 5). When read, $\overline{\text{CTS}}$/PS reflects the state of the external $\overline{\text{CTS}}$ input. If the $\overline{\text{CTS}}$ input pin is High, $\overline{\text{CTS}}$/PS is read as 1.

Note: When the $\overline{\text{CTS}}$ input pin is High, the TDRE bit is inhibited (that is, held at 0).

For channel 1, the $\overline{\text{CTS}}$ input is multiplexed with RXS pin (Clocked Serial Receive Data). Thus, $\overline{\text{CTS}}$/PS is only valid when read if the channel 1 CTS1E bit = 1 and the $\overline{\text{CTS}}$ input pin function is selected. The READ data of $\overline{\text{CTS}}$/PS is not affected by $\overline{\text{RESET}}$.

If the SS2–0 bits in this register are not 111, and the BRG mode bit in the ASEXT register is 0, then writing to this bit sets the prescale (PS) control. Under those circumstances, a 0 indicates a divide-by-10 prescale function while a 1 indicates divide-by-30. The bit resets to 0.

PEO: Parity Even Odd (Bit 4) . PEO selects oven or odd parity. PEO does not affect the enabling/disabling of parity (MOD1 bit of CNTLA). If PEO is cleared to 0, even parity is selected. If PEO is set to 1, odd parity is selected. PEO is cleared to 0 during RESET.

DR: Divide Ratio (Bit 3). If the X1 bit in the ASEXT register is 0, this bit specifies the divider used to obtain baud rate from the data sampling clock. If DR is reset to 0, divide-by-16 is used, while if DR is set to 1, divide-by-64 is used. DR is cleared to 0 during RESET.

SS2,1,0: Source/Speed Select 2,1,0 (Bits 2–0). First, if these bits are 111, as they are after a RESET, the CKA pin is used as a clock input, and is divided by 1, 16, or 64 depending on the DR bit and the X1 bit in the ASEXT register.

If these bits are not 111 and the BRG mode bit is ASEXT is 0, then these bits specify a power-of-two divider for the PHI clock as indicated in Table 10.

Setting or leaving these bits as 111 makes sense for a channel only when its CKA pin is selected for the CKA function. CKAO/CKS offers the CKAO function when bit 4 of the System Configuration Register is 0. $\overline{\text{DCD0}}$/CKA1 offers the CKA1 function when bit 0 of the Interrupt Edge register is 1.

Table 10. Divide Ratio

SS2	SS1	SS0	Divide Ratio
0	0	0	÷1
0	0	1	÷2
0	1	0	÷4
0	1	1	÷8
1	0	0	÷16
1	0	1	÷32
1	1	0	÷64
1	1	1	External Clock

never both set to 1 at the same time. TE is cleared to 0 during RESET and IOSTOP mode.

SS2, 1, 0: Speed Select 2, 1, 0 (Bits 2–0). SS2, SS1 and SS0 select the CSI/O transmit/receive clock source and speed. SS2, SS1 and SS0 are all set to 1 during $\overline{\text{RESET}}$. Table 11 indicates CSI/O Baud Rate Selection.

Table 11. CSI/O Baud Rate Selection

SS2	SS1	SS0	Divide Ratio
0	0	0	÷20
0	0	1	÷40
0	1	0	÷80
0	1	1	÷160
1	0	0	÷320
1	0	1	÷640
1	1	0	÷1280
1	1	1	External Clock Input (Less Than ÷20)

After $\overline{\text{RESET}}$, the CKS pin is configured as an external clock input (SS2, SS1, SS0 = 1). Changing these values causes CKS to become an output pin and the selected clock is output when transmit or receive operations are enabled.

CSI/O Transmit/Receive Data Register

Mnemonic TRDR
Address 0BH

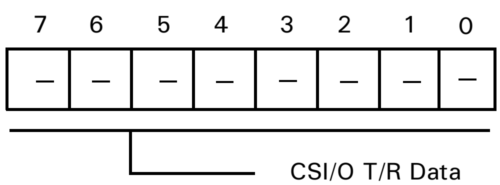

Figure 41. CSI/O Transmit/Receive Data Register

Timer Data Register Channel 0 Low

Mnemonic TMDR0L
Address 0CH

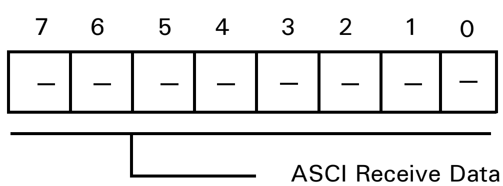

Figure 42. Timer Register Channel 0 Low

Timer Data Register Channel 0H

Mnemonic TMDR0H
Address 0DH

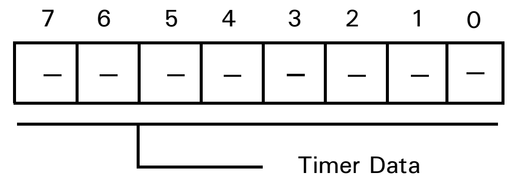

Figure 43. Timer Data Register Channel 0 High

Timer Reload Register Channel 0 Low

Mnemonic RLDR0L
Address 0EH

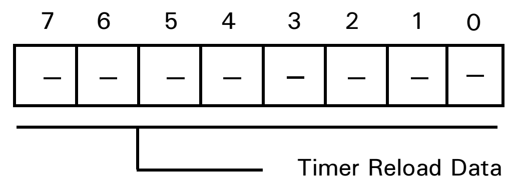

Figure 44. Timer Reload Register Low

Timer Reload Register Channel 0 High

Mnemonic RLDR0H
Address 0FH

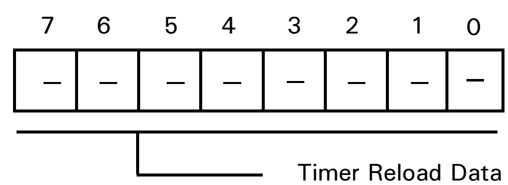

Figure 45. Timer Reload Register Channel 0 High

ASCI EXTENSION CONTROL REGISTER CHANNEL 0 AND CHANNEL 1 (Continued)

Timer Data Register Channel 1 Low

Mnemonic TMDR1L
Address 14H

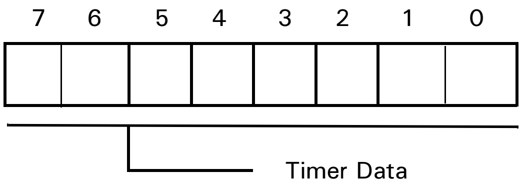

Figure 48. Timer Data Register 1 Low

Timer Data Register Channel 1 High

Mnemonic TMDR1H
Address 15H

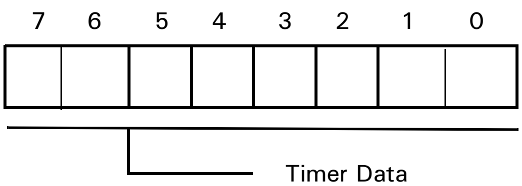

Figure 49. Timer Data Register 1 High

Timer Reload Register Channel 1 Low

Mnemonic RLDR1L
Address 16

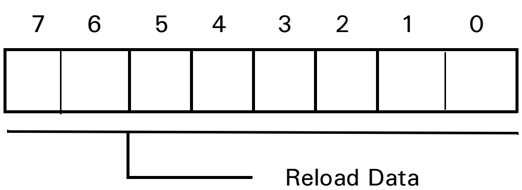

Figure 50. Timer Reload Channel 1 Low

Timer Reload Register Channel 1 High

Mnemonic RLDR1H
Address 17H

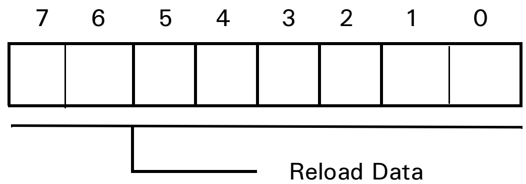

Figure 51. Timer Reload Register Channel 1 High

Free Running Counter (Read Only)

Mnemonic FRC
Address 18H

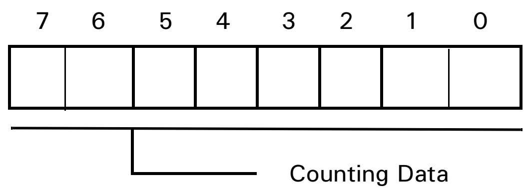

Figure 52. Free Running Counter

DMA DESTINATION ADDRESS REGISTER CHANNEL 0

The DMA Destination Address Register Channel 0 specifies the physical destination address for channel 0 transfers. The register contains 20 bits and can specify up to 1024-KB memory addresses or up to 64-KB I/O addresses. Channel 0 destination can be memory, I/O, or memory mapped I/O. For I/O, the MS bits of this register identify the Request Handshake signal for channel 0.

DMA Destination Address Register Channel 0 Low

Mnemonic DAR0L
Address 23H

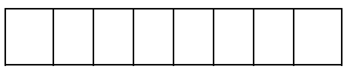

Figure 58. DMA Destination Address Register Channel 0 Low

DMA Destination Address Register Channel 0 High

Mnemonic DAR0H
Address 24H

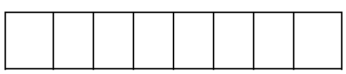

Figure 59. DMA Destination Address Register Channel 0 High

DMA Destination Address Register Channel 0B

Mnemonic DAR0B
Address 25H

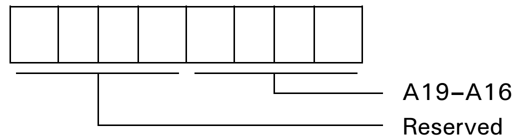

Figure 60. DMA Destination Address Register Channel 0B

If the DMA destination is in I/O space, bits 1–0 of this register select the DMA request signal for DMA0, as follows:

Bit 1 (A17)	Bit 0 (A16)	DMA Transfer Request
0	0	DREQ0 (external)
0	1	TDR0 (ASCI0)
1	0	TDR1 (ASCI1)
1	1	Not Used

DMA MODE REGISTER

The DMA Mode Register (DMODE) is used to set the addressing and transfer mode for channel 0.

DMA Mode Register

Mnemonic DMODE
Address 31H

Bit	7	6	5	4	3	2	1	0
	—	—	DM1	DM0	SM1	SM0	MMOD	—
			R/W	R/W	R/W	R/W	R/W	

Figure 72. DMA Mode Register (DMODE: I/O Address = 31H)

DM1, DM0: Destination Mode Channel 0 (Bits 5,4). This mode specifies whether the destination for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred. DM1 and DM0 are cleared to 0 during RESET.

Table 14. Channel 0 Destination

DM1	DM0	Memory I/O	Memory Increment/Decrement
0	0	Memory	+1
0	1	Memory	–1
1	0	Memory	fixed
1	1	I/O	fixed

SM1, SM0: Source Mode Channel 0 (Bits 3, 2) . This mode specifies whether the source for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred.

Table 15. Channel 0 Source

SM1	SM0	Memory I/O	Memory Increment/Decrement
0	0	Memory	+1
0	1	Memory	–1
1	0	Memory	fixed
1	1	I/O	fixed

Table 16 indicates all DMA transfer mode combinations of DM0, DM1, SM0, and SM1. Because I/O to/from I/O transfers are not implemented, 12 combinations are available.

Table 16. Transfer Mode Combinations

DM1	DM0	SM1	SM0	Transfer Mode	Address Increment/Decrement
0	0	0	0	Memory→Memory	SAR0 + 1, DAR0 + 1
0	0	0	1	Memory→Memory	SAR0−1, DAR0 + 1
0	0	1	0	Memory*→Memory	SAR0 fixed, DAR0 + 1
0	0	1	1	I/O→Memory	SAR0 fixed, DAR0 + 1
0	1	0	0	Memory→Memory	SAR0 + 1, DAR0−1
0	1	0	1	Memory→Memory	SAR0−1, DAR0−1
0	1	1	0	Memory*→Memory	SAR0 fixed, DAR0−1
0	1	1	1	I/O→Memory	SAR0 fixed, DAR0−1
1	0	0	0	Memory→Memory*	SAR0 + 1, DAR0 fixed
1	0	0	1	Memory→Memory*	SAR0−1, DAR0 fixed
1	0	1	0	Reserved	
1	0	1	1	Reserved	
1	1	0	0	Memory→I/O	SAR0 + 1, DAR0 fixed
1	1	0	1	Memory→I/O	SAR0−1, DAR0 fixed
1	1	1	0	Reserved	
1	1	1	1	Reserved	

Note: * Includes memory mapped I/O.

MMOD: Memory Mode Channel 0 (Bit 1). When channel 0 is configured for memory to/from memory transfers there is no Request Handshake signal to control the transfer timing. Instead, two automatic transfer timing modes are selectable: burst (MMOD = 1) and cycle steal (MMOD = 0). For burst memory to/from memory transfers, the DMAC takes control of the bus continuously until the DMA transfer completes (as indicated by the byte count register = 0). In cycle steal mode, the CPU is provided a cycle for each DMA byte transfer cycle until the transfer is completed.

For channel 0 DMA with I/O source or destination, the selected Request signal times the transfer ignoring MMOD. MMOD is cleared to 0 during RESET.

DMA/WAIT CONTROL REGISTER

The DMA/WAIT Control Register (DCNTL) controls the insertion of wait states into DMAC (and CPU) accesses of memory or I/O. Also, the register defines the Request signal for each channel as level or edge sense. DCNTL also sets the DMA transfer mode for channel 1, which is limited to memory to/from I/O transfers.

Bit	7	6	5	4	3	2	1	0
	MWI1	MWI0	IWI1	IWI0	DMS1	DMS0	DIM1	DIM0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 73. DMA/WAIT Control Register (DCNTL: I/O Address = 32H)

MWI1, MWI0: Memory Wait Insertion (Bits 7–6). This bit specifies the number of wait states introduced into CPU or DMAC memory access cycles. MWI1 and MWI0 are set to 1 during RESET.

MWI1	MWI0	Wait State
0	0	0
0	1	1
1	0	2
1	1	3

IWI1, IWI0: I/O Wait Insertion (Bits 5–4). This bit specifies the number of wait states introduced into CPU or DMAC I/O access cycles. IWI1 and IWI0 are set to 1 during RESET.

IWI1	IWI0	Wait State
0	0	1
0	1	2
1	0	3
1	1	4

Note: These wait states are added to the 3-clock I/O cycle that is used to access the on-chip I/O registers. It is equally valid to regard these as 0 to 3 wait states added to a 4-clock external I/O cycle.

DMS1, DMS0: DMA Request Sense (Bits 3–2). DMS1 and DMS0 specify the DMA request sense for channel 0 and channel 1 respectively. When reset to 0, the input is level sense. When set to 1, the input is edge sense. DMS1 and DMS0 are cleared to 0 during RESET.

DMSi	Sense
1	Edge Sense
0	Level Sense

Typically, for an input/source device, the associated DMS bit should be programmed as 0 for level sense. The device takes a relatively long time to update its Request signal after the DMA channel reads data (in the first of the two machine cycles involved in transferring a byte).

An output/destination device takes much less time to update its Request signal after the DMA channel starts a WRITE operation to it (the second machine cycle of the two cycles involved in transferring a byte). With zero-wait state I/O cycles, a device cannot update its request signal in the required time, so edge sensing must be used.

A one-wait-state I/O cycle also does not provide sufficient time for updating, so edge sensing is again required.

DIM1, DIM0: DMA Channel 1 I/O and Memory Mode (Bits 1–0). Specifies the source/destination and address modifier for channel 1 memory to/from I/O transfer modes. DIM1 and DIM0 are cleared to 0 during RESET.

Table 17. Channel 1 Transfer Mode

DIM1	DMI0	Transfer Mode	Address Increment/Decrement
0	0	Memory→I/O	MAR1 +1, IAR1 fixed
0	1	Memory→I/O	MAR1 –1, IAR1 fixed
1	0	I/O→Memory	IAR1 fixed, MAR1 +1
1	1	I/O→Memory	IAR1 fixed, MAR1 –1

INTERRUPT VECTOR LOW REGISTER

Bits 7–5 of the Interrupt Vector Low Register (I_L) are used as bits 7–5 of the synthesized interrupt vector during interrupts for the $\overline{INT1}$ and $\overline{INT2}$ pins and for the DMAs, ASCIs, PRTs, and CSI/O. These three bits are cleared to 0 during RESET (Figure 74).

Interrupt Vector Low Register

Mnemonic: IL
Address 33H

Bit	7	6	5	4	3	2	1	0
	IL 7	IL 6	IL 5	––	––	––	––	––
	R/W	R/W	R/W					
	Programmable			Interrupt Source Dependent Code				

Figure 74. Interrupt Vector Low Register (IL: I/O Address = 33H)

INT/TRAP CONTROL REGISTER

This register is used in handling TRAP interrupts and to enable or disable Maskable Interrupt Level 0 and the $\overline{INT1}$ and $\overline{INT2}$ pins.

INT/TRAP Control Register

Mnemonics ITC
Address 34H

Bit	7	6	5	4	3	2	1	0
	TRAP	UFO	––	––	––	ITE2	ITE1	ITE0
	R/W	R				R/W	R/W	R/W

TRAP (Bit 7). This bit is set to 1 when an undefined opcode is fetched. TRAP can be reset under program control by writing it with a 0; however, TRAP cannot be written with 1 under program control. TRAP is reset to 0 during RESET.

UFO: Undefined Fetch Object (Bit 6). When a TRAP interrupt occurs, the contents of UFO allow the starting address of the undefined instruction to be determined. This interrupt is necessary because the TRAP may occur on either the second or third byte of the opcode. UFO allows the stacked PC value to be correctly adjusted. If UFO = 0, the first opcode should be interpreted as the stacked PC-1. If UFO = 1, the first opcode address is stacked PC-2. UFO is Read-Only.

ITE2, 1, 0: Interrupt Enable 2, 1, 0 (Bits 2–0). ITE2 and ITE1 enable and disable the external interrupt inputs $\overline{INT2}$ and $\overline{INT1}$, respectively. ITE0 enables and disables interrupts from:

- ESCC
- CTCs
- Bidirectional Centronics controller
- External interrupt input $\overline{INT0}$

A 1 in a bit enables the corresponding interrupt level while a 0 disables it. A RESET sets ITE0 to 1 and clears ITE1 and ITE2 to 0.

TRAP Interrupt. The Z8S180/Z8L180 generates a TRAP sequence when an undefined opcode fetch occurs. This feature can be used to increase software reliability, implement an *extended* instruction set, or both. TRAP may occur during opcode fetch cycles and also if an undefined opcode is fetched during the interrupt acknowledge cycle for $\overline{INT0}$ when Mode 0 is used.

When a TRAP sequence occurs, the Z8S180/Z8L180:

1. Sets the TRAP bit in the Interrupt TRAP/Control (ITC) register to 1.
2. Saves the current Program Counter (PC) value, reflecting the location of the undefined opcode, on the stack.
3. Resumes execution at logical address 0.

Note: If logical address 0000H is mapped to physical address 00000H, the vector is the same as for RESET. In this case, testing the TRAP bit in ITC reveals whether the restart at physical address 00000H was caused by RESET or TRAP.

REFRESH CONTROL REGISTER

Mnemonic RCR
Address 36H

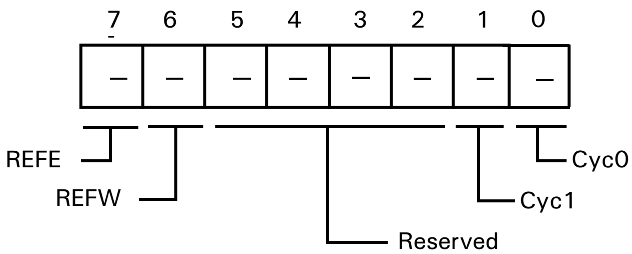

Figure 77. Refresh Control Register (RCR: I/O Address = 36H)

The Refresh Control Register (RCR) specifies the interval and length of refresh cycles, while enabling or disabling the refresh function.

REFE: Refresh Enable (Bit 7). REFE = 0 disables the refresh controller, while REFE = 1 enables refresh cycle insertion. REFE is set to 1 during RESET.

REFW: Refresh Wait (Bit 6). REFW = 0 causes the refresh cycle to be two clocks in duration. REFW = 1 causes the refresh cycle to be three clocks in duration by adding a refresh wait cycle (TRW). REFW is set to 1 during RESET.

CYC1, 0: Cycle Interval (Bit 1,0). CYC1 and CYC0 specify the interval (in clock cycles) between refresh cycles. When dynamic RAM requires 128 refresh cycles every 2 ms (or 256 cycles in every 4 ms), the required refresh interval is less than or equal to 15.625 µs. Thus, the underlined values indicate the best refresh interval depending on CPU clock frequency. CYC0 and CYC1 are cleared to 0 during RESET (see Table 18).

Table 18. DRAM Refresh Intervals

			Time Interval				
CYC1	**CYC0**	**Insertion Interval**	**PHI: 10 MHz**	**8 MHz**	**6 MHz**	**4 MHz**	**2.5 MHz**
0	0	10 states	(1.0 µs)*	(1.25 µs)*	1.66 µs	2.5 µs	4.0 µs
0	1	20 states	(2.0 µs)*	(2.5 µs)*	3.3 µs	5.0 µs	8.0 µs
1	0	40 states	(4.0 µs)*	(5.0 µs)*	6.6 µs	10.0 µs	16.0 µs
1	1	80 states	(8.0 µs)*	(10.0 µs)*	13.3 µs	20.0 µs	32.0 µs

Note: *calculated interval.

Refresh Control and Reset. After RESET, based on the initialized value of RCR, refresh cycles occur with an interval of 10 clock cycles and be 3 clock cycles in duration.

Dynamic RAM Refresh Operation

1. Refresh Cycle insertion is stopped when the CPU is in the following states:
   a. During RESET
   b. When the bus is released in response to $\overline{\text{BUSREQ}}$
   c. During SLEEP mode
   d. During $\overline{\text{WAIT}}$ states
2. Refresh cycles are suppressed when the bus is released in response to $\overline{\text{BUSREQ}}$. However, the refresh timer continues to operate. The time at which the first refresh cycle occurs after the Z8S180/Z8L180 reacquires the bus depends on the refresh timer. This cycle offers no timing relationship with the bus exchange.
3. Refresh cycles are suppressed during SLEEP mode. If a refresh cycle is requested during SLEEP mode, the refresh cycle request is internally latched (until replaced with the next refresh request). The latched refresh cycle is inserted at the end of the first machine cycle after SLEEP mode is exited. After this initial cycle, the time at which the next refresh cycle occurs depends on the refresh time and offers no relationship with the exit from SLEEP mode.
4. The refresh address is incremented by one for each successful refresh cycle, not for each refresh. Thus, independent of the number of missed refresh requests, each refresh bus cycle uses a refresh address incremented by one from that of the previous refresh bus cycles.