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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	64-DIP (0.750", 19.05mm)
Supplier Device Package	64-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8s18010psc

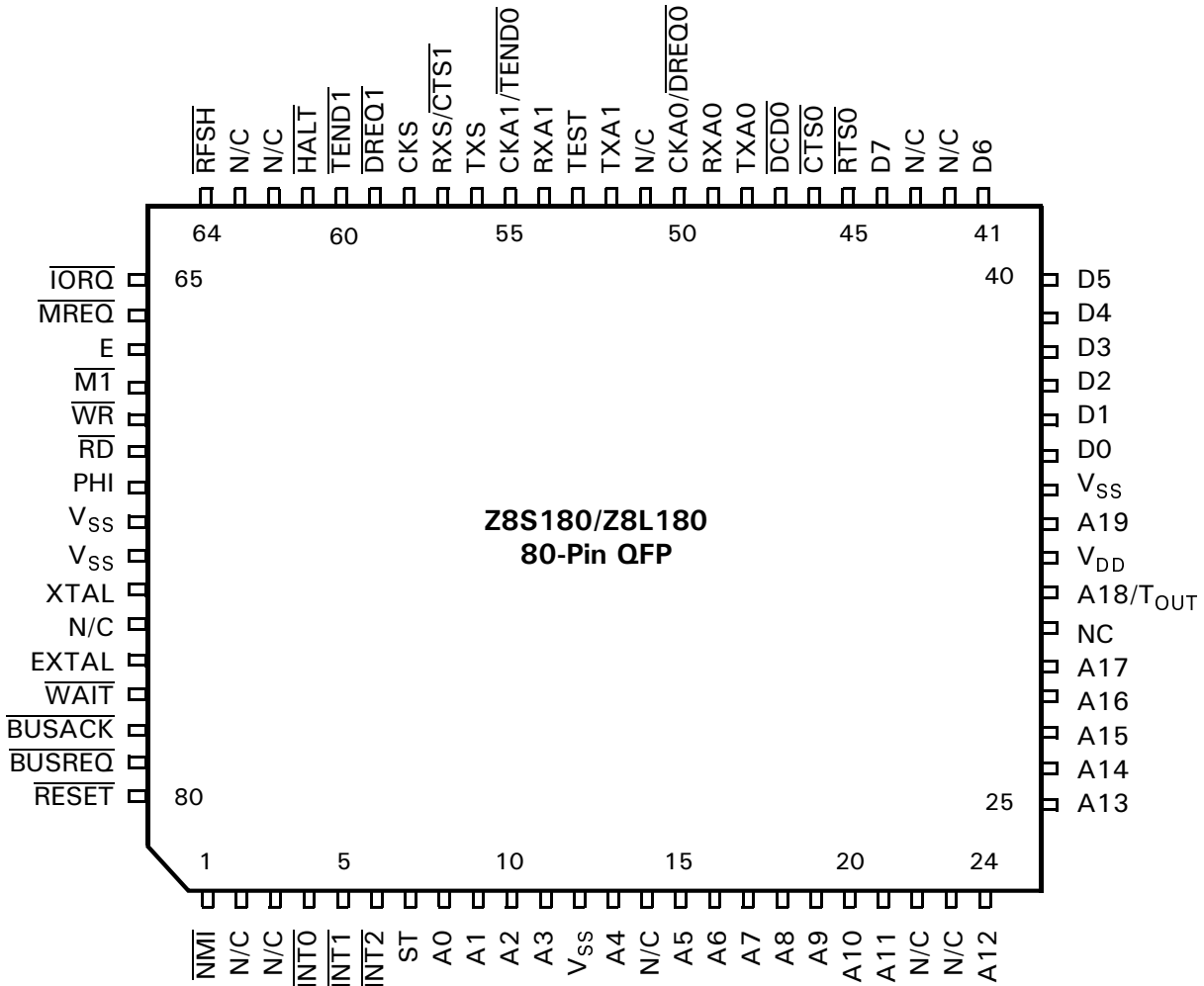


Figure 4. Z8S180/Z8L180 80-Pin QFP Pin Configuration

Table 1. Z8S180/Z8L180 Pin Identification

Pin Number and Package Type			Default Function	Secondary Function	Control
QFP	PLCC	DIP			
1	9	8	$\overline{\text{NMI}}$		
2			NC		
3			NC		
4	10	9	$\overline{\text{INT0}}$		
5	11	10	$\overline{\text{INT1}}$		
6	12	11	$\overline{\text{INT2}}$		
7	13	12	ST		
8	14	13	A0		
9	15	14	A1		
10	16	15	A2		
11	17	16	A3		
12	18		V _{SS}		

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)

Pin Number and Package Type			Pin Status				
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
39	41	38	D4		3T	3T	3T
40	42	39	D5		3T	3T	3T
41	43	40	D6		3T	3T	3T
42			NC				
43			NC				
44	44	41	D7		3T	3T	3T
45	45	42	$\overline{\text{RTS0}}$		High	OUT	High
46	46	43	$\overline{\text{CTS0}}$		IN	OUT	IN
47	47	44	$\overline{\text{DCD0}}$		IN	IN	IN
48	48	45	TXA0		High	OUT	OUT
49	49	46	RXA0		IN	IN	IN
50	50	47	CKA0		3T	I/O	I/O
			$\overline{\text{DREQ0}}$		N/A	IN	IN
51			NC				
52	51	48	TXA1		High	OUT	OUT
53	52		TEST				
54	53	49	RXA1		IN	IN	IN
55	54	50	CKA1		3T	I/O	I/O
			$\overline{\text{TEND0}}$		N/A	High	High
56	55	51	TXS		High	OUT	OUT
57	56	52	RXS		IN	IN	IN
			$\overline{\text{CTS1}}$		N/A	IN	IN
58	57	53	CKS		3T	I/O	I/O
59	58	54	$\overline{\text{DREQ1}}$		IN	3T	IN
60	59	55	$\overline{\text{TEND1}}$		High	OUT	High
61	60	56	$\overline{\text{HALT}}$		High	High	Low
62			NC				
63			NC				
64	61	57	$\overline{\text{RFSH}}$		High	OUT	High
65	62	58	$\overline{\text{IORQ}}$		High	3T	High
66	63	59	$\overline{\text{MREQ}}$		High	3T	High
67	64	60	E		Low	OUT	OUT
68	65	61	$\overline{\text{M1}}$		High	High	High
69	66	62	$\overline{\text{WR}}$		High	3T	High
70	67	63	$\overline{\text{RD}}$		High	3T	High
71	68	64	PHI		OUT	OUT	OUT
72	1	1	V _{SS}		GND	GND	GND
73	2		V _{SS}		GND	GND	GND
74	3	2	XTAL		OUT	OUT	OUT
75			NC				

PIN IDENTIFICATION (Continued)

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
76	4	3	EXTAL		IN	IN	IN
77	5	4	$\overline{\text{WAIT}}$		IN	IN	IN
78	6	5	$\overline{\text{BUSACK}}$		High	OUT	OUT
79	7	6	$\overline{\text{BUSREQ}}$		IN	IN	IN
80	8	7	$\overline{\text{RESET}}$		IN	IN	IN

OPERATION MODES (Continued)

The Z8S180/Z8L180 leaves HALT mode in response to:

- Low on $\overline{\text{RESET}}$
- Interrupt from an enabled on-chip source
- External request on $\overline{\text{NMI}}$
- Enabled external request on $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, or $\overline{\text{INT2}}$

In case of an interrupt, the return address is the instruction following the HALT instruction. The program can either branch back to the HALT instruction to wait for another interrupt or can examine the new state of the system/application and respond appropriately.

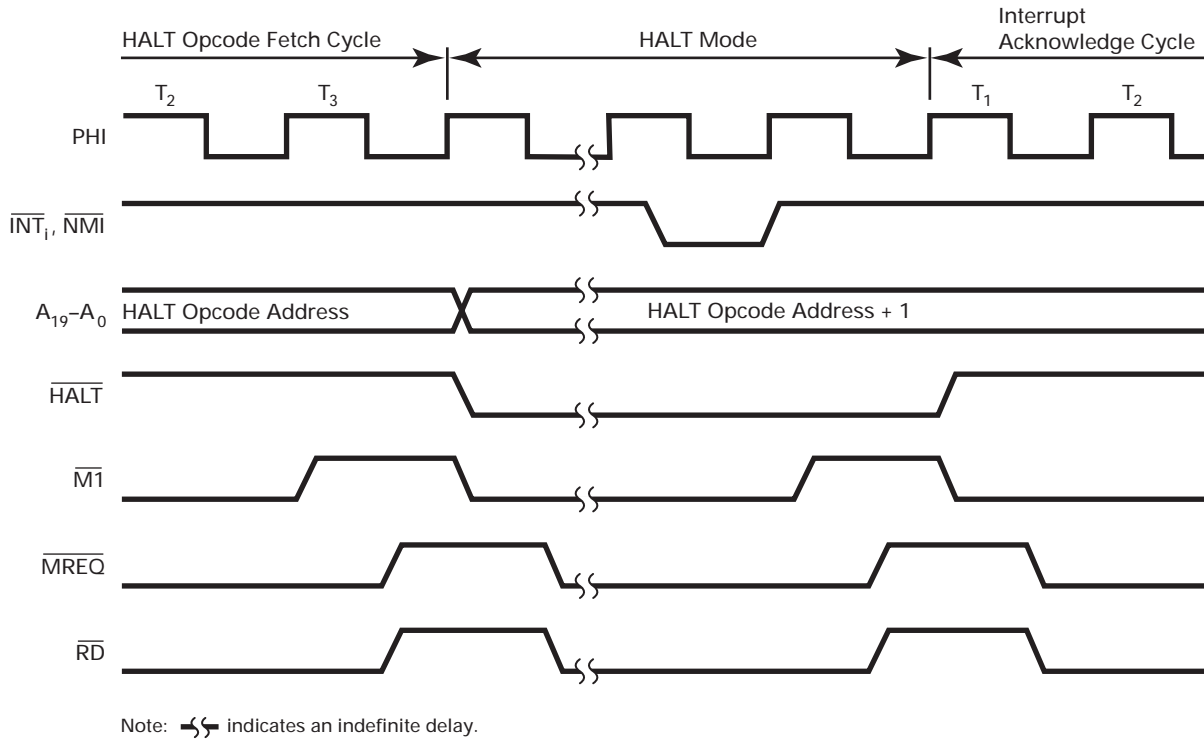


Figure 13. HALT Timing

SLEEP Mode. This mode is entered by keeping the IOSTOP bit (ICR5) and bits 3 and 6 of the CPU Control Register (CCR3, CCR6) all zero and executing the SLP instruction. The oscillator and PHI output continue operating, but are blocked from the CPU core and DMA channels to reduce power consumption. DRAM refresh stops, but interrupts and granting to an external Master can occur. Except when the bus is granted to an external Master, A19-0 and all control signals except $\overline{\text{HALT}}$ are maintained High. $\overline{\text{HALT}}$ is Low. I/O operations continue as before the SLP instruction, except for the DMA channels.

The Z8S180/Z8L180 leaves SLEEP mode in response to a Low on $\overline{\text{RESET}}$, an interrupt request from an on-chip source,

an external request on $\overline{\text{NMI}}$, or an external request on $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, or $\overline{\text{INT2}}$.

If an interrupt source is individually disabled, it cannot bring the Z8S180/Z8L180 out of SLEEP mode. If an interrupt source is individually enabled, and the IEF bit is 1 so that interrupts are globally enabled (by an EI instruction), the highest priority active interrupt occurs with the return address being the instruction after the SLP instruction. If an interrupt source is individually enabled, but the IEF bit is 0 so that interrupts are globally disabled (by a DI instruction), the Z8S180/Z8L180 leaves SLEEP mode by simply executing the following instruction(s).

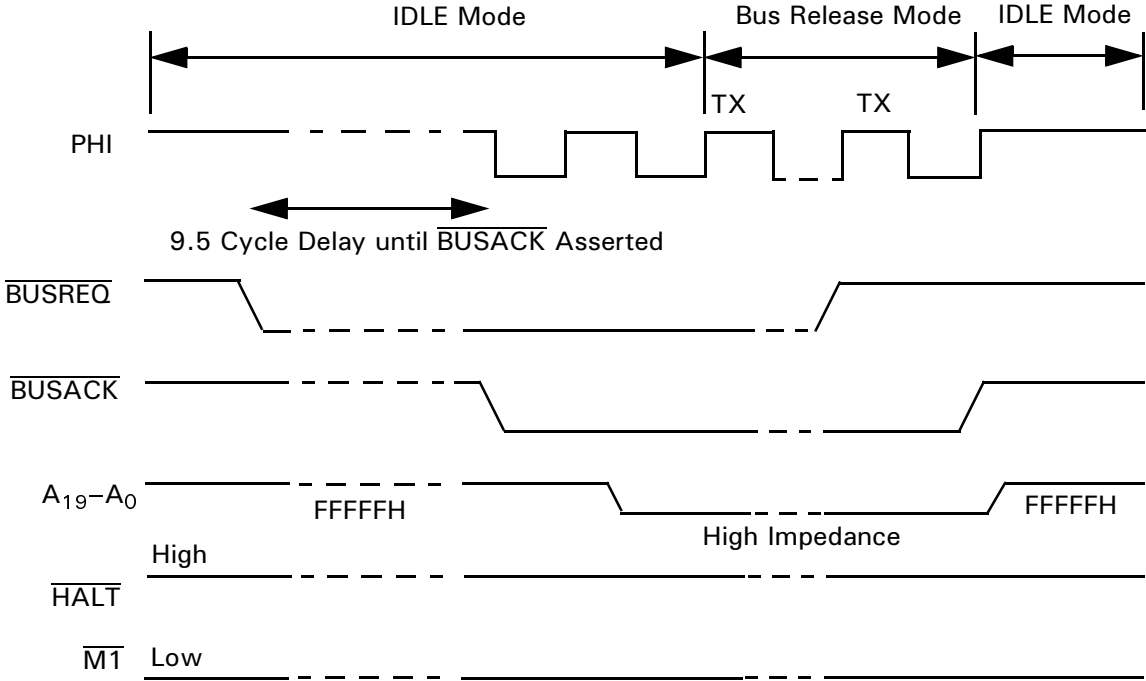


Figure 16. Bus Granting to External Master in IDLE Mode

STANDBY Mode (With or Without QUICK RECOVERY).

Software can put the Z8S180/Z8L180 into this mode by setting the IOSTOP bit (ICR5) to 1, CCR6 to 1, and executing the SLP instruction. This mode stops the on-chip oscillator and thus draws the least power of any mode, less than 10µA.

As with IDLE mode, the Z8S180/Z8L180 leaves STANDBY mode in response to a Low on $\overline{\text{RESET}}$, on $\overline{\text{NMI}}$, or a Low on $\overline{\text{INT0-2}}$ that is enabled by a 1 in the corresponding bit in the INT/TRAP Control Register. This action grants the bus to an external Master if the BREXT bit in the CPU Control Register (CCR5) is 1. The time required for all of these operations is greatly increased by the necessity for restarting the on-chip oscillator, and ensuring that it stabilizes to square-wave operation.

When an external clock is connected to the EXTAL pin rather than a crystal to the XTAL and EXTAL pins and the external clock runs continuously, there is little necessity to use STANDBY mode because no time is required to restart the oscillator, and other modes restart faster. However, if external logic stops the clock during STANDBY mode (for example, by decoding $\overline{\text{HALT}}$ Low and $\overline{\text{M1}}$ High for several clock cycles), then STANDBY mode can be useful to allow the external clock source to stabilize after it is re-enabled.

When external logic drives $\overline{\text{RESET}}$ Low to bring the device out of STANDBY mode, and a crystal is in use or an external clock source is stopped, the external logic must hold $\overline{\text{RESET}}$ Low until the on-chip oscillator or external clock source is restarted and stabilized.

The clock-stability requirements of the Z8S180/Z8L180 are much less in the divide-by-two mode that is selected by a RESET sequence and controlled by the Clock Divide bit in the CPU Control Register (CCR7). As a result, software performs the following actions:

1. Sets CCR7 to 0 for divide-by-two mode before an SLP instruction and STANDBY mode.
2. Delays setting CCR7 back to 1 for divide-by-one mode as long as possible to allow additional clock stabilization time after a RESET, interrupt, or in-line RESTART after an SLP 01 instruction.

If CCR6 is set to 1 before the SLP instruction places the MPU in STANDBY mode, the value of the CCR3 bit determines the length of the delay before the oscillator restarts and stabilizes when it leaves STANDBY mode due to an external interrupt request. When CCR3 is 0, the Z8S180/Z8L180 waits 2^{17} (131,072) clock cycles. When CCR3 is 1, it waits 64 clock cycles. This state is called QUICK RECOVERY mode. The same delay applies to grant-

ing the bus to an external Master during STANDBY mode, when the BREXT bit in the CPU Control Register (CCR5) is 1.

As described previously for SLEEP and IDLE modes, when the MPU leaves STANDBY mode due to $\overline{\text{NMI}}$ Low or an enabled $\overline{\text{INT0}}\text{--}\overline{\text{INT2}}$ Low when the IEF, flag is 1 due to an IE instruction, it starts by performing the interrupt with the return address being that of the instruction following the SLP instruction. If the Z8S180/Z8L180 leaves STANDBY mode due to an external interrupt request that's enabled in the INT/TRAP Control Register, but the IEF, bit is 0 due to

a DI instruction, the processor restarts by executing the instruction(s) following the SLP instruction. If $\overline{\text{INT0}}$, or $\overline{\text{INT1}}$ or $\overline{\text{INT2}}$ goes inactive before the end of the clock stabilization delay, the Z8S180/Z8L180 stays in STANDBY mode.

Figure 17 indicates the timing for leaving STANDBY mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes either 64 or 2^{17} (131,072) clocks to restart, depending on the CCR3 bit.

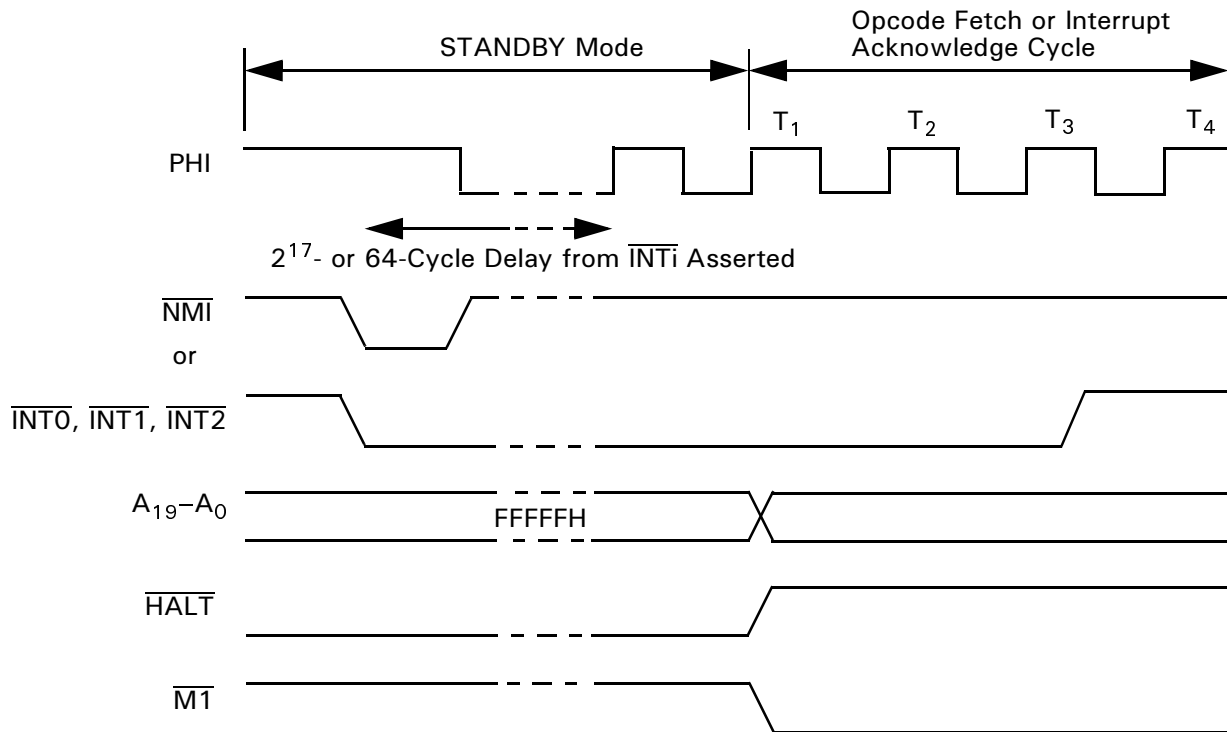


Figure 17. Z8S180/Z8L180 STANDBY Mode Exit Due to External Interrupt

While the Z8S180/Z8L180 is in STANDBY mode, it grants the bus to an external Master if the BREXT bit (CCR5) is 1. Figure 18 indicates the timing of this sequence. The device takes 64 or 2^{17} (131,072) clock cycles to grant the bus de-

pending on the CCR3 bit. The latter (not the QUICK RECOVERY) case may be prohibitive for many demand-driven external Masters. If so, QUICK RECOVERY or IDLE mode can be used.

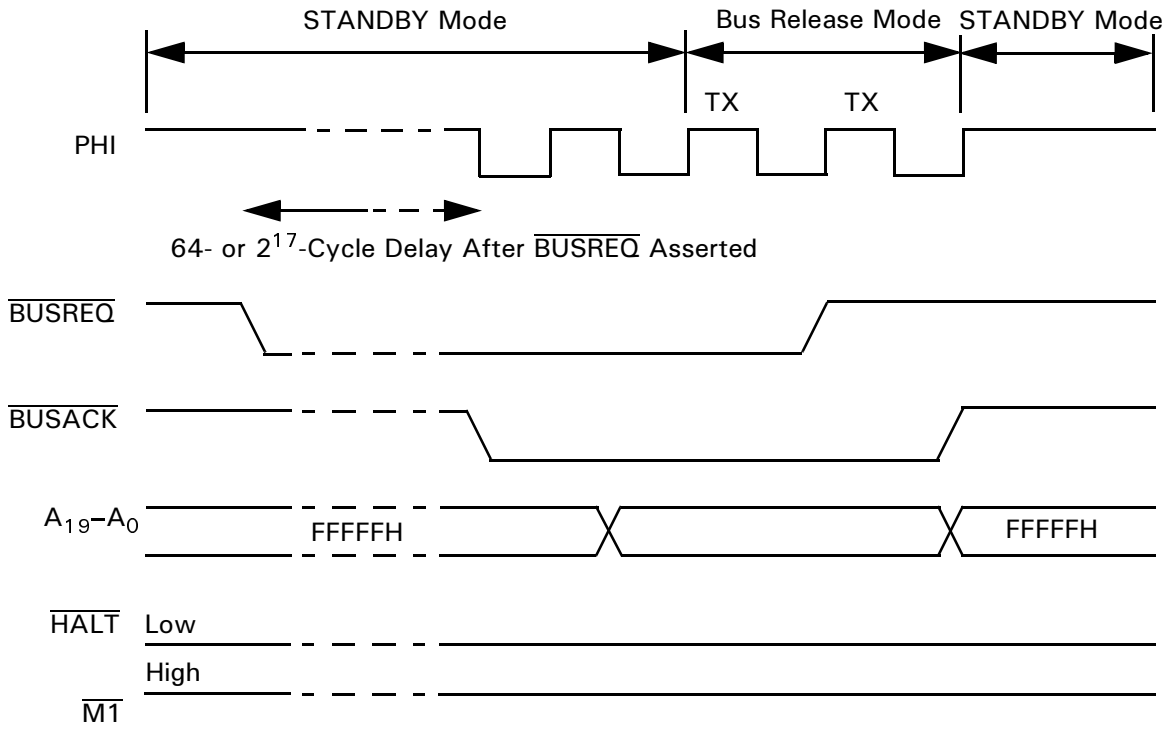


Figure 18. Bus Granting to External Master During STANDBY Mode

DC CHARACTERISTICS—Z8S180

Table 6. Z8S180 DC Characteristics
 $V_{DD} = 5V \pm 10\%$; $V_{SS} = 0V$

Symbol	Item	Condition	Min	Typ	Max	Unit
V_{IH1}	Input H Voltage \overline{RESET} , EXTAL, \overline{NMI}		$V_{DD} - 0.6$	—	$V_{DD} + 0.3$	V
V_{IH2}	Input H Voltage Except \overline{RESET} , EXTAL, \overline{NMI}		2.0	—	$V_{DD} + 0.3$	V
V_{IH3}	Input H Voltage CKS, CKA0, CKA1		2.4	—	$V_{DD} + 0.3$	V
V_{IL1}	Input L Voltage RESET, EXTAL, NMI		-0.3	—	0.6	V
V_{IL2}	Input L Voltage Except RESET, EXTAL, NMI		-0.3	—	0.8	V
V_{OH}	Outputs H Voltage All outputs	$I_{OH} = -200 \mu A$	2.4	—	—	V
		$I_{OH} = -20 \mu A$	$V_{DD} - 1.2$	—	—	
V_{OL}	Outputs L Voltage All outputs	$I_{OL} = 2.2 \text{ mA}$	—	—	0.45	V
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL	$V_{IN} = 0.5 \sim V_{DD} - 0.5$	—	—	1.0	μA
I_{TL}	Three State Leakage Current	$V_{IN} = 0.5 \sim V_{DD} - 0.5$	—	—	1.0	μA
I_{DD}^1	Power Dissipation (Normal Operation)	F = 10 MHz	—	25	60	mA
		20	—	30	50	
		33	—	60	100	
	Power Dissipation (SYSTEM STOP mode)	F = 10 MHz	—	2	5	
		20	—	3	6	
		33	—	5	9	
C_p	Pin Capacitance	$V_{IN} = 0V$, $f = 1 \text{ MHz}$ $T_A = 25^\circ C$	—	—	12	pF

Note:

1. $V_{IHmin} = V_{DD} - 1.0V$, $V_{ILmax} = 0.8V$ (All output terminals are at NO LOAD.) $V_{DD} = 5.0V$.

Table 8. Z8S180 AC Characteristics (Continued)
 $V_{DD} = 5V \pm 10\%$ or $V_{DD} = 3.3V \pm 10\%$; 33-MHz Characteristics Apply Only to 5V Operation

Number	Symbol	Item	Z8S180—20 MHz		Z8S180—33 MHz		Unit
			Min	Max	Min	Max	
63	t_{REH}	$\overline{\text{RESET}}$ Hold Time from PHI Fall	25	—	15	—	ns
64	t_{OSC}	Oscillator Stabilization Time	—	20	—	20	ns
65	t_{EXR}	External Clock Rise Time (EXTAL)	—	5	—	5	ns
66	t_{EXF}	External Clock Fall Time (EXTAL)	—	5	—	5	ns
67	t_{RR}	$\overline{\text{RESET}}$ Rise Time	—	50	—	50	ms
68	t_{RF}	$\overline{\text{RESET}}$ Fall Time	—	50	—	50	ms
69	t_{IR}	Input Rise Time (except EXTAL, $\overline{\text{RESET}}$)	—	50	—	50	ns
70	t_{IF}	Input Fall Time (except EXTAL, $\overline{\text{RESET}}$)	—	50	—	50	ns

TIMING DIAGRAMS (Continued)

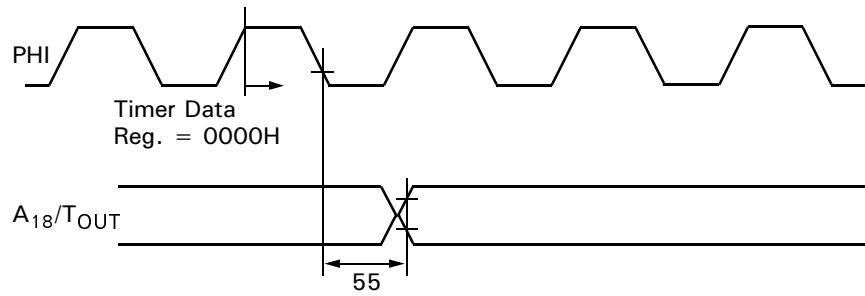


Figure 27. Timer Output Timing

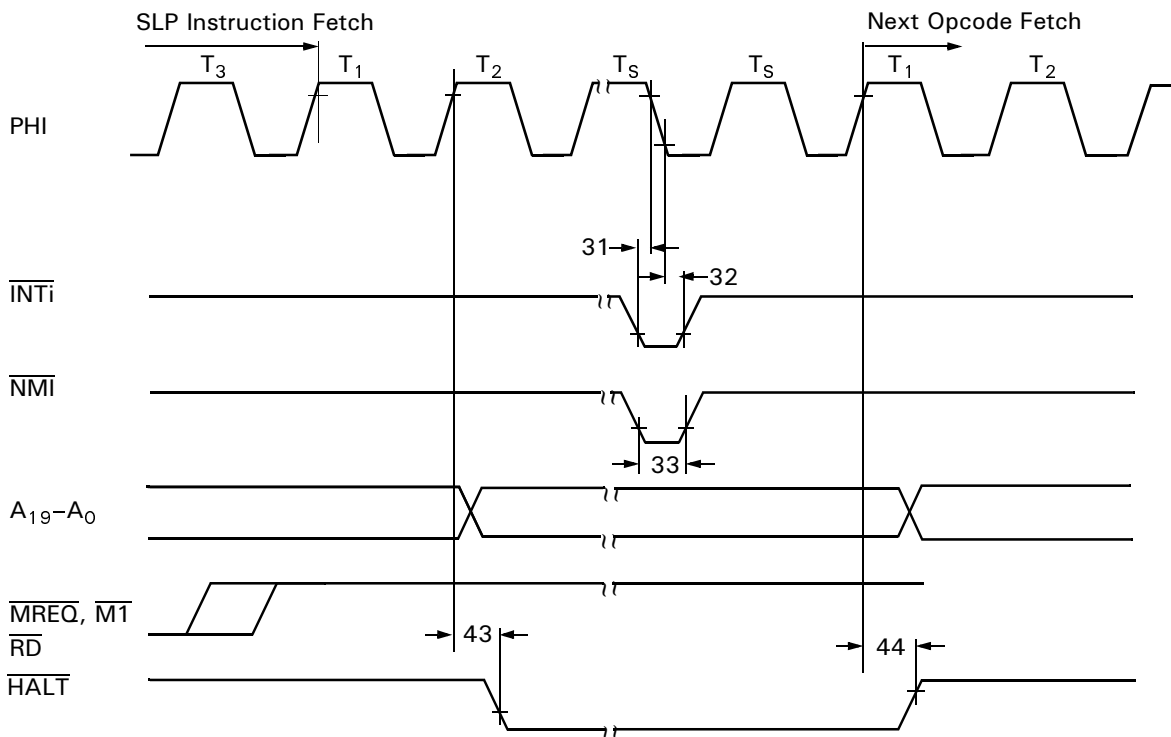


Figure 28. SLP Execution Cycle

ASCII CHANNEL CONTROL REGISTER B

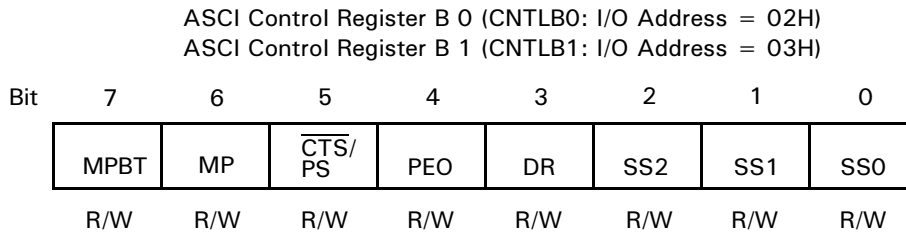


Figure 34. ASCII Channel Control Register B

MPBT: Multiprocessor Bit Transmit (Bit 7). When multiprocessor communication format is selected (MP bit = 1), MPBT is used to specify the MPB data bit for transmission. If MPBT = 1, then MPB = 1 is transmitted. If MPBT = 0, then MPB = 0 is transmitted. The MPBT state is undefined during and after RESET.

MP: Multiprocessor Mode (Bit 6). When MP is set to 1, the data format is configured for multiprocessor mode based on MOD2 (number of data bits) and MODO (number of stop bits) in CNTLA. The format is as follows:

Start bit + 7 or 8 data bits + MPB bit + 1 or 2 stop bits

Multiprocessor (MP = 1) format offers no provision for parity. If MP = 0, the data format is based on MODO, MOD1, MOD2, and may include parity. The MP bit is cleared to 0 during RESET.

$\overline{\text{CTS}}/\text{PS}$: Clear to Send/Prescale (Bit 5). When read, $\overline{\text{CTS}}/\text{PS}$ reflects the state of the external $\overline{\text{CTS}}$ input. If the $\overline{\text{CTS}}$ input pin is High, $\overline{\text{CTS}}/\text{PS}$ is read as 1.

Note: When the $\overline{\text{CTS}}$ input pin is High, the TDRE bit is inhibited (that is, held at 0).

For channel 1, the $\overline{\text{CTS}}$ input is multiplexed with RXS pin (Clocked Serial Receive Data). Thus, $\overline{\text{CTS}}/\text{PS}$ is only valid when read if the channel 1 CTS1E bit = 1 and the $\overline{\text{CTS}}$ input pin function is selected. The READ data of $\overline{\text{CTS}}/\text{PS}$ is not affected by $\overline{\text{RESET}}$.

If the SS2–0 bits in this register are not 111, and the BRG mode bit in the ASEXT register is 0, then writing to this bit sets the prescale (PS) control. Under those circumstances, a 0 indicates a divide-by-10 prescale function while a 1 indicates divide-by-30. The bit resets to 0.

PEO: Parity Even Odd (Bit 4). PEO selects even or odd parity. PEO does not affect the enabling/disabling of parity (MOD1 bit of CNTLA). If PEO is cleared to 0, even parity is selected. If PEO is set to 1, odd parity is selected. PEO is cleared to 0 during RESET.

DR: Divide Ratio (Bit 3). If the X1 bit in the ASEXT register is 0, this bit specifies the divider used to obtain baud rate from the data sampling clock. If DR is reset to 0, divide-by-16 is used, while if DR is set to 1, divide-by-64 is used. DR is cleared to 0 during RESET.

SS2,1,0: Source/Speed Select 2,1,0 (Bits 2–0). First, if these bits are 111, as they are after a RESET, the CKA pin is used as a clock input, and is divided by 1, 16, or 64 depending on the DR bit and the X1 bit in the ASEXT register.

If these bits are not 111 and the BRG mode bit is ASEXT is 0, then these bits specify a power-of-two divider for the PHI clock as indicated in Table 10.

Setting or leaving these bits as 111 makes sense for a channel only when its CKA pin is selected for the CKA function. CKA0/CKS offers the CKA0 function when bit 4 of the System Configuration Register is 0. $\overline{\text{DCD0}}/\text{CKA1}$ offers the CKA1 function when bit 0 of the Interrupt Edge register is 1.

Table 10. Divide Ratio

SS2	SS1	SS0	Divide Ratio
0	0	0	÷1
0	0	1	÷2
0	1	0	÷4
0	1	1	÷8
1	0	0	÷16
1	0	1	÷32
1	1	0	÷64
1	1	1	External Clock

ASCII STATUS REGISTER 0,1

Each ASCII channel status register (STAT0,1) allows interrogation of ASCII communication, error and modem control

signal status, and the enabling or disabling of ASCII interrupts.

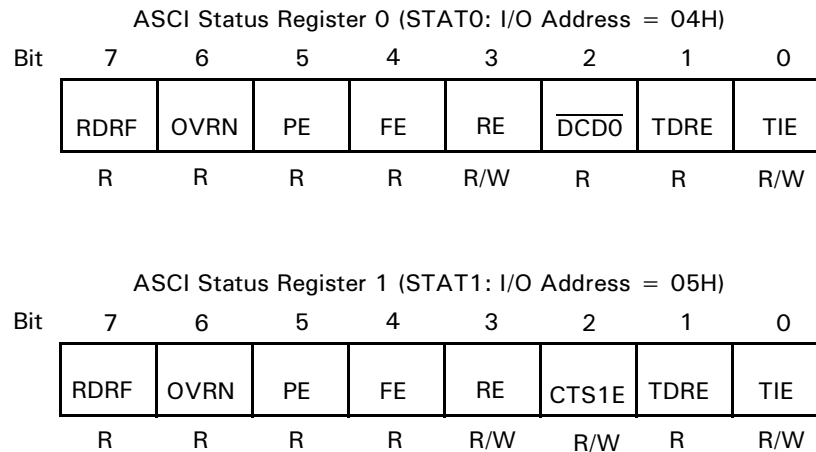


Figure 35. ASCII Status Registers

RDRF: Receive Data Register Full (Bit 7). RDRF is set to 1 when an incoming data byte is loaded into an empty Rx FIFO. If a framing or parity error occurs, RDRF is still set and the receive data (which generated the error) is still loaded into the FIFO. RDRF is cleared to 0 by reading RDR and most recently received character in the FIFO from IOSTOP mode, during RESET and for ASCII0 if the $\overline{\text{DCD0}}$ input is auto-enabled and is negated (High).

OVRN: Overrun Error (Bit 6). An overrun condition occurs if the receiver finishes assembling a character but the Rx FIFO is full so there is no room for the character. However, this status bit is not set until the most recent character received before the overrun becomes the oldest byte in the FIFO. This bit is cleared when software writes a 1 to the EFR bit in the CNTLA register. The bit may also be cleared by RESET in IOSTOP mode or ASCII0 if the $\overline{\text{DCD0}}$ pin is auto enabled and is negated (High).

Note: When an overrun occurs, the receiver does not place the character in the shift register into the FIFO, nor any subsequent characters, until the most recent good character enters the top of the FIFO so that OVRN is set. Software then writes a 1 to EFR to clear it.

PE: Parity Error (Bit 5). A parity error is detected when parity checking is enabled. When the MOD1 bit in the

CNTLA register is 1, a character is assembled in which the parity does not match the PEO bit in the CNTLB register. However, this status bit is not set until or unless the error character becomes the oldest one in the Rx FIFO. PE is cleared when software writes a 1 to the EFR bit in the CNTRLA register. PE is also cleared by RESET in IOSTOP mode, or on ASCII0, if the $\overline{\text{DCD0}}$ pin is auto-enabled and is negated (High).

FE: Framing Error (Bit 4). A framing error is detected when the stop bit of a character is sampled as 0/SPACE. However, this status bit is not set until/unless the error character becomes the oldest one in the Rx FIFO. FE is cleared when software writes a 1 to the EFR bit in the CNTLA register. FE is also cleared by RESET in IOSTOP mode, or on ASCII0, if the $\overline{\text{DCD0}}$ pin is auto-enabled and is negated (High).

REI: Receive Interrupt Enable (Bit 3). RIE should be set to 1 to enable ASCII receive interrupt requests. When RIE is 1, the Receiver requests an interrupt when a character is received and RDRF is set, but only if neither DMA channel requires its request-routing field to be set to receive data from this ASCII. That is, if SM1-0 are 11 and SAR17-16 are 10, or DIM1 is 1 and IAR17-16 are 10, then ASCII1 does not request an interrupt for RDRF. If RIE is 1, either ASCII requests an interrupt when OVRN, PE or FE is set, and

ASCI0 requests an interrupt when $\overline{DCD0}$ goes High. RIE is cleared to 0 by RESET.

$\overline{DCD0}$: Data Carrier Detect (Bit 2 STAT0). This bit is set to 1 when the pin is High. It is cleared to 0 on the first READ of STAT0 following the pin's transition from High to Low and during RESET. When bit 6 of the ASEXTO register is 0 to select auto-enabling, and the pin is negated (High), the receiver is reset and its operation is inhibited.

$\overline{CTS1E}$: Clear To Send (Bit 2 STAT1). Channel 1 features an external $\overline{CTS1}$ input, which is multiplexed with the receive data pin RSX for the CSI/O. Setting this bit to 1 selects the CTS1 function; clearing the bit to 0 selects the RXS function.

TDRE: Transmit Data Register Empty (Bit 1). TDRE = 1 indicates that the TDR is empty and the next transmit data byte is written to TDR. After the byte is written to TDR, TDRE is cleared to 0 until the ASCI transfers the byte from TDR to the TSR and then TDRE is again set to 1. TDRE is set to 1 in IOSTOP mode and during RESET. On ASCI0, if the $\overline{CTS0}$ pin is auto-enabled in the ASEXTO register and the pin is High, TDRE is reset to 0.

TIE: Transmit Interrupt Enable (Bit 0). TIE should be set to 1 to enable ASCI transmit interrupt requests. If TIE = 1, an interrupt is requested when TDRE = 1. TIE is cleared to 0 during RESET.

ASCI TRANSMIT DATA REGISTERS

Register addresses 06H and 07H hold the ASCI transmit data for channel 0 and channel 1, respectively.

ASCI Transmit Data Registers Channel 0

Mnemonic TDR0
Address 06H

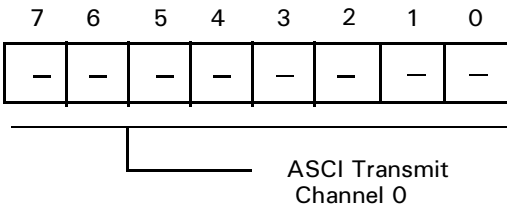


Figure 36. ASCII Register

ASCI Transmit Data Registers Channel 1

Mnemonic TDR1
Address 07H

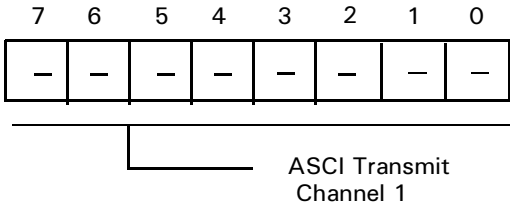


Figure 37. ASCII Register

DMA SOURCE ADDRESS REGISTER CHANNEL 0

The DMA Source Address Register Channel 0 specifies the physical source address for channel 0 transfers. The register contains 20 bits and can specify up to 1024 KB memory addresses or up to 64-KB I/O addresses. Channel 0 source can be memory, I/O, or memory mapped I/O. For I/O, bits 17–16 of this register identify the Request Handshake signal.

DMA Source Address Register, Channel 0 Low

Mnemonic SAR0L
Address 20H

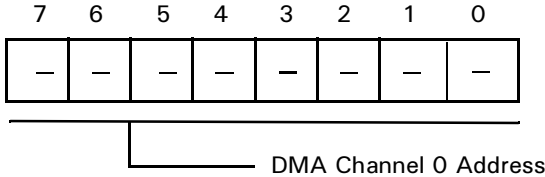


Figure 55. DMA Source Address Register 0 Low

DMA Source Address Register, Channel 0 High

Mnemonic SAR0H
Address 21H

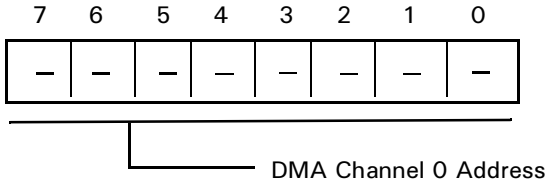


Figure 56. DMA Source Address Register 0 High

DMA Source Address Register Channel 0B

Mnemonic SAR0B
Address 22H

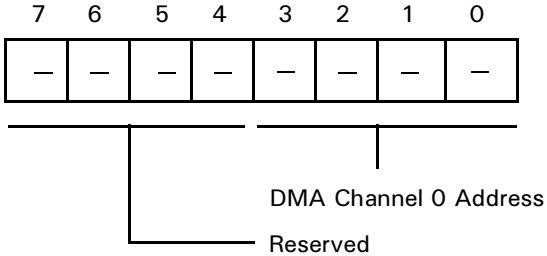


Figure 57. DMA Source Address Register 0B

If the source is in I/O space, bits 1–0 of this register select the DMA request signal for DMA0, as follows:

Bit 1 (A17)	Bit 0 (A16)	DMA Transfer Request
0	0	DREQ0 (external)
0	1	RDRF (ASCIO)
1	0	RDRF (ASC11)
1	1	Reserved

DMA DESTINATION ADDRESS REGISTER CHANNEL 0

The DMA Destination Address Register Channel 0 specifies the physical destination address for channel 0 transfers. The register contains 20 bits and can specify up to 1024-KB memory addresses or up to 64-KB I/O addresses. Channel 0 destination can be memory, I/O, or memory mapped I/O. For I/O, the MS bits of this register identify the Request Handshake signal for channel 0.

DMA Destination Address Register Channel 0 Low

Mnemonic DAR0L
Address 23H

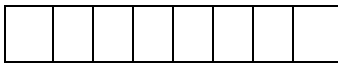


Figure 58. DMA Destination Address Register Channel 0 Low

DMA Destination Address Register Channel 0 High

Mnemonic DAR0H
Address 24H

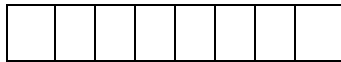


Figure 59. DMA Destination Address Register Channel 0 High

DMA Destination Address Register Channel 0B

Mnemonic DAR0B
Address 25H

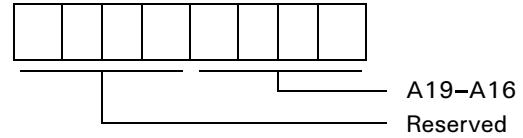


Figure 60. DMA Destination Address Register Channel 0B

If the DMA destination is in I/O space, bits 1–0 of this register select the DMA request signal for DMA0, as follows:

Bit 1 (A17)	Bit 0 (A16)	DMA Transfer Request
0	0	DREQ0 (external)
0	1	TDR0 (ASCII0)
1	0	TDR1 (ASCII1)
1	1	Not Used

DMA BYTE COUNT REGISTER CHANNEL 0

The DMA Byte Count Register Channel 0 specifies the number of bytes to be transferred. This register contains 16 bits and may specify up to 64-KB transfers. When one byte is transferred, the register is decremented by one. If n bytes should be transferred, n must be stored before the DMA operation.

Note: All DMA Count Register channels are undefined during RESET.

DMA Byte Count Register Channel 0 Low

Mnemonic BCR0L
Address 26H



Figure 61. DMA Byte Count Register 0 Low

DMA Byte Count Register Channel 0 High

Mnemonic BCR0H
Address 27H



Figure 62. DMA Byte Count Register 0 High

DMA Byte Count Register Channel 1 Low

Mnemonic BCR1L
Address 2EH



Figure 63. DMA Byte Count Register 1 Low

DMA Byte Count Register Channel 1 High

Mnemonic BCR1H
Address 2FH



Figure 64. DMA Byte Count Register 1 High

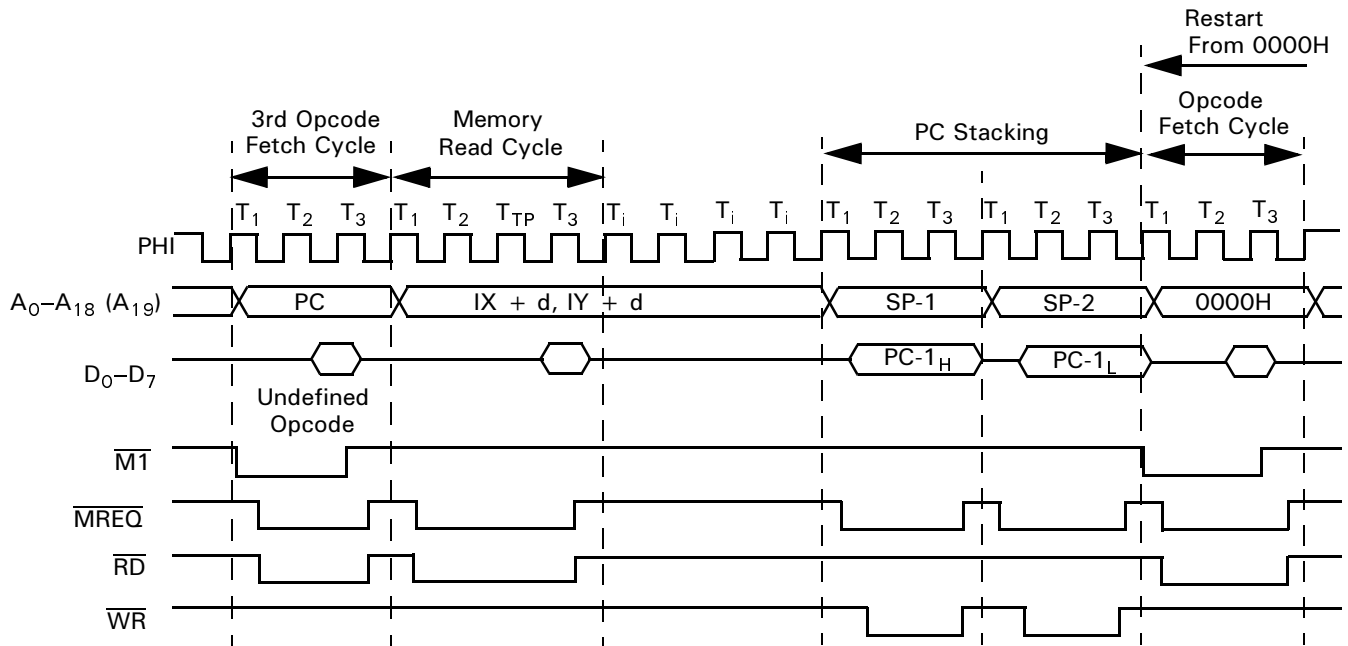


Figure 76. TRAP Timing—3rd Opcode Undefined

MMU COMMON BASE REGISTER

The Common Base Register (CBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical

address for Common Area 1 accesses. All bits of CBR are reset to 0 during RESET.

MMU Common Base Register

Mnemonic CBR
Address 38H

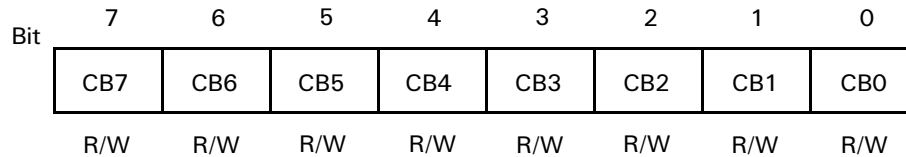


Figure 78. MMU Common Base Register (CBR: I/O Address = 38H)

MMU BANK BASE REGISTER

The Bank Base Register (BBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical ad-

dress for Bank Area accesses. All bits of BBR are reset to 0 during RESET.

MMU Bank Base Register

Mnemonic BBR
Address 39H

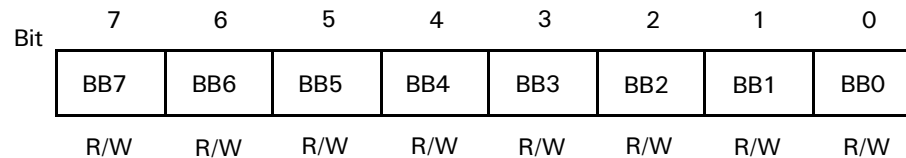


Figure 79. MMU Bank Base Register (BBR: I/O Address = 39H)

MMU COMMON/BANK AREA REGISTER

The Common/Bank Area Register (CBAR) specifies boundaries within the Z8S180/Z8L180 64-KB logical address

space for up to three areas; Common Area), Bank Area and Common Area 1.

MMU Common/Bank Area Register

Mnemonic CBAR
Address 3AH

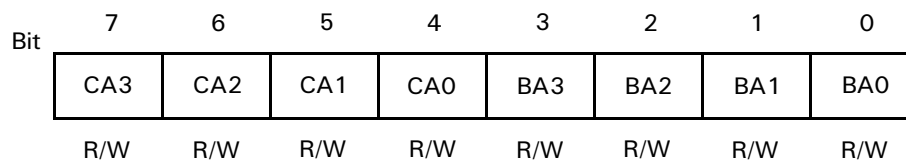


Figure 80. MMU Common/Bank Area Register (CBAR: I/O Address = 3AH)

I/O CONTROL REGISTER

The I/O Control Register (ICR) allows relocation of the internal I/O addresses. ICR also controls the enabling and disabling of IOSTOP mode (Figure 83).

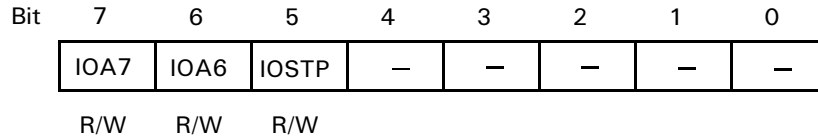


Figure 83. I/O Control Register (ICR: I/O Address = 3FH)

IOA7, 6: I/O Address Relocation (Bits 7,6). IOA7 and IOA6 relocate internal I/O as indicated in Figure 84.

Note: The high-order 8 bits of 16-bit internal I/O address are always 0. IOA7 and IOA6 are cleared to 0 during RESET.

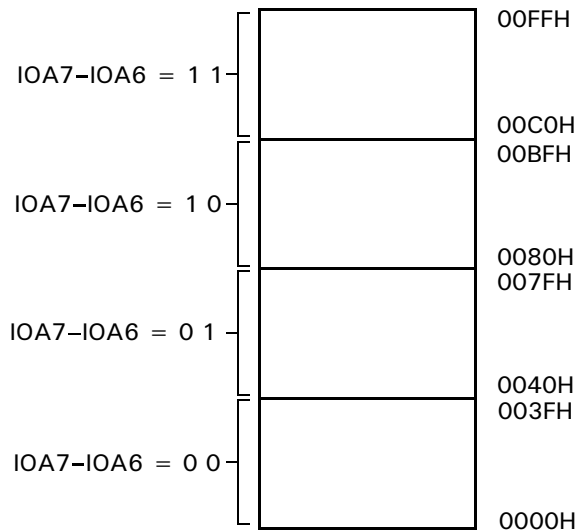


Figure 84. I/O Address Relocation

IOSTP: IOSTOP Mode (Bit 5). IOSTOP mode is enabled when IOSTP is set to 1. Normal I/O operation resumes when IOSTP is reprogrammed or RESET to 0.

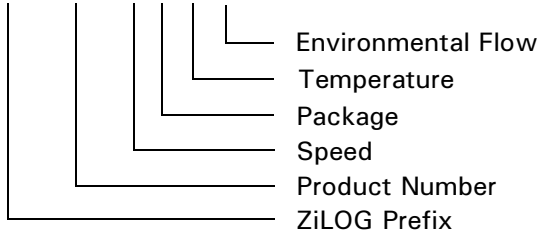
ORDERING INFORMATION

Codes	
Speed	10 = 10 MHz 20 = 20 MHz 33 = 33 MHz
Package	P = 60-Pin Plastic DIP V = 68-Pin PLCC F = 80-Pin QFP
Temperature	S = 0°C to +70°C E = -40°C to +85°C
Environmental	C = Plastic Standard

For fast results, contact your local ZiLOG sales office for assistance in ordering the part(s) required.

Example:

Z 8S180 10 P S C is a Z8S180 10-MHz 60-Pin DIP, 0° to +70°C, Plastic Standard Flow



Pre-Characterization Product

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or non-conformance

with some aspects of the document may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

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ZiLOG, Inc.
910 East Hamilton Avenue, Suite 110
Campbell, CA 95008
Telephone (408) 558-8500
FAX (408) 558-8300
Internet: <http://www.zilog.com>