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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8s18010vec

PIN IDENTIFICATION (Continued)

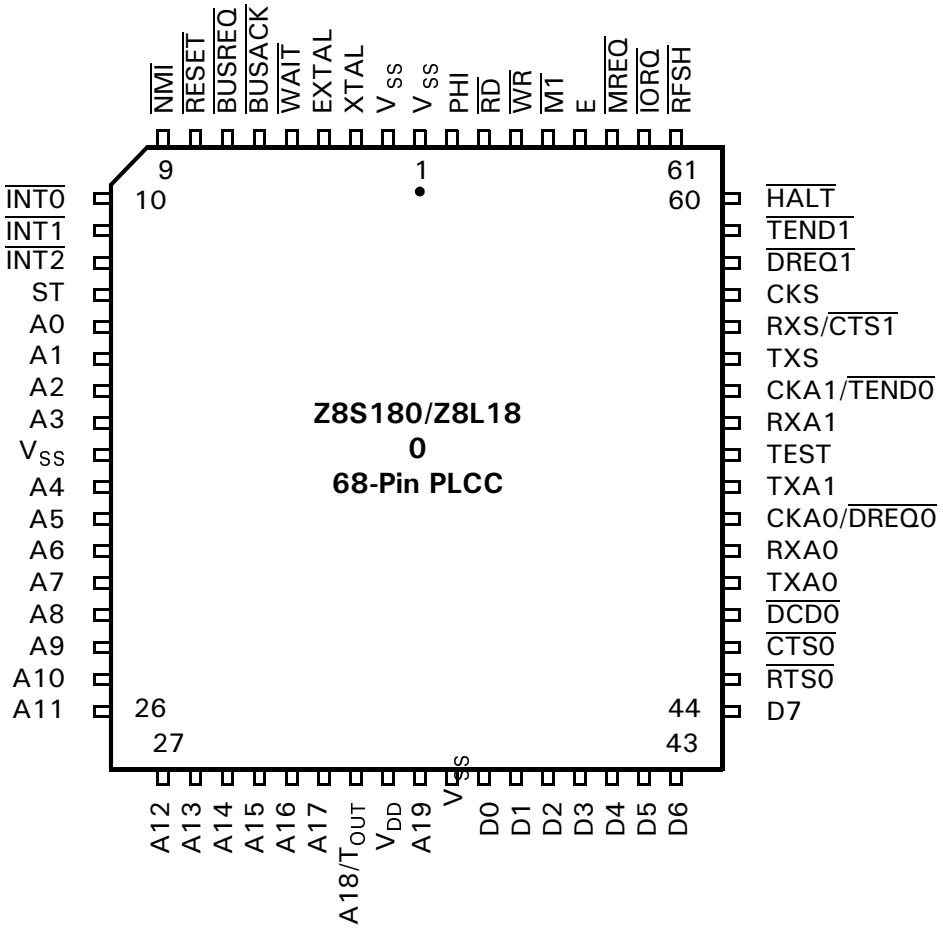


Figure 3. Z8S180/Z8L180 68-Pin PLCC Pin Configuration

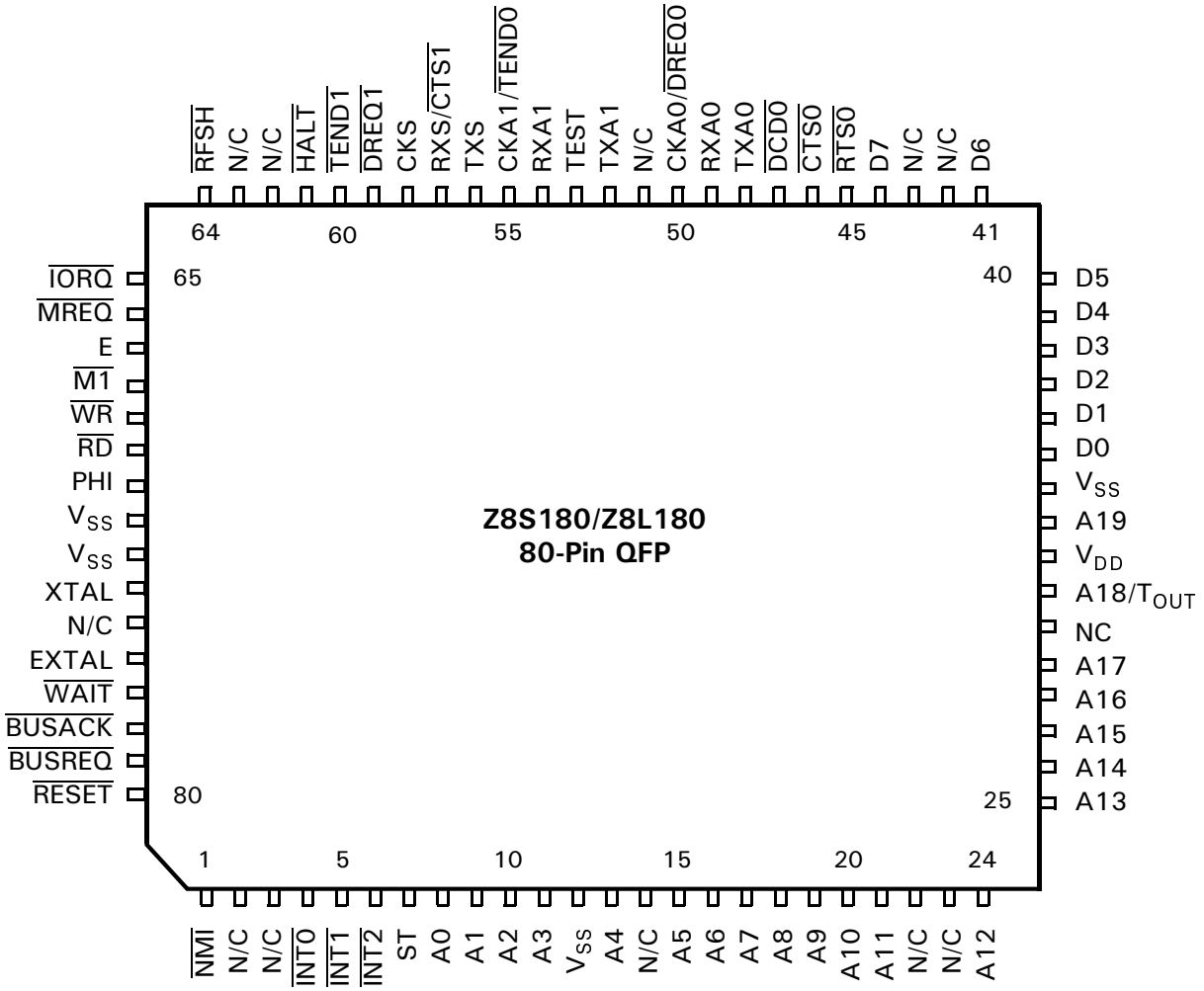


Figure 4. Z8S180/Z8L180 80-Pin QFP Pin Configuration

Table 1. Z8S180/Z8L180 Pin Identification

Pin Number and Package Type			Default	Secondary	
QFP	PLCC	DIP	Function	Function	Control
1	9	8	$\overline{NMI}$		
2			NC		
3			NC		
4	10	9	$\overline{INT0}$		
5	11	10	$\overline{INT1}$		
6	12	11	$\overline{INT2}$		
7	13	12	ST		
8	14	13	A0		
9	15	14	A1		
10	16	15	A2		
11	17	16	A3		
12	18		V_{SS}		

PIN IDENTIFICATION (Continued)

Table 1. Z8S180/Z8L180 Pin Identification (Continued)

Pin Number and Package Type			Default	Secondary	
QFP	PLCC	DIP	Function	Function	Control
13	19	17	A4		
14			NC		
15	20	18	A5		
16	21	19	A6		
17	22	20	A7		
18	23	21	A8		
19	24	22	A9		
20	25	23	A10		
21	26	24	A11		
22			NC		
23			NC		
24	27	25	A12		
25	28	26	A13		
26	29	27	A14		
27	30	28	A15		
28	31	29	A16		
29	32	30	A17		
30			NC		
31	33	31	A18	T_{OUT}	Bit 2 or Bit 3 of TCR
32	34	32	V_{DD}		
33	35		A19		
34	36	33	V_{SS}		
35	37	34	D0		
36	38	35	D1		
37	39	36	D2		
38	40	37	D3		
39	41	38	D4		
40	42	39	D5		
41	43	40	D6		
42			NC		
43			NC		
44	44	41	D7		
45	45	42	$\overline{RTS0}$		
46	46	43	$\overline{CTS0}$		
47	47	44	$\overline{DCD0}$		
48	48	45	TXA0		
49	49	46	RXA0		
50	50	47	CKA0	$\overline{DREQ0}$	Bit 3 or Bit 5 of DMODE
51			NC		
52	51	48	TXA1		

PIN DESCRIPTIONS (Continued)

ways recognized at the end of an instruction, regardless of the state of the interrupt-enable flip-flops. This signal forces CPU execution to continue at location 0066H.

PHI. System Clock (Output). The output is used as a reference clock for the MPU and the external system. The frequency of this output may be one-half, equal to, or twice the crystal or input clock frequency.

$\overline{RD}$. Read (Output, active Low, 3-state). $\overline{RD}$ indicates that the CPU wants to read data from either memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus.

$\overline{RFSH}$. Refresh (Output, active Low). Together with $\overline{MREQ}$, $\overline{RFSH}$ indicates that the current CPU machine cycle and the contents of the address bus should be used for refresh of dynamic memories. The low-order 8 bits of the address bus (A7–A0) contain the refresh address. *This signal is analogous to the $\overline{REF}$ signal of the Z64180.*

$\overline{RTS0}$. Request to Send 0 (Output, active Low); a programmable MODEM control signal for ASCI channel 0.

RXA0, RXA1. Receive Data 0 and 1 (Input). These signals are the receive data for the ASCI channels.

RXS. Clocked Serial Receive Data (Input). This line is the receive data for the CSI/O channel. RXS is multiplexed with the $\overline{CTS1}$ signal for ASCI channel 1.

ST. Status (Output). This signal is used with the $\overline{M1}$ and $\overline{HALT}$ output to decode the status of the CPU machine cycle. See Table 3.

Table 3. Status Summary

ST	$\overline{HALT}$	$\overline{M1}$	Operation
0	1	0	CPU Operation (1st Opcode Fetch)
1	1	0	CPU Operation (2nd Opcode and 3rd Opcode Fetch)
1	1	1	CPU Operation (MC Except Opcode Fetch)
0	X	1	DMA Operation
0	0	0	HALT Mode
1	0	1	SLEEP Mode (Including SYSTEM STOP Mode)

Notes:
X = Do not care.
MC = Machine Cycle.

$\overline{TEND0}$, $\overline{TEND1}$. Transfer End 0 and 1 (Outputs, active Low). This output is asserted active during the most recent WRITE cycle of a DMA operation. It is used to indicate the end of the block transfer. $\overline{TEND0}$ is multiplexed with CKA1.

TEST. Test (Output, not in DIP version). This pin is for test and should be left open.

T_{OUT}. Timer Out (Output). T_{OUT} is the output from PRT channel 1. This line is multiplexed with A18 of the address bus.

TXA0, TXA1. Transmit Data 0 and 1 (Outputs). These signals are the transmitted data from the ASCI channels. Transmitted data changes are with respect to the falling edge of the transmit clock.

TXS. Clocked Serial Transmit Data (Output). This line is the transmitted data from the CSI/O channel.

$\overline{WAIT}$. Wait (Input, active Low). $\overline{WAIT}$ indicates to the MPU that the addressed memory or I/O devices are not ready for data transfer. This input is sampled on the falling edge of T2 (and subsequent WAIT states). If the input is sampled Low, then the additional WAIT states are inserted until the $\overline{WAIT}$ input is sampled High, at which time execution continues.

$\overline{WR}$. WRITE (Output, active Low, 3-state). $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

XTAL. Crystal Oscillator Connection (Input). This pin should be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (see DC Characteristics).

Several pins are used for different conditions, depending on the circumstance.

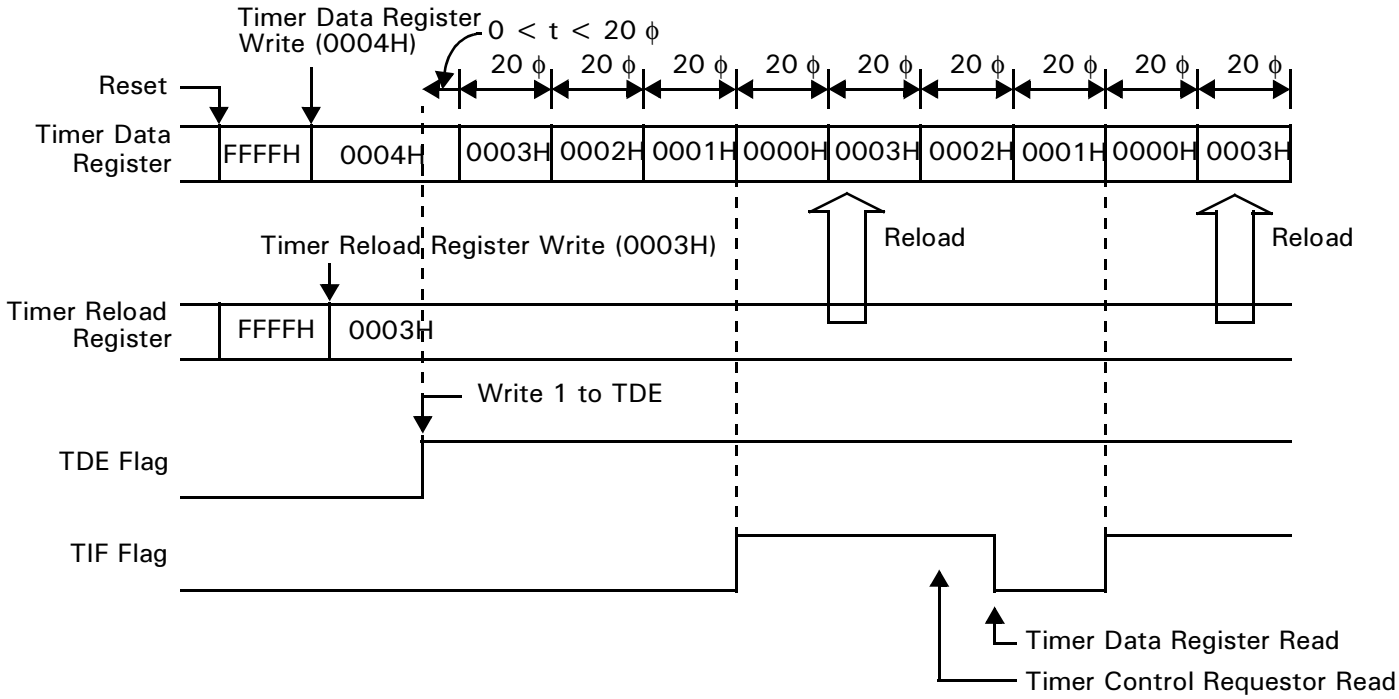


Figure 5. Timer Initialization, Count Down, and Reload Timing

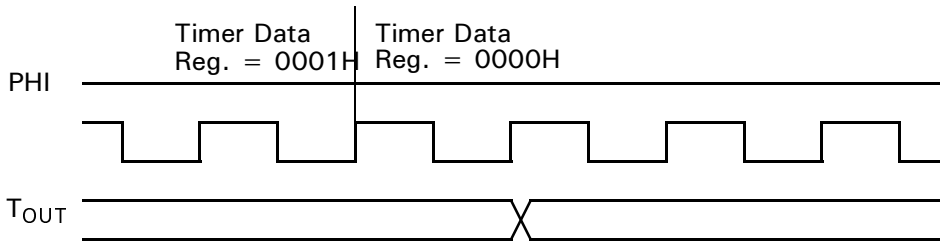


Figure 6. Timer Output Timing

Clocked Serial I/O (CSI/O). The CSI/O channel provides a half-duplex serial transmitter and receiver. This channel can be used for simple high-speed data connection to another microprocessor or microcomputer. TRDR is used for both CSI/O transmission and reception. Thus, the system design must ensure that the constraints of half-duplex operation are met (Transmit and Receive operation cannot occur simultaneously). For example, if a CSI/O transmission is attempted while the CSI/O is receiving data, a CSI/O does not work.

Note: TRDR is not buffered. Performing a CSI/O transmit while the previous transmission is still in progress causes the data to be immediately updated and corrupts the transmit operation. Similarly, reading TRDR while a transmit or receive is in progress should be avoided.

This condition provides a technique for synchronization with high-speed external events without incurring the latency imposed by an interrupt-response sequence. Figure 14 depicts the timing for exiting SLEEP mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes about 1.5 clock ticks to restart.

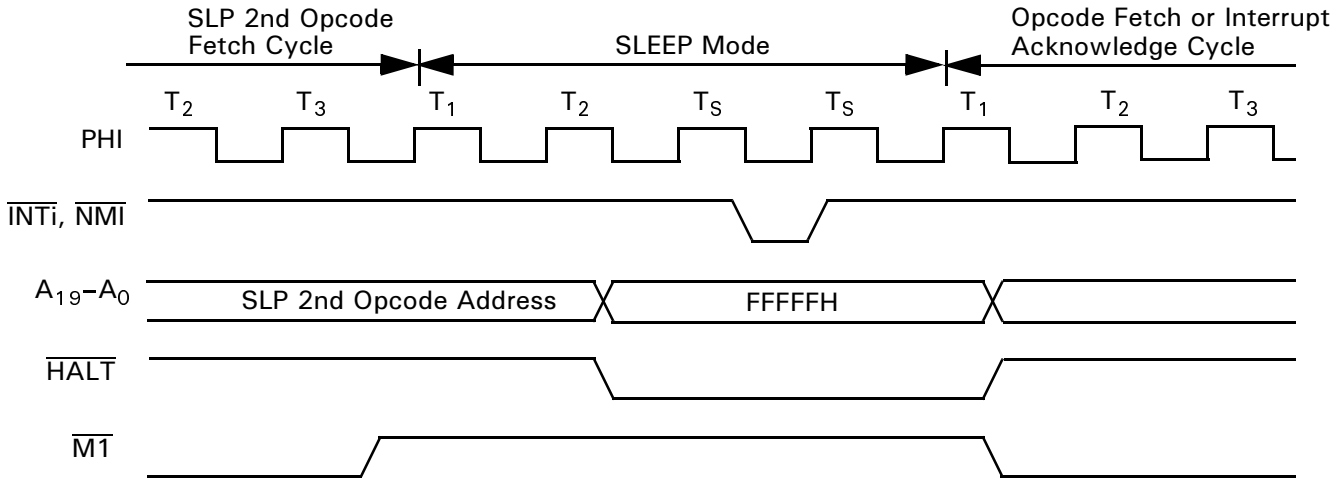


Figure 14. SLEEP Timing

IOSTOP Mode. IOSTOP mode is entered by setting the IOSTOP bit of the I/O Control Register (ICR) to 1. In this case, on-chip I/O (ASCI, CSI/O, PRT) stops operating. However, the CPU continues to operate. Recovery from IOSTOP mode is performed by resetting the IOSTOP bit in ICR to 0.

SYSTEM STOP Mode. SYSTEM STOP mode is the combination of SLEEP and IOSTOP modes. SYSTEM STOP mode is entered by setting the IOSTOP bit in ICR to 1 followed by execution of the SLP instruction. In this mode, on-chip I/O and CPU stop operating, reducing power consumption, but the PHI output continues to operate. Recovery from SYSTEM STOP mode is the same as recovery from SLEEP mode except that internal I/O sources (disabled by IOSTOP) cannot generate a recovery interrupt.

IDLE Mode. Software puts the Z8S180/Z8L180 into this mode by performing the following actions:

- Set the IOSTOP bit (ICR5) to 1
- Set CCR6 to 0
- Set CCR3 to 1
- Execute the SLP instruction

The oscillator keeps operating but its output is blocked to all circuitry including the PHI pin. DRAM refresh and all internal devices stop, but external interrupts can occur. Bus granting to external Masters can occur if the BREST bit in the CPU control Register (CCR5) was set to 1 before IDLE mode was entered.

The Z8S180/Z8L180 leaves IDLE mode in response to a Low on $\overline{\text{RESET}}$, an external interrupt request on $\overline{\text{NMI}}$, or an external interrupt request on $\overline{\text{INT0}}$, $\overline{\text{INT1}}$ or $\overline{\text{INT2}}$ that is enabled in the INT/TRAP Control Register. As previously described for SLEEP mode, when the Z8S180/Z8L180 leaves IDLE mode due to an $\overline{\text{NMI}}$, or due to an enabled external interrupt request when the $\overline{\text{IEF}}$ flag is 1 due to an EI instruction, the device starts by performing the interrupt with the return address of the instruction after the SLP instruction.

If an external interrupt enables the INT/TRAP control register while the IEF1 bit is 0, Z8S180/Z8L180 leaves IDLE mode; specifically, the processor restarts by executing the instructions following the SLP instruction.

Figure 15 indicates the timing for exiting IDLE mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes about 9.5 clocks to restart.

OPERATION MODES (Continued)

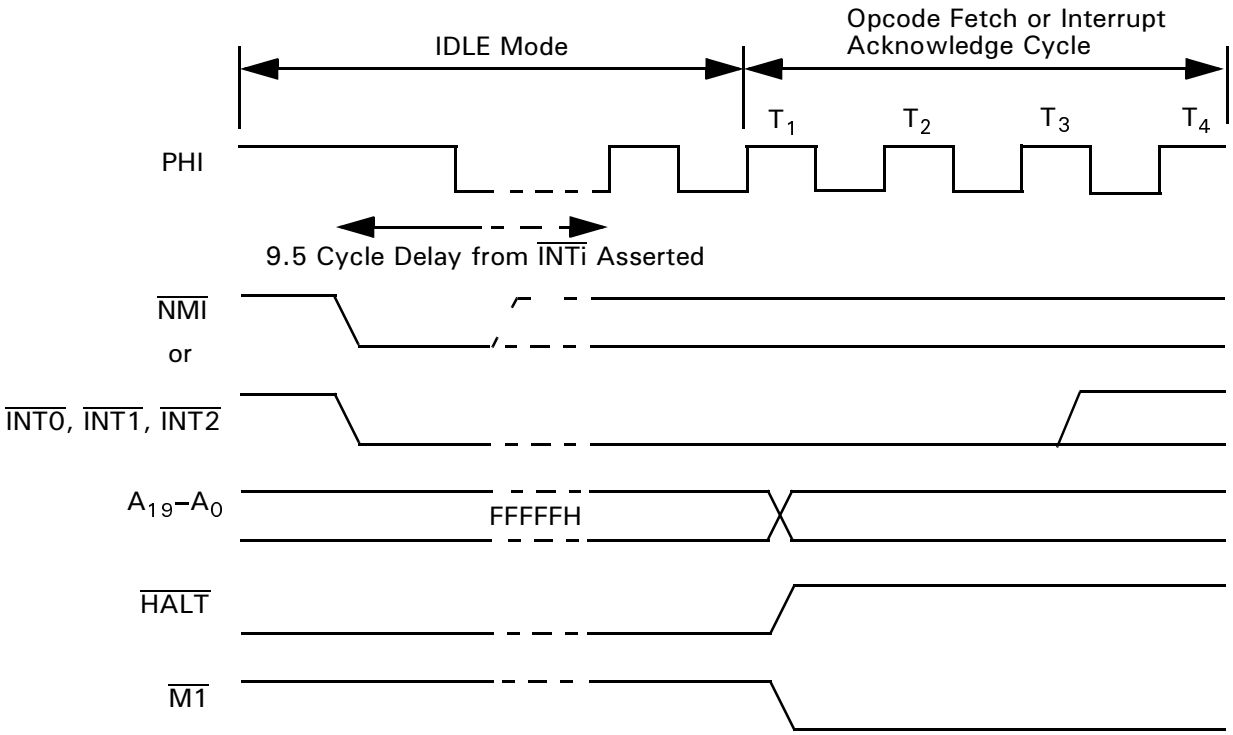


Figure 15. Z8S180/Z8L180 IDLE Mode Exit Due To External Interrupt

While the Z8S180/Z8L180 is in IDLE mode, it grants the bus to an external Master if the BREXT bit (CCR5) is 1. Figure 16 depicts the timing for this sequence.

Note: A response to a bus request takes 8 clock cycles longer than in normal operation.

After the external Master negates the Bus Request, the Z8S180/Z8L180 disables the PHI clock and remains in IDLE mode.

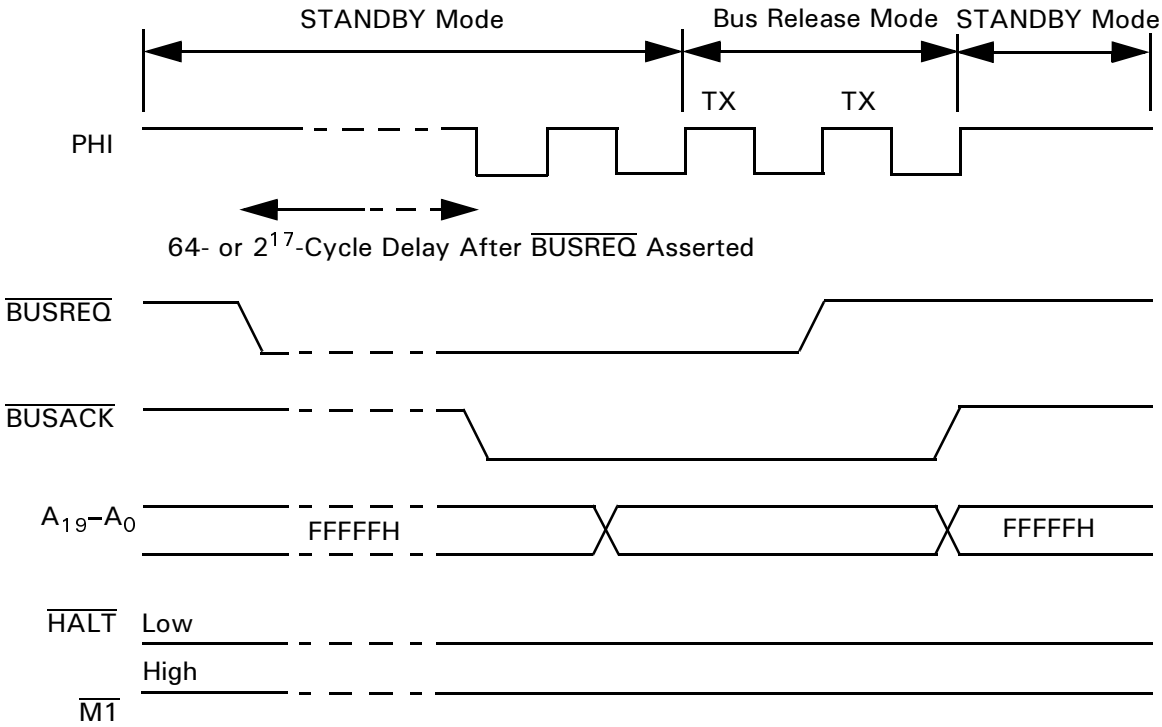


Figure 18. Bus Granting to External Master During STANDBY Mode

STANDARD TEST CONDITIONS

The following standard test conditions apply to DC Characteristics, unless otherwise noted. All voltages are referenced to V_{SS} (0V). Positive current flows into the referenced pin.

All AC parameters assume a load capacitance of 100 pF. Add a 10-ns delay for each 50-pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to V_{OL} MAX or V_{OL} MIN as indicated in Figures 20 through 30 (except for CLOCK, which is referenced to the 10% and 90% points). Ordering Information lists temperature ranges and product numbers. Find package drawings in Package Information.

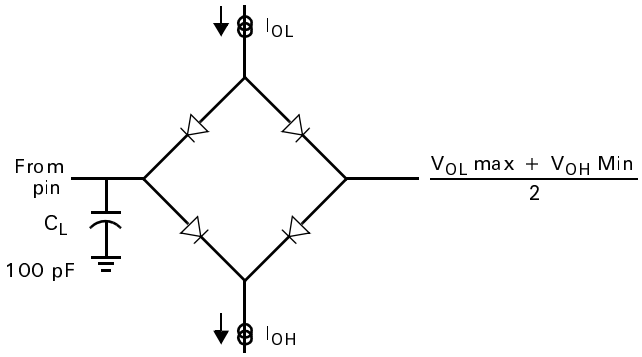


Figure 19. AC Parameter Test Circuit

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 ~ +7.0	V
Input Voltage	V_{IN}	–0.3 ~ V_{cc} +0.3	V
Operating Temperature	T_{OPR}	0 ~ 70	°C
Extended Temperature	T_{EXT}	–40 ~ 85	°C
Storage Temperature	T_{STG}	–55 ~ +150	°C

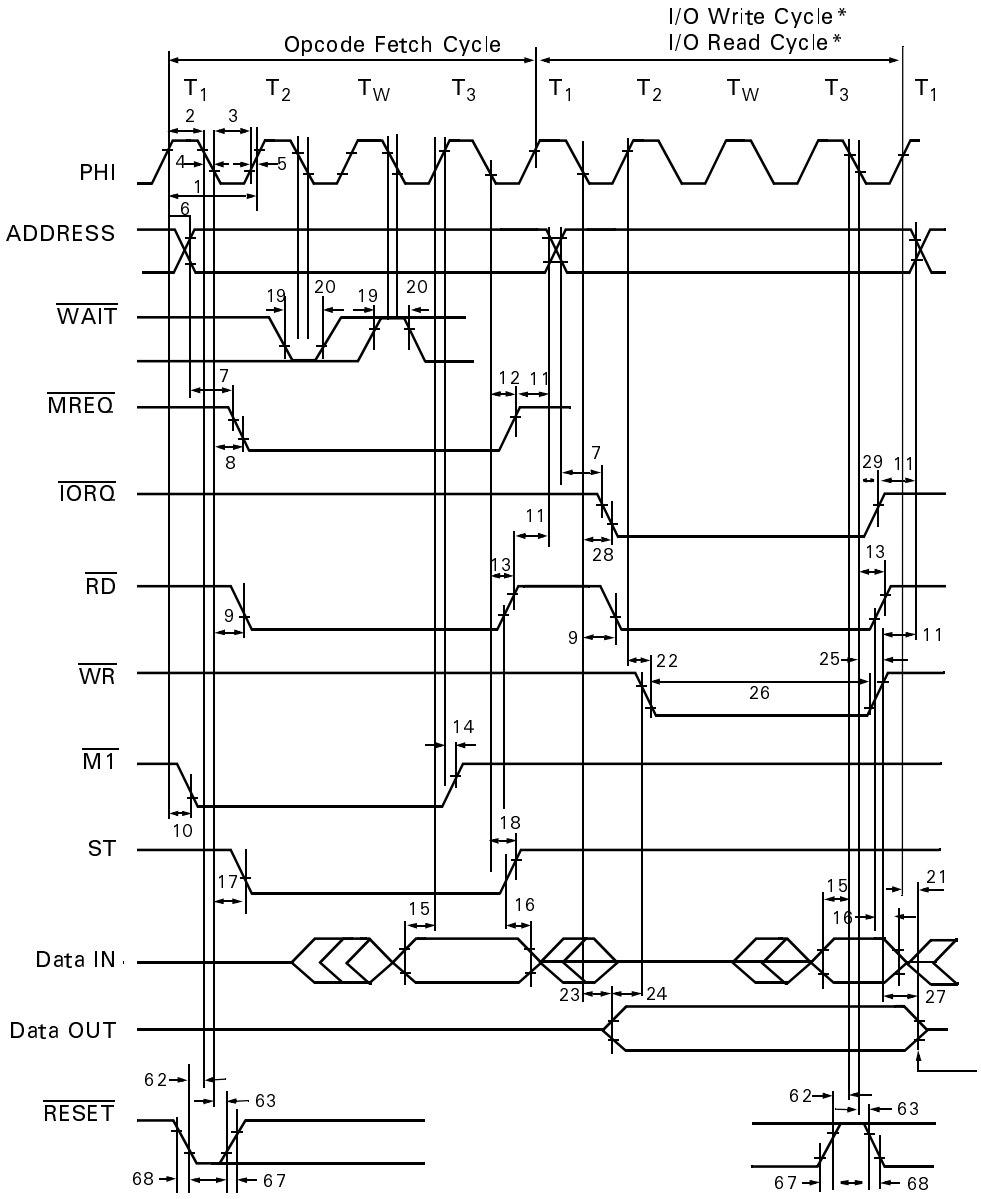
Note: Permanent damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability.

AC CHARACTERISTICS—Z8S180

Table 8. Z8S180 AC Characteristics
V_{DD} = 5V ±10% or V_{DD} = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation

			Z8S180—20 MHz		Z8S180—33 MHz		
Number	**Symbol**	**Item**	**Min**	**Max**	**Min**	**Max**	**Unit**
1	t_{CYC}	Clock Cycle Time	50	DC	30	DC	ns
2	t_{CHW}	Clock "H" Pulse Width	15	—	10	—	ns
3	t_{CLW}	Clock "L" Pulse Width	15	—	10	—	ns
4	t_{CF}	Clock Fall Time	—	10	—	5	ns
5	t_{CR}	Clock Rise Time	—	10	—	5	ns
6	t_{AD}	PHI Rise to Address Valid Delay	—	30	—	15	ns
7	t_{AS}	Address Valid to $\overline{MREQ}$ Fall or $\overline{IORQ}$ Fall)	5	—	5	—	ns
8	t_{MED1}	PHI Fall to $\overline{MREQ}$ Fall Delay	—	25	—	15	ns
9	t_{RDD1}	PHI Fall to $\overline{RD}$ Fall Delay $\overline{IOC}$ = 1	—	25	—	15	ns
		PHI Rise to $\overline{RD}$ Rise Delay $\overline{IOC}$ = 0	—	25	—	15	
10	t_{M1D1}	PHI Rise to $\overline{M1}$ Fall Delay	—	35	—	15	ns
11	t_{AH}	Address Hold Time from $\overline{MREQ}$, $\overline{IOREQ}$, $\overline{RD}$, $\overline{WR}$ High	5	—	5	—	ns
12	t_{MED2}	PHI Fall to $\overline{MREQ}$ Rise Delay	—	25	—	15	ns
13	t_{RDD2}	PHI Fall to $\overline{RD}$ Rise Delay	—	25	—	15	ns
14	t_{M1D2}	PHI Rise to $\overline{M1}$ Rise Delay	—	40	—	15	ns
15	t_{DRS}	Data Read Set-up Time	10	—	5	—	ns
16	t_{DRH}	Data Read Hold Time	0	—	0	—	ns
17	t_{STD1}	PHI Fall to ST Fall Delay	—	30	—	15	ns
18	t_{STD2}	PHI Fall to ST Rise Delay	—	30	—	15	ns
19	t_{WS}	$\overline{WAIT}$ Set-up Time to PHI Fall	15	—	10	—	ns
20	t_{WH}	$\overline{WAIT}$ Hold Time from PHI Fall	10	—	5	—	ns
21	t_{WDZ}	PHI Rise to Data Float Delay	—	35	—	20	ns
22	t_{WRD1}	PHI Rise to $\overline{WR}$ Fall Delay	—	25	—	15	ns
23	t_{WDD}	PHI Fall to Write Data Delay Time	—	25	—	15	ns
24	t_{WDS}	Write Data Set-up Time to $\overline{WR}$ Fall	10	—	10	—	ns
25	t_{WRD2}	PHI Fall to $\overline{WR}$ Rise Delay	—	25	—	15	ns
26	t_{WRP}	$\overline{WR}$ Pulse Width (Memory Write Cycle)	80	—	45	—	ns
26a		$\overline{WR}$ Pulse Width (I/O Write Cycle)	150	—	70	—	ns
27	t_{WDH}	Write Data Hold Time from $\overline{WR}$ Rise	10	—	5	—	ns
28	t_{IOD1}	PHI Fall to $\overline{IORQ}$ Fall Delay $\overline{IOC}$ = 1	—	25	—	15	ns
		PHI Rise to $\overline{IORQ}$ Fall Delay $\overline{IOC}$ = 0	—	25	—	15	
29	t_{IOD2}	PHI Fall to $\overline{IORQ}$ Rise Delay	—	25	—	15	ns
30	t_{IOD3}	$\overline{M1}$ Fall to $\overline{IORQ}$ Fall Delay	125	—	80	—	ns
31	t_{INTS}	$\overline{INT}$ Set-up Time to PHI Fall	20	—	15	—	ns

TIMING DIAGRAMS



Note: *Memory Read/Write Cycle timing is the same as I/O Read/Write Cycle except there are no automatic wait states (T_W), and $\overline{MREQ}$ is active instead of $\overline{IORQ}$.

Figure 20. CPU Timing
(Opcode Fetch Cycle, Memory Read Cycle, Memory Write Cycle, I/O Write Cycle, I/O Read Cycle)

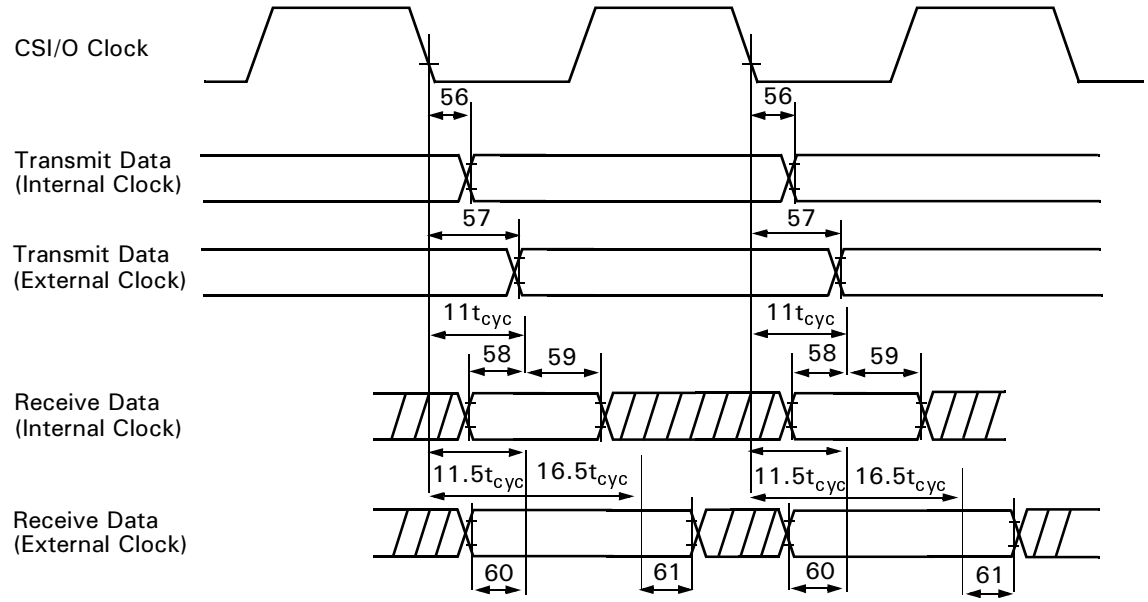


Figure 29. CSI/O Receive/Transmit Timing

External Clock Rise Time and Fall Time

Input Rise Time and Fall Time (Except EXTAL, $\overline{\text{RESET}}$)

Figure 30. Rise Time and Fall Times

Bit 2 LNIO. This bit controls the drive capability of certain external I/O pins of the Z8S180/Z8L180. When this bit is set to 1, the output drive capability of the following pins is reduced to 33 percent of the original drive capability:

$\overline{RTS0}$	TxS
CKA1/$\overline{TEND0}$	CKA0/$\overline{DREQ0}$
TXA0	TXA1
$\overline{TENDi}$	CKS

Bit 1 LNCPUCTL. This bit controls the drive capability of the CPU Control pins. When this bit is set to 1, the output drive capability of the following pins is reduced to 33 percent of the original drive capability:

$\overline{BUSACK}$	$\overline{RD}$
$\overline{WR}$	$\overline{M1}$
$\overline{MREQ}$	$\overline{IORQ}$
$\overline{RFSH}$	$\overline{HALT}$
E	TEST
ST	

Bit 0 LNAD/DATA. This bit controls the drive capability of the Address/Data bus output drivers. If this bit is set to 1, the output drive capability of the Address and Data bus outputs is reduced to 33 percent of its original drive capability.

Data can be written into and read from the ASCI Transmit Data Register. If data is read from the ASCI Transmit Data Register, the ASCI data transmit operation is not affected by this READ operation.

ASCI Receive Shift Register 0,1 (RSR0,1). This register receives data shifted in on the RXA pin. When full, data is automatically transferred to the ASCI Receive Data Register (RDR) if it is empty. If RSR is not empty when the next incoming data byte is shifted in, an overrun error occurs. This register is not program accessible.

ASCI Receive Data FIFO 0,1 (RDR0, 1:I/O Address = 08H, 09H). The ASCI Receive Data Register is a read-only register. When a complete incoming data byte is assembled in RSR, it is automatically transferred to the 4 character Receive Data First-In First-Out (FIFO) memory. The oldest character in the FIFO (if any) can be read from the Receive Data Register (RDR). The next incoming data byte can be shifted into RSR while the FIFO is full. Thus, the ASCI receiver is well buffered.

ASCI STATUS FIFO

This four-entry FIFO contains Parity Error, Framing Error, Rx Overrun, and Break status bits associated with each character in the receive data FIFO. The status of the oldest character (if any) can be read from the ASCI status registers.

ASCI CHANNEL CONTROL REGISTER A

ASCI Control Register A 0 (CNTLA0: I/O Address = 00H)

Bit	7	6	5	4	3	2	1	0
	MPE	RE	TE	$\overline{\text{RTS0}}$	MPBR/ EFR	MOD2	MOD1	MOD0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASCI Control Register A 1 (CNTLA1: I/O Address = 01H)

Bit	7	6	5	4	3	2	1	0
	MPE	RE	TE	CKA1D	MPBR/ EFR	MOD2	MOD1	MOD0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 33. ASCI Channel Control Register A

MPE: Multi-Processor Mode Enable (Bit 7). The ASCI features a multiprocessor communication mode that utilizes an extra data bit for selective communication when a number of processors share a common serial bus. Multiprocessor data format is selected when the MP bit in CNTLB is set to 1. If multiprocessor mode is not selected (MP bit in CNTLB = 0), MPE has no effect. If multiprocessor mode is selected, MPE enables or disables the *wake-up* feature as follows. If MBE is set to 1, only received bytes in which the multiprocessor bit (MPB) = 1 can affect the RDRF and error flags. Effectively, other bytes (with MPB = 0) are *ignored* by the ASCI. If MPE is reset to 0, all bytes, regardless of the state of the MPB data bit, affect the REDR and error flags. MPE is cleared to 0 during RESET.

RE: Receiver Enable (Bit 6). When RE is set to 1, the ASCI transmitter is enabled. When TE is reset to 0, the transmitter is disables and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the previous contents of TDRE are held. TE is cleared to 0 in IOSTOP mode during RESET.

TE: Transmitter Enable (Bit 5). When TE is set to 1, the ASCI receiver is enabled. When $\overline{\text{TE}}$ is reset to 0, the transmitter is disabled and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the pre-

ASCI STATUS REGISTER 0,1

Each ASCI channel status register (STAT0,1) allows interrogation of ASCI communication, error and modem control signal status, and the enabling or disabling of ASCI interrupts.

ASCI Status Register 0 (STAT0: I/O Address = 04H)

Bit	7	6	5	4	3	2	1	0
	RDRF	OVRN	PE	FE	RE	$\overline{DCD0}$	TDRE	TIE
	R	R	R	R	R/W	R	R	R/W

ASCI Status Register 1 (STAT1: I/O Address = 05H)

Bit	7	6	5	4	3	2	1	0
	RDRF	OVRN	PE	FE	RE	CTS1E	TDRE	TIE
	R	R	R	R	R/W	R/W	R	R/W

Figure 35. ASCI Status Registers

RDRF: Receive Data Register Full (Bit 7). RDRF is set to 1 when an incoming data byte is loaded into an empty Rx FIFO. If a framing or parity error occurs, RDRF is still set and the receive data (which generated the error) is still loaded into the FIFO. RDRF is cleared to 0 by reading RDR and most recently received character in the FIFO from IOSTOP mode, during RESET and for ASCI0 if the $\overline{DCD0}$ input is auto-enabled and is negated (High).

OVRN: Overrun Error (Bit 6). An overrun condition occurs if the receiver finishes assembling a character but the Rx FIFO is full so there is no room for the character. However, this status bit is not set until the most recent character received before the overrun becomes the oldest byte in the FIFO. This bit is cleared when software writes a 1 to the EFR bit in the CNTLA register. The bit may also be cleared by RESET in IOSTOP mode or ASCI0 if the $\overline{DCD0}$ pin is auto enabled and is negated (High).

Note: When an overrun occurs, the receiver does not place the character in the shift register into the FIFO, nor any subsequent characters, until the most recent good character enters the top of the FIFO so that OVRN is set. Software then writes a 1 to EFR to clear it.

PE: Parity Error (Bit 5). A parity error is detected when parity checking is enabled.When the MOD1 bit in the CNTLA register is 1, a character is assembled in which the parity does not match the PEO bit in the CNTLB register. However, this status bit is not set until or unless the error character becomes the oldest one in the Rx FIFO. PE is cleared when software writes a 1 to the EFR bit in the CNTRLA register. PE is also cleared by RESET in IOSTOP mode, or on ASCI0, if the $\overline{DCD0}$ pin is auto-enabled and is negated (High).

FE: Framing Error (Bit 4). A framing error is detected when the stop bit of a character is sampled as 0/SPACE. However, this status bit is not set until/unless the error character becomes the oldest one in the Rx FIFO. FE is cleared when software writes a 1 to the EFR bit in the CNTLA register. FE is also cleared by RESET in IOSTOP mode, or on ASCI0, if the $\overline{DCD0}$ pin is auto-enabled and is negated (High).

REI: Receive Interrupt Enable (Bit 3). RIE should be set to 1 to enable ASCI receive interrupt requests. When RIE is 1, the Receiver requests an interrupt when a character is received and RDRF is set, but only if neither DMA channel requires its request-routing field to be set to receive data from this ASCI. That is, if SM1–0 are 11 and SAR17–16 are 10, or DIM1 is 1 and IAR17–16 are 10, then ASCI1 does not request an interrupt for RDRF. If RIE is 1, either ASCI requests an interrupt when OVRN, PE or FE is set, and

ASCI EXTENSION CONTROL REGISTER CHANNEL 0 AND CHANNEL 1

The ASCI Extension Control Registers (ASEXT0 and ASEXT1) control functions that have been added to the ASCIs in the Z8S180/Z8L180 family. All bits in this register reset to 0.

ASCI Extension Control Register 0 (ASEXT0 I/O Address = 12H)

Bit	7	6	5	4	3	2	1	0
	Reserved	DCD0 Disable	CTS0 Disable	X1	BRG0 Mode	Break Enable	Break	Send Break

ASCI Extension Control Register 1 (ASEXT1 I/O Address = 13H)

Bit	7	6	5	4	3	2	1	0
	Reserved	Reserved	Reserved	X1	BRG1 Mode	Break Enable	Break	Send Break

Figure 47. ASCI Extension Control Registers, Channels 0 and 1

DCD0 Disable (Bit 6, ASCI0 Only). If this bit is 0, then the $\overline{\text{DCD0}}$ pin auto-enables the ASCI0 receiver, such that when the pin is negated/High, the Receiver is held in a RESET state. If this bit is 1, the state of the $\overline{\text{DCD}}$-pin has no effect on receiver operation. In either state of this bit, software can read the state of the $\overline{\text{DCD0}}$ pin in the STAT0 register, and the receiver interrupts on a rising edge of $\overline{\text{DCD0}}$.

CTS0 Disable (Bit 5, ASCI0 Only). If this bit is 0, then the $\overline{\text{CTS0}}$ pin auto-enables the ASCIO transmitter, in that when the pin is negated/High, the TDRE bit in the STAT0 register is forced to 0. If this bit is 1, the state of the $\overline{\text{CTS0}}$ pin has no effect on the transmitter. Regardless of the state of this bit, software can read the state of the $\overline{\text{CTS0}}$ pin the CNTLB0 register.

X1 (Bit 4). If this bit is 1, the clock from the Baud Rate Generator or CKA pin is taken as a 1X-bit clock (sometimes called *isochronous mode*). In this mode, receive data on the RXA pin must be synchronized to the clock on the CKA pin, regardless of whether CKA is an input or an output. If this bit is 0, the clock from the Baud Rate Generator or CKA pin is divided by 16 or 64 per the DR bit in the CNTLB register, to obtain the actual bit rate. In this mode, receive data on the RXA pin is not required to be synchronized to a clock.

BRG Mode (Bit 3). If the SS2–0 bits in the CNTLB register are not 111, and this bit is 0, the ASCI Baud Rate Generator divides PHI by 10 or 30, depending on the PS bit in CNTLB, and factored by a power of two (selected by the SS2–0 bits), to obtain the clock that is presented to the transmitter and receiver and output on the CKA pin. If SS2–0 are not 111, and this bit is 1, the Baud Rate Generator divides PHI by twice the sum of the 16-bit value (programmed into the Time Constant registers) and 2. This mode is identical to the operation of the baud rate generator in the ESCC.

Break Enable (Bit 2). If this bit is 1, the receiver detects BREAK conditions and report them in bit 1, and the transmitter sends BREAKs under the control of bit 0.

Break Detect (Bit 1). The receiver sets this read-only bit to 1 when an all-zero character with a Framing Error becomes the oldest character in the Rx FIFO. The bit is cleared when software writes a 0 to the EFR bit in CNTLA register, also by RESET, by IOSTOP mode, and for ASCI0, if the $\overline{\text{DCD0}}$ pin is auto-enabled and is negated (High).

Send Break (Bit 0). If this bit and bit 2 are both 1, the transmitter holds the TXA pin Low to send a BREAK condition. The duration of the BREAK is under software control (one of the PRTs or CTCs can be used to time it). This bit resets to 0, in which state TXA carries the serial output of the transmitter.

Table 16 indicates all DMA transfer mode combinations of DM0, DM1, SM0, and SM1. Because I/O to/from I/O transfers are not implemented, 12 combinations are available.

Table 16. Transfer Mode Combinations

DM1	DM0	SM1	SM0	Transfer Mode	Address Increment/Decrement
0	0	0	0	Memory→Memory	SAR0 + 1, DAR0 + 1
0	0	0	1	Memory→Memory	SAR0–1, DAR0 + 1
0	0	1	0	Memory*→Memory	SAR0 fixed, DAR0 + 1
0	0	1	1	I/O→Memory	SAR0 fixed, DAR0 + 1
0	1	0	0	Memory→Memory	SAR0 + 1, DAR0–1
0	1	0	1	Memory→Memory	SAR0–1, DAR0–1
0	1	1	0	Memory*→Memory	SAR0 fixed, DAR0–1
0	1	1	1	I/O→Memory	SAR0 fixed, DAR0–1
1	0	0	0	Memory→Memory*	SAR0 + 1, DAR0 fixed
1	0	0	1	Memory→Memory*	SAR0–1, DAR0 fixed
1	0	1	0	Reserved	
1	0	1	1	Reserved	
1	1	0	0	Memory→I/O	SAR0 + 1, DAR0 fixed
1	1	0	1	Memory→I/O	SAR0–1, DAR0 fixed
1	1	1	0	Reserved	
1	1	1	1	Reserved	

Note: * Includes memory mapped I/O.

MMOD: Memory Mode Channel 0 (Bit 1). When channel 0 is configured for memory to/from memory transfers there is no Request Handshake signal to control the transfer timing. Instead, two automatic transfer timing modes are selectable: burst (MMOD = 1) and cycle steal (MMOD = 0). For burst memory to/from memory transfers, the DMAC takes control of the bus continuously until the DMA transfer completes (as indicated by the byte count register = 0). In cycle steal mode, the CPU is provided a cycle for each DMA byte transfer cycle until the transfer is completed.

For channel 0 DMA with I/O source or destination, the selected Request signal times the transfer ignoring MMOD. MMOD is cleared to 0 during RESET.

INTERRUPT VECTOR LOW REGISTER

Bits 7–5 of the Interrupt Vector Low Register (I_L) are used as bits 7–5 of the synthesized interrupt vector during interrupts for the $\overline{INT1}$ and $\overline{INT2}$ pins and for the DMAs, ASCIs, PRTs, and CSI/O. These three bits are cleared to 0 during RESET (Figure 74).

Interrupt Vector Low Register

Mnemonic: IL
Address 33H

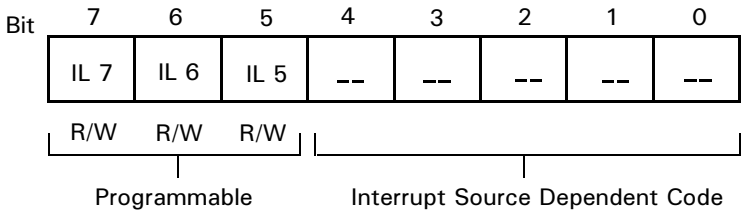


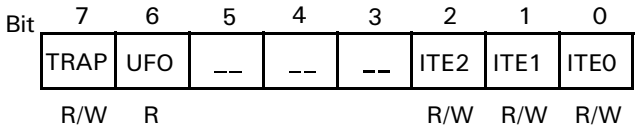
Figure 74. Interrupt Vector Low Register (IL: I/O Address = 33H)

INT/TRAP CONTROL REGISTER

This register is used in handling TRAP interrupts and to enable or disable Maskable Interrupt Level 0 and the $\overline{INT1}$ and $\overline{INT2}$ pins.

INT/TRAP Control Register

Mnemonics ITC
Address 34H



TRAP (Bit 7). This bit is set to 1 when an undefined opcode is fetched. TRAP can be reset under program control by writing it with a 0; however, TRAP cannot be written with 1 under program control. TRAP is reset to 0 during RESET.

UFO: Undefined Fetch Object (Bit 6). When a TRAP interrupt occurs, the contents of UFO allow the starting address of the undefined instruction to be determined. This interrupt is necessary because the TRAP may occur on either the second or third byte of the opcode. UFO allows the stacked PC value to be correctly adjusted. If UFO = 0, the first opcode should be interpreted as the stacked PC-1. If UFO = 1, the first opcode address is stacked PC-2. UFO is Read-Only.

ITE2, 1, 0: Interrupt Enable 2, 1, 0 (Bits 2–0). ITE2 and ITE1 enable and disable the external interrupt inputs $\overline{INT2}$ and $\overline{INT1}$, respectively. ITE0 enables and disables interrupts from:

- ESCC
- Bidirectional Centronics controller
- CTCs
- External interrupt input $\overline{INT0}$

A 1 in a bit enables the corresponding interrupt level while a 0 disables it. A RESET sets ITE0 to 1 and clears ITE1 and ITE2 to 0.

TRAP Interrupt. The Z8S180/Z8L180 generates a TRAP sequence when an undefined opcode fetch occurs. This feature can be used to increase software reliability, implement an *extended* instruction set, or both. TRAP may occur during opcode fetch cycles and also if an undefined opcode is fetched during the interrupt acknowledge cycle for $\overline{INT0}$ when Mode 0 is used.

When a TRAP sequence occurs, the Z8S180/Z8L180:

1. Sets the TRAP bit in the Interrupt TRAP/Control (ITC) register to 1.
2. Saves the current Program Counter (PC) value, reflecting the location of the undefined opcode, on the stack.
3. Resumes execution at logical address 0.

Note: If logical address 0000H is mapped to physical address 00000H, the vector is the same as for RESET. In this case, testing the TRAP bit in ITC reveals whether the restart at physical address 00000H was caused by RESET or TRAP.

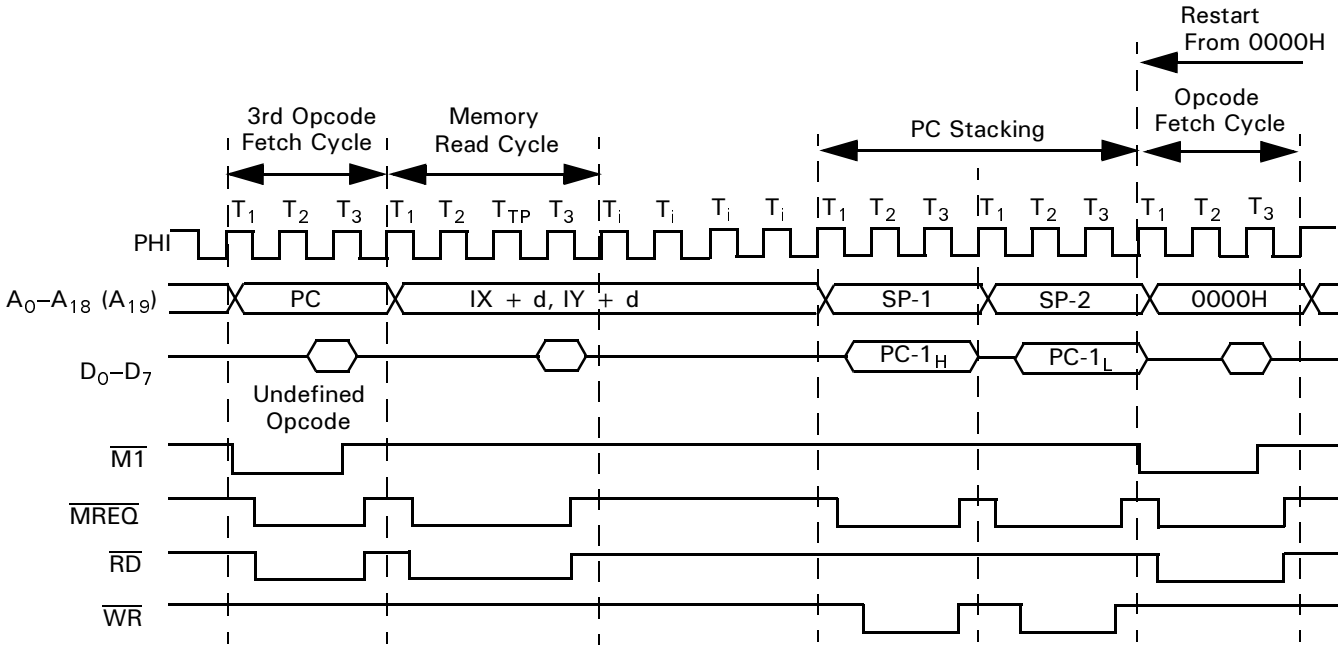


Figure 76. TRAP Timing—3rd Opcode Undefined

I/O CONTROL REGISTER

The I/O Control Register (ICR) allows relocation of the internal I/O addresses. ICR also controls the enabling and disabling of IOSTOP mode (Figure 83).

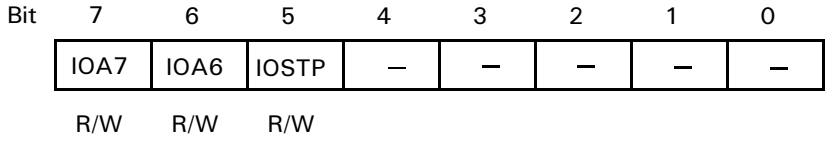


Figure 83. I/O Control Register (ICR: I/O Address = 3FH)

IOA7, 6: I/O Address Relocation (Bits 7,6). IOA7 and IOA6 relocate internal I/O as indicated in Figure 84.

Note: The high-order 8 bits of 16-bit internal I/O address are always 0. IOA7 and IOA6 are cleared to 0 during RESET.

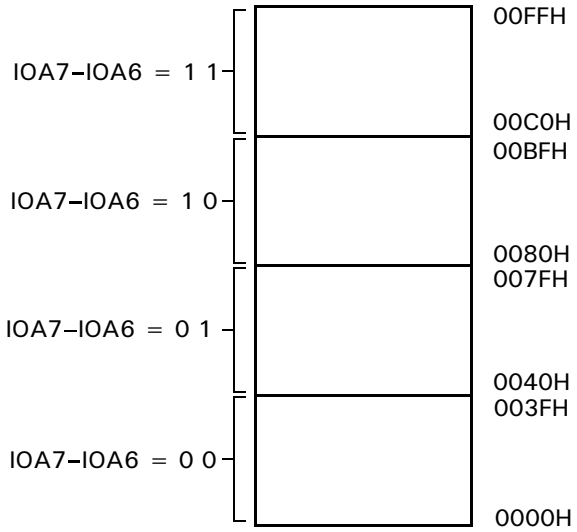


Figure 84. I/O Address Relocation

IOSTP: IOSTOP Mode (Bit 5). IOSTOP mode is enabled when IOSTP is set to 1. Normal I/O operation resumes when IOSTP is reprogrammed or RESET to 0.