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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8s18010veg

GENERAL DESCRIPTION (Continued)

Power connections follow the conventional descriptions below:

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}



Figure 1. Z8S180/Z8L180 Functional Block Diagram

PIN IDENTIFICATION (Continued)

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
1	9	8	$\overline{\text{NMI}}$		IN	IN	IN
2			NC				
3			NC				
4	10	9	$\overline{\text{INT0}}$		IN	IN	IN
5	11	10	$\overline{\text{INT1}}$		IN	IN	IN
6	12	11	$\overline{\text{INT2}}$		IN	IN	IN
7	13	12	ST		High	High	High
8	14	13	A0		3T	3T	High
9	15	14	A1		3T	3T	High
10	16	15	A2		3T	3T	High
11	17	16	A3		3T	3T	High
12	18		V _{SS}		V _{SS}	V _{SS}	V _{SS}
13	19	17	A4		3T	3T	High
14			NC				
15	20	18	A5		3T	3T	High
16	21	19	A6		3T	3T	High
17	22	20	A7		3T	3T	High
18	23	21	A8		3T	3T	High
19	24	22	A9		3T	3T	High
20	25	23	A10		3T	3T	High
21	26	24	A11		3T	3T	High
22			NC				
23			NC				
24	27	25	A12		3T	3T	High
25	28	26	A13		3T	3T	High
26	29	27	A14		3T	3T	High
27	30	28	A15		3T	3T	High
28	31	29	A16		3T	3T	High
29	32	30	A17		3T	3T	High
30			NC				
31	33	31	A18		3T	3T	High
			T _{OUT}		N/A	OUT	OUT
32	34	32	V _{DD}		V _{DD}	V _{DD}	V _{DD}
33	35		A19		3T	3T	High
34	36	33	V _{SS}		V _{SS}	V _{SS}	V _{SS}
35	37	34	D0		3T	3T	3T
36	38	35	D1		3T	3T	3T
37	39	36	D2		3T	3T	3T
38	40	37	D3		3T	3T	3T

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)

Pin Number and Package Type			Pin Status				
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
39	41	38	D4		3T	3T	3T
40	42	39	D5		3T	3T	3T
41	43	40	D6		3T	3T	3T
42			NC				
43			NC				
44	44	41	D7		3T	3T	3T
45	45	42	$\overline{\text{RTS0}}$		High	OUT	High
46	46	43	$\overline{\text{CTS0}}$		IN	OUT	IN
47	47	44	$\overline{\text{DCD0}}$		IN	IN	IN
48	48	45	TXA0		High	OUT	OUT
49	49	46	RXA0		IN	IN	IN
50	50	47	CKA0		3T	I/O	I/O
			$\overline{\text{DREQ0}}$		N/A	IN	IN
51			NC				
52	51	48	TXA1		High	OUT	OUT
53	52		TEST				
54	53	49	RXA1		IN	IN	IN
55	54	50	CKA1		3T	I/O	I/O
			$\overline{\text{TEND0}}$		N/A	High	High
56	55	51	TXS		High	OUT	OUT
57	56	52	RXS		IN	IN	IN
			$\overline{\text{CTS1}}$		N/A	IN	IN
58	57	53	CKS		3T	I/O	I/O
59	58	54	$\overline{\text{DREQ1}}$		IN	3T	IN
60	59	55	$\overline{\text{TEND1}}$		High	OUT	High
61	60	56	$\overline{\text{HALT}}$		High	High	Low
62			NC				
63			NC				
64	61	57	$\overline{\text{RFSH}}$		High	OUT	High
65	62	58	$\overline{\text{IORQ}}$		High	3T	High
66	63	59	$\overline{\text{MREQ}}$		High	3T	High
67	64	60	E		Low	OUT	OUT
68	65	61	$\overline{\text{M1}}$		High	High	High
69	66	62	$\overline{\text{WR}}$		High	3T	High
70	67	63	$\overline{\text{RD}}$		High	3T	High
71	68	64	PHI		OUT	OUT	OUT
72	1	1	V _{SS}		GND	GND	GND
73	2		V _{SS}		GND	GND	GND
74	3	2	XTAL		OUT	OUT	OUT
75			NC				

Table 4. Multiplexed Pin Descriptions

A18/TOUT	During RESET, this pin is initialized as A18. If either the TOC1 or the TOC0 bit of the Timer Control register (TCR) is set to 1, the T _{OUT} function is selected. If TOC1 and TOC0 are cleared to 0, the A18 function is selected.
CKA0/ $\overline{\text{DREQ0}}$	During RESET, this pin is initialized as CKA0. If either DM1 or SM1 in the DMA Mode register (DMODE) is set to 1, the $\overline{\text{DREQ0}}$ function is selected.
CKA1/ $\overline{\text{TEND0}}$	During RESET, this pin is initialized as CKA1. If the CKA1D bit in ASCI control register ch1 (CNTLA1) is set to 1, the $\overline{\text{TEND0}}$ function is selected. If the CKA1D bit is set to 0, the CKA1 function is selected.
RXS/ $\overline{\text{CTS1}}$	During RESET, this pin is initialized as RXS. If the CTS1E bit in the ASCI status register ch1 (STAT1) is set to 1, the $\overline{\text{CTS1}}$ function is selected. If the CTS1E bit is set to 0, the RXS function is selected.

OPERATION MODES (Continued)



Figure 15. Z8S180/Z8L180 IDLE Mode Exit Due To External Interrupt

While the Z8S180/Z8L180 is in IDLE mode, it grants the bus to an external Master if the BREXT bit (CCR5) is 1. Figure 16 depicts the timing for this sequence.

After the external Master negates the Bus Request, the Z8S180/Z8L180 disables the PHI clock and remains in IDLE mode.

Note: A response to a bus request takes 8 clock cycles longer than in normal operation.

ing the bus to an external Master during STANDBY mode, when the BREXT bit in the CPU Control Register (CCR5) is 1.

As described previously for SLEEP and IDLE modes, when the MPU leaves STANDBY mode due to $\overline{\text{NMI}}$ Low or an enabled $\overline{\text{INT0}}\text{--}\overline{\text{INT2}}$ Low when the IEF, flag is 1 due to an IE instruction, it starts by performing the interrupt with the return address being that of the instruction following the SLP instruction. If the Z8S180/Z8L180 leaves STANDBY mode due to an external interrupt request that's enabled in the INT/TRAP Control Register, but the IEF, bit is 0 due to

a DI instruction, the processor restarts by executing the instruction(s) following the SLP instruction. If $\overline{\text{INT0}}$, or $\overline{\text{INT1}}$ or $\overline{\text{INT2}}$ goes inactive before the end of the clock stabilization delay, the Z8S180/Z8L180 stays in STANDBY mode.

Figure 17 indicates the timing for leaving STANDBY mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes either 64 or 2^{17} (131,072) clocks to restart, depending on the CCR3 bit.

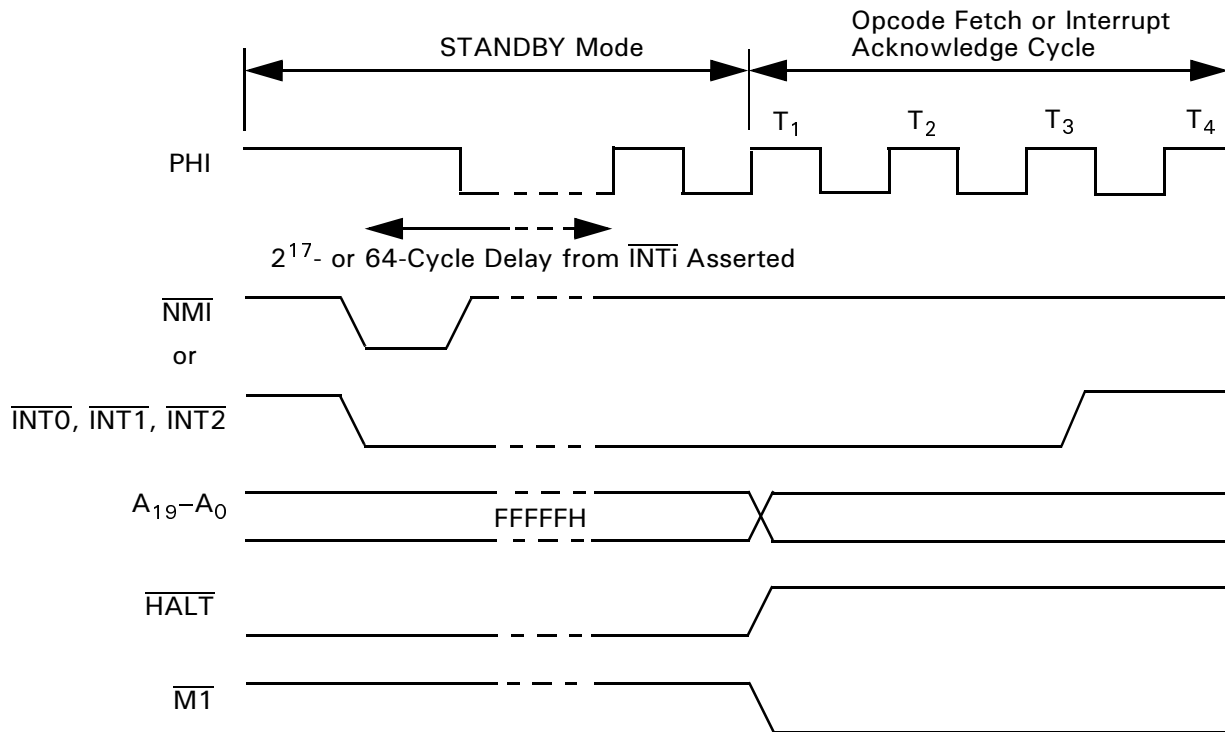


Figure 17. Z8S180/Z8L180 STANDBY Mode Exit Due to External Interrupt

While the Z8S180/Z8L180 is in STANDBY mode, it grants the bus to an external Master if the BREXT bit (CCR5) is 1. Figure 18 indicates the timing of this sequence. The device takes 64 or 2^{17} (131,072) clock cycles to grant the bus de-

pending on the CCR3 bit. The latter (not the QUICK RECOVERY) case may be prohibitive for many demand-driven external Masters. If so, QUICK RECOVERY or IDLE mode can be used.

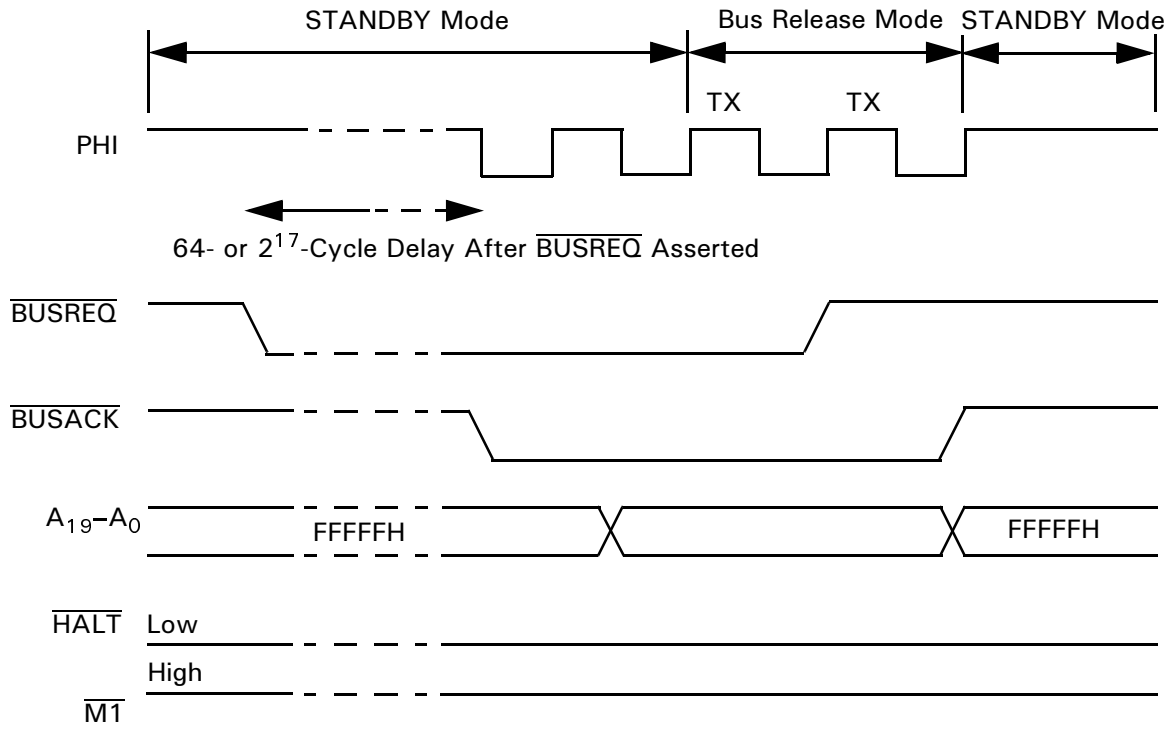


Figure 18. Bus Granting to External Master During STANDBY Mode

STANDARD TEST CONDITIONS

The following standard test conditions apply to [DC Characteristics](#), unless otherwise noted. All voltages are referenced to V_{SS} (0V). Positive current flows into the referenced pin.

All AC parameters assume a load capacitance of 100 pF. Add a 10-ns delay for each 50-pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to $V_{OL\ MAX}$ or $V_{OL\ MIN}$ as indicated in Figures 20 through 30 (except for CLOCK, which is referenced to the 10% and 90% points). [Ordering Information](#) lists temperature ranges and product numbers. Find package drawings in [Package Information](#).

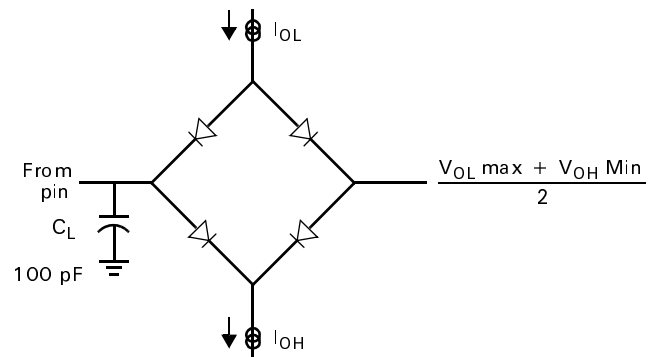


Figure 19. AC Parameter Test Circuit

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 ~ +7.0	V
Input Voltage	V_{IN}	-0.3 ~ $V_{CC} + 0.3$	V
Operating Temperature	T_{OPR}	0 ~ 70	°C
Extended Temperature	T_{EXT}	-40 ~ 85	°C
Storage Temperature	T_{STG}	-55 ~ +150	°C

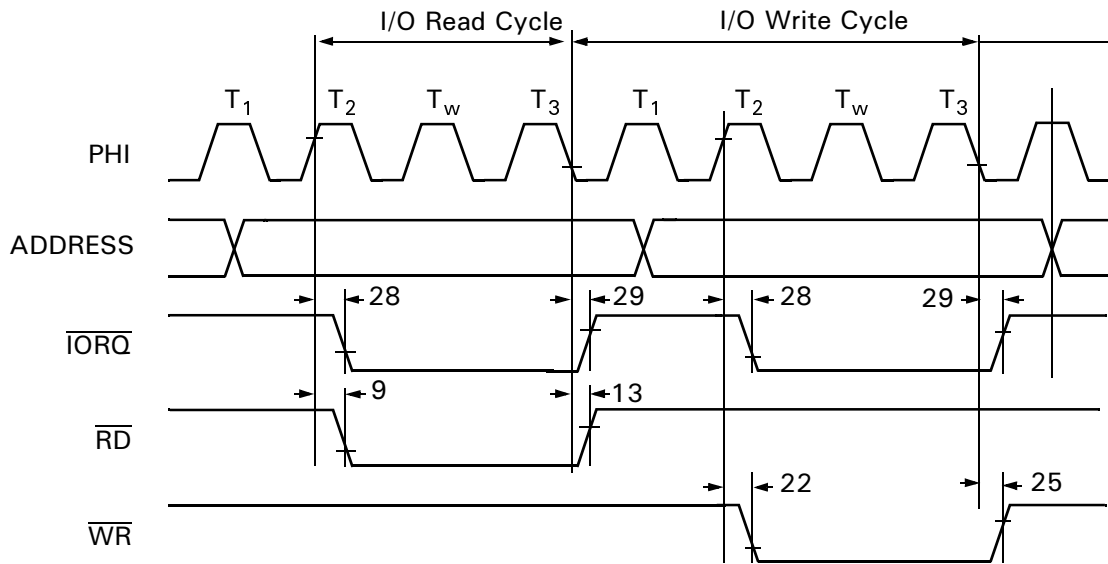
Note: Permanent damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability.

AC CHARACTERISTICS—Z8S180 (Continued)

Table 8. Z8S180 AC Characteristics (Continued)
 $V_{DD} = 5V \pm 10\%$ or $V_{DD} = 3.3V \pm 10\%$; 33-MHz Characteristics Apply Only to 5V Operation

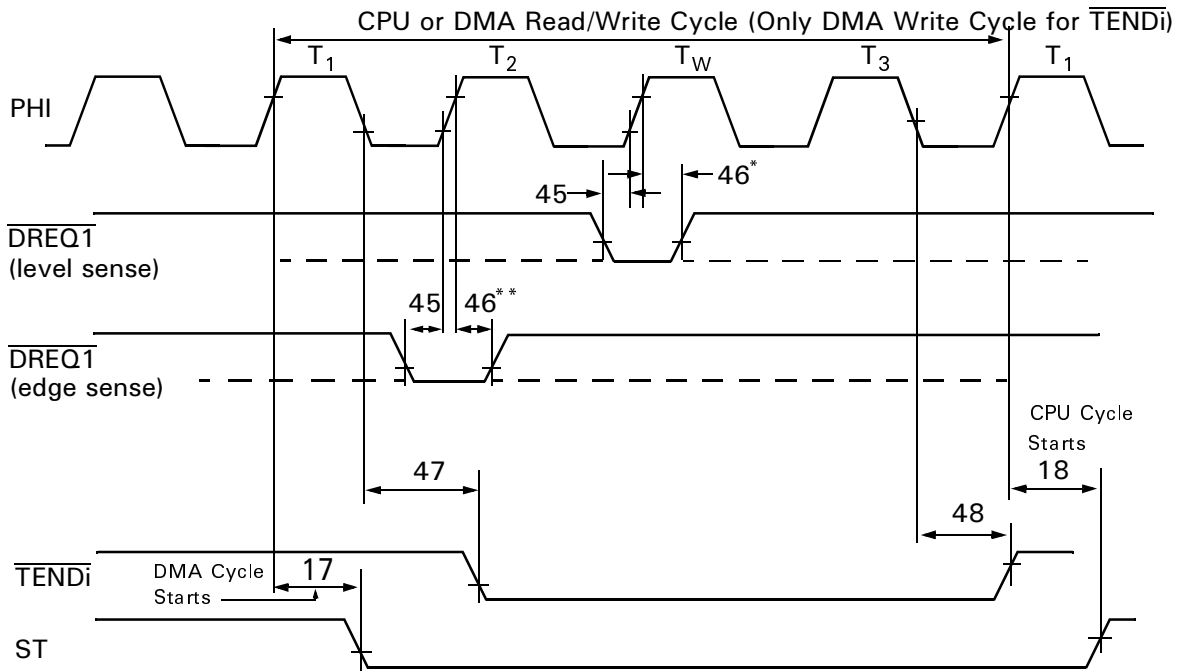
Number	Symbol	Item	Z8S180—20 MHz		Z8S180—33 MHz		Unit
			Min	Max	Min	Max	
32	t_{INTH}	\overline{INT} Hold Time from PHI Fall	10	—	10	—	ns
33	t_{NMIW}	\overline{NMI} Pulse Width	35	—	25	—	ns
34	t_{BRS}	\overline{BUSREQ} Set-up Time to PHI Fall	10	—	10	—	ns
35	t_{BRH}	\overline{BUSREQ} Hold Time from PHI Fall	10	—	10	—	ns
36	t_{BAD1}	PHI Rise to \overline{BUSACK} Fall Delay	—	25	—	15	ns
37	t_{BAD2}	PHI Fall to \overline{BUSACK} Rise Delay	—	25	—	15	ns
38	t_{BZD}	PHI Rise to Bus Floating Delay Time	—	40	—	30	ns
39	t_{MEWH}	\overline{MREQ} Pulse Width (High)	35	—	25	—	ns
40	t_{MEWL}	\overline{MREQ} Pulse Width (Low)	35	—	25	—	ns
41	t_{RFD1}	PHI Rise to \overline{RFSH} Fall Delay	—	20	—	15	ns
42	t_{RFD2}	PHI Rise to \overline{RFSH} Rise Delay	—	20	—	15	ns
43	t_{HAD1}	PHI Rise to \overline{HALT} Fall Delay	—	15	—	15	ns
44	t_{HAD2}	PHI Rise to \overline{HALT} Rise Delay	—	15	—	15	ns
45	t_{DROS}	$\overline{DREQ1}$ Set-up Time to PHI Rise	20	—	15	—	ns
46	t_{DROH}	$\overline{DREQ1}$ Hold Time from PHI Rise	20	—	15	—	ns
47	t_{TED1}	PHI Fall to \overline{TENDi} Fall Delay	—	25	—	15	ns
48	t_{TED2}	PHI Fall to \overline{TENDi} Rise Delay	—	25	—	15	ns
49	t_{ED1}	PHI Rise to E Rise Delay	—	30	—	15	ns
50	t_{ED2}	PHI Fall or Rise to E Fall Delay	—	30	—	15	ns
51	P_{WEH}	E Pulse Width (High)	25	—	20	—	ns
52	P_{WEL}	E Pulse Width (Low)	50	—	40	—	ns
53	t_{Er}	Enable Rise Time	—	10	—	10	ns
54	t_{Ef}	Enable Fall Time	—	10	—	10	ns
55	t_{TOD}	PHI Fall to Timer Output Delay	—	75	—	50	ns
56	t_{STDI}	CSI/O Transmit Data Delay Time (Internal Clock Operation)	—	2	—	2	tcyc
57	t_{STDE}	CSI/O Transmit Data Delay Time (External Clock Operation)	—	$7.5 t_{CYC} + 75$	—	$75 t_{CYC} + 60$	ns
58	t_{SRSI}	CSI/O Receive Data Set-up Time (Internal Clock Operation)	1	—	1	—	tcyc
59	t_{SRHI}	CSI/O Receive Data Hold Time (Internal Clock Operation)	1	—	1	—	tcyc
60	t_{SRSE}	CSI/O Receive Data Set-up Time (External Clock Operation)	1	—	1	—	tcyc
61	t_{SRHE}	CSI/O Receive Data Hold Time (External Clock Operation)	1	—	1	—	tcyc
62	t_{RES}	\overline{RESET} Set-up Time to PHI Fall	40	—	25	—	ns

TIMING DIAGRAMS (Continued)



$$\text{CPU Timing } (\overline{\text{IOC}} = 0) = \begin{cases} \text{I/O Read Cycle} \\ \text{I/O Write Cycle} \end{cases}$$

Figure 22. CPU Timing ($\overline{\text{IOC}} = 0$)
(I/O Read Cycle, I/O Write Cycle)



Notes:

- * T_{DROS} and T_{DRQH} are specified for the rising edge of the clock followed by T_3 .
- ** T_{DROS} and T_{DRQH} are specified for the rising edge of the clock.

Figure 23. DMA Control Signals

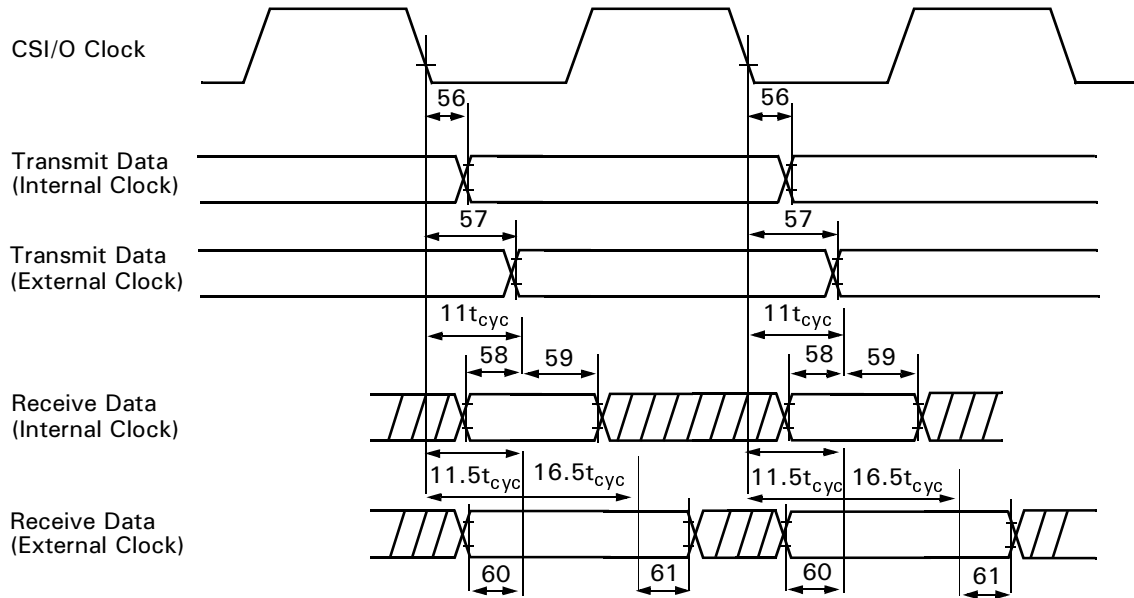


Figure 29. CSI/O Receive/Transmit Timing



Figure 30. Rise Time and Fall Times

Data can be written into and read from the ASCII Transmit Data Register. If data is read from the ASCII Transmit Data Register, the ASCII data transmit operation is not affected by this READ operation.

ASCII Receive Shift Register 0,1 (RSR0,1). This register receives data shifted in on the RXA pin. When full, data is automatically transferred to the ASCII Receive Data Register (RDR) if it is empty. If RSR is not empty when the next incoming data byte is shifted in, an overrun error occurs. This register is not program accessible.

ASCII Receive Data FIFO 0,1 (RDR0, 1:I/O Address = 08H, 09H). The ASCII Receive Data Register is a read-only register. When a complete incoming data byte is assembled in RSR, it is automatically transferred to the 4 character Receive Data First-In First-Out (FIFO) memory. The oldest character in the FIFO (if any) can be read from the Receive Data Register (RDR). The next incoming data byte can be shifted into RSR while the FIFO is full. Thus, the ASCII receiver is well buffered.

ASCII STATUS FIFO

This four-entry FIFO contains Parity Error, Framing Error, Rx Overrun, and Break status bits associated with each character in the receive data FIFO. The status of the oldest character (if any) can be read from the ASCII status registers.

acter in the receive data FIFO. The status of the oldest character (if any) can be read from the ASCII status registers.

ASCII CHANNEL CONTROL REGISTER A

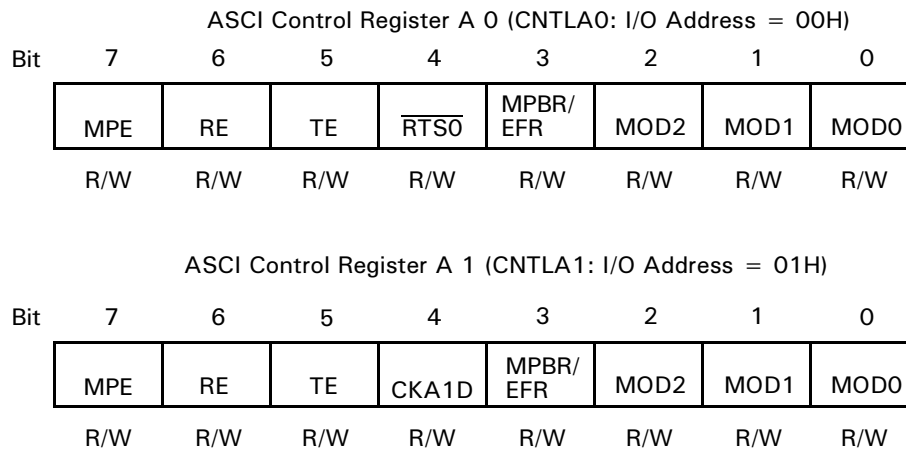


Figure 33. ASCII Channel Control Register A

MPE: Multi-Processor Mode Enable (Bit 7). The ASCII features a multiprocessor communication mode that utilizes an extra data bit for selective communication when a number of processors share a common serial bus. Multiprocessor data format is selected when the MP bit in CNTLB is set to 1. If multiprocessor mode is not selected (MP bit in CNTLB = 0), MPE has no effect. If multiprocessor mode is selected, MPE enables or disables the *wake-up* feature as follows. If MBE is set to 1, only received bytes in which the multiprocessor bit (MPB) = 1 can affect the RDRF and error flags. Effectively, other bytes (with MPB = 0) are *ignored* by the ASCII. If MPE is reset to 0, all bytes, regardless of

the state of the MPB data bit, affect the REDR and error flags. MPE is cleared to 0 during RESET.

RE: Receiver Enable (Bit 6). When RE is set to 1, the ASCII transmitter is enabled. When RE is reset to 0, the transmitter is disabled and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the previous contents of TDRE are held. TE is cleared to 0 in IOSTOP mode during RESET.

TE: Transmitter Enable (Bit 5). When TE is set to 1, the ASCII receiver is enabled. When $\overline{\text{TE}}$ is reset to 0, the transmitter is disabled and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the pre-

ASCII CHANNEL CONTROL REGISTER A (Continued)

vious contents of TDRE are held. TE is cleared to 0 in IOSTOP mode during RESET.

RTS0: Request to Send Channel 0 (Bit 4 in CNTLA0 Only). If bit 4 of the System Configuration Register is 0, the $\overline{\text{RTS0}}$ /TXS pin exhibits the $\overline{\text{RTS0}}$ function. $\overline{\text{RTS0}}$ allows the ASCII to control (start/stop) another communication devices transmission (for example, by connecting to that device's $\overline{\text{CTS}}$ input). $\overline{\text{RTS0}}$ is essentially a 1-bit output port, having no side effects on other ASCII registers or flags.

Bit 4 in CNTLA1 is used.

$$\text{CKA1D} = 1, \text{CKA1}/\overline{\text{TEND0}} \text{ pin} = \overline{\text{TEND0}}$$

$$\text{CKA1D} = 0, \text{CKA1}/\overline{\text{TEND0}} \text{ pin} = \text{CKA1}$$

These bits are cleared to 0 on reset.

MPBR/EFR: Multiprocessor Bit Receive/Error Flag Reset (Bit 3). When multiprocessor mode is enabled (MP in CNTLB = 1), MPBR, when read, contains the value of the MPB bit for the most recent receive operation. When written to 0, the EFR function is selected to reset all error flags (OVRN, FE, PE and BRK in the ASEXT Register) to 0. MPBR/EFR is undefined during RESET.

MOD2, 1, 0: ASCII Data Format Mode 2,1,0 (bits 2–0).

These bits program the ASCII data format as follows.

MOD2

= 0→7 bit data

= 1→8 bit data

MOD1

= 0→No parity

= 1→Parity enabled

MOD0

= 0→1 stop bit

= 1→2 stop bits

The data formats available based on all combinations of MOD2, MOD1, and MOD0 are indicated in Table 9.

Table 9. Data Formats

MOD2	MOD1	MOD0	Data Format
0	0	0	Start + 7 bit data + 1 stop
0	0	1	Start + 7 bit data + 2 stop
0	1	0	Start + 7 bit data + parity + 1 stop
0	1	1	Start + 7 bit data + parity + 2 stop
1	0	0	Start + 8 bit data + 1 stop
1	0	1	Start + 8 bit data + 2 stop
1	1	0	Start + 8 bit data + parity + 1 stop
1	1	1	Start + 8 bit data + parity + 2 stop

ASCII CHANNEL CONTROL REGISTER B

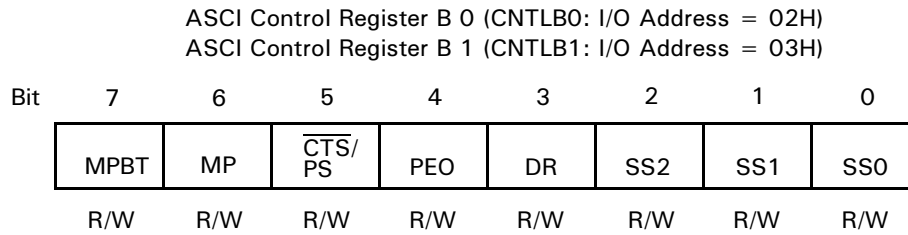


Figure 34. ASCII Channel Control Register B

MPBT: Multiprocessor Bit Transmit (Bit 7). When multiprocessor communication format is selected (MP bit = 1), MPBT is used to specify the MPB data bit for transmission. If MPBT = 1, then MPB = 1 is transmitted. If MPBT = 0, then MPB = 0 is transmitted. The MPBT state is undefined during and after RESET.

MP: Multiprocessor Mode (Bit 6). When MP is set to 1, the data format is configured for multiprocessor mode based on MOD2 (number of data bits) and MODO (number of stop bits) in CNTLA. The format is as follows:

Start bit + 7 or 8 data bits + MPB bit + 1 or 2 stop bits

Multiprocessor (MP = 1) format offers no provision for parity. If MP = 0, the data format is based on MODO, MOD1, MOD2, and may include parity. The MP bit is cleared to 0 during RESET.

$\overline{\text{CTS}}/\text{PS}$: Clear to Send/Prescale (Bit 5). When read, $\overline{\text{CTS}}/\text{PS}$ reflects the state of the external $\overline{\text{CTS}}$ input. If the $\overline{\text{CTS}}$ input pin is High, $\overline{\text{CTS}}/\text{PS}$ is read as 1.

Note: When the $\overline{\text{CTS}}$ input pin is High, the TDRE bit is inhibited (that is, held at 0).

For channel 1, the $\overline{\text{CTS}}$ input is multiplexed with RXS pin (Clocked Serial Receive Data). Thus, $\overline{\text{CTS}}/\text{PS}$ is only valid when read if the channel 1 CTS1E bit = 1 and the $\overline{\text{CTS}}$ input pin function is selected. The READ data of $\overline{\text{CTS}}/\text{PS}$ is not affected by $\overline{\text{RESET}}$.

If the SS2–0 bits in this register are not 111, and the BRG mode bit in the ASEXT register is 0, then writing to this bit sets the prescale (PS) control. Under those circumstances, a 0 indicates a divide-by-10 prescale function while a 1 indicates divide-by-30. The bit resets to 0.

PEO: Parity Even Odd (Bit 4). PEO selects even or odd parity. PEO does not affect the enabling/disabling of parity (MOD1 bit of CNTLA). If PEO is cleared to 0, even parity is selected. If PEO is set to 1, odd parity is selected. PEO is cleared to 0 during RESET.

DR: Divide Ratio (Bit 3). If the X1 bit in the ASEXT register is 0, this bit specifies the divider used to obtain baud rate from the data sampling clock. If DR is reset to 0, divide-by-16 is used, while if DR is set to 1, divide-by-64 is used. DR is cleared to 0 during RESET.

SS2,1,0: Source/Speed Select 2,1,0 (Bits 2–0). First, if these bits are 111, as they are after a RESET, the CKA pin is used as a clock input, and is divided by 1, 16, or 64 depending on the DR bit and the X1 bit in the ASEXT register.

If these bits are not 111 and the BRG mode bit is ASEXT is 0, then these bits specify a power-of-two divider for the PHI clock as indicated in Table 10.

Setting or leaving these bits as 111 makes sense for a channel only when its CKA pin is selected for the CKA function. CKA0/CKS offers the CKA0 function when bit 4 of the System Configuration Register is 0. $\overline{\text{DCD0}}/\text{CKA1}$ offers the CKA1 function when bit 0 of the Interrupt Edge register is 1.

Table 10. Divide Ratio

SS2	SS1	SS0	Divide Ratio
0	0	0	÷1
0	0	1	÷2
0	1	0	÷4
0	1	1	÷8
1	0	0	÷16
1	0	1	÷32
1	1	0	÷64
1	1	1	External Clock

ASCII STATUS REGISTER 0,1

Each ASCII channel status register (STAT0,1) allows interrogation of ASCII communication, error and modem control

signal status, and the enabling or disabling of ASCII interrupts.

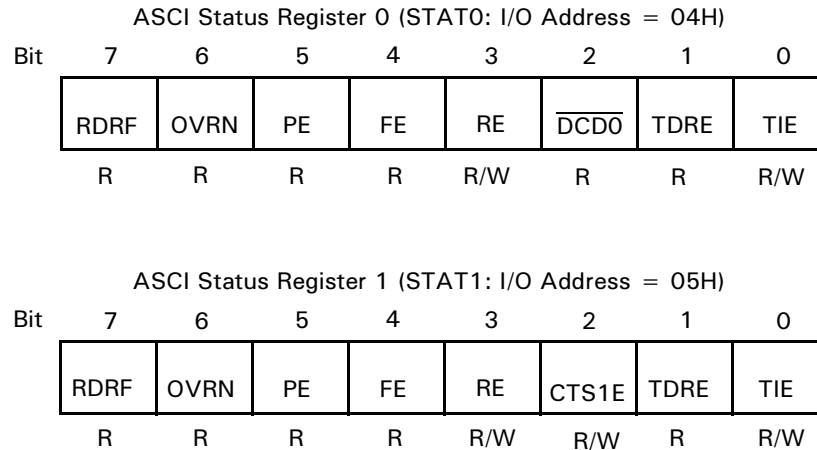


Figure 35. ASCII Status Registers

RDRF: Receive Data Register Full (Bit 7). RDRF is set to 1 when an incoming data byte is loaded into an empty Rx FIFO. If a framing or parity error occurs, RDRF is still set and the receive data (which generated the error) is still loaded into the FIFO. RDRF is cleared to 0 by reading RDR and most recently received character in the FIFO from IOSTOP mode, during RESET and for ASCII0 if the $\overline{\text{DCD0}}$ input is auto-enabled and is negated (High).

OVRN: Overrun Error (Bit 6). An overrun condition occurs if the receiver finishes assembling a character but the Rx FIFO is full so there is no room for the character. However, this status bit is not set until the most recent character received before the overrun becomes the oldest byte in the FIFO. This bit is cleared when software writes a 1 to the EFR bit in the CNTLA register. The bit may also be cleared by RESET in IOSTOP mode or ASCII0 if the $\overline{\text{DCD0}}$ pin is auto enabled and is negated (High).

Note: When an overrun occurs, the receiver does not place the character in the shift register into the FIFO, nor any subsequent characters, until the most recent good character enters the top of the FIFO so that OVRN is set. Software then writes a 1 to EFR to clear it.

PE: Parity Error (Bit 5). A parity error is detected when parity checking is enabled. When the MOD1 bit in the

CNTLA register is 1, a character is assembled in which the parity does not match the PEO bit in the CNTLB register. However, this status bit is not set until or unless the error character becomes the oldest one in the Rx FIFO. PE is cleared when software writes a 1 to the EFR bit in the CNTRLA register. PE is also cleared by RESET in IOSTOP mode, or on ASCII0, if the $\overline{\text{DCD0}}$ pin is auto-enabled and is negated (High).

FE: Framing Error (Bit 4). A framing error is detected when the stop bit of a character is sampled as 0/SPACE. However, this status bit is not set until/unless the error character becomes the oldest one in the Rx FIFO. FE is cleared when software writes a 1 to the EFR bit in the CNTLA register. FE is also cleared by RESET in IOSTOP mode, or on ASCII0, if the $\overline{\text{DCD0}}$ pin is auto-enabled and is negated (High).

REI: Receive Interrupt Enable (Bit 3). RIE should be set to 1 to enable ASCII receive interrupt requests. When RIE is 1, the Receiver requests an interrupt when a character is received and RDRF is set, but only if neither DMA channel requires its request-routing field to be set to receive data from this ASCII. That is, if SM1-0 are 11 and SAR17-16 are 10, or DIM1 is 1 and IAR17-16 are 10, then ASCII1 does not request an interrupt for RDRF. If RIE is 1, either ASCII requests an interrupt when OVRN, PE or FE is set, and

TIMER CONTROL REGISTER

The Timer Control Register (TCR) monitors both channels (PRT0, PRT1) TMDR status. It also controls the enabling

and disabling of down-counting and interrupts, and controls the output pin A18/T_{OUT} for PRT1.

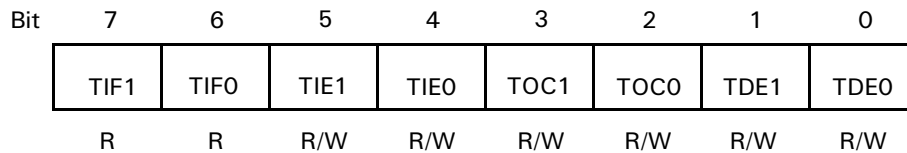


Figure 46. Timer Control Register (TCR: I/O Address = 10H)

TIF1: Timer Interrupt Flag 1 (Bit 7) . When TMDR1 decrements to 0, TIF1 is set to 1. This condition generates an interrupt request if enabled by TIE1 = 1. TIF1 is reset to 0 when TCR is read and the higher or lower byte of TMDR1 is read. During RESET, TIF1 is cleared to 0.

TIFO: Timer Interrupt Flag 0 (Bit 6). When TMDR0 decrements to 0, TIFO is set to 1. This condition generates an interrupt request if enabled by TIE0 = 1. TIFO is reset to 0 when TCR is read and the higher or lower byte of TMDR0 is read. During RESET, TIFO is cleared to 0.

TIE1: Timer Interrupt Enable 1 (Bit 5). When TIE0 is set to 1, TIF1 = 1 generates a CPU interrupt request. When TIE0 is reset to 0, the interrupt request is inhibited. During RESET, TIE0 is cleared to 0.

TOC1, 0: Timer Output Control (Bits 3, 2). TOC1 and TOC0 control the output of PRT1 using the multiplexed A18/T_{OUT} pin as indicated in Table 12. During RESET, TOC1 and TOC0 are cleared to 0. If bit 3 of the IAR1B register is 1, the T_{OUT} function is selected. By programming

TOC1 and TOC0, the A18/T_{OUT} pin can be forced High, Low, or toggled when TMDR1 decrements to 0.

Table 12. Timer Output Control

TOC1	TOC0	Output
0	0	Inhibited
0	1	Toggled
1	0	0
1	1	1

The A18/T_{OUT} pin is not affected by the PRT

If bit 3 of IAR1B is 1, the A18/T_{OUT} pin is toggled or set Low or High as indicated

TDE1, 0: Timer Down Count Enable (Bits 1, 0). TDE1 and TDE0 enable and disable down-counting for TMDR1 and TMDR0, respectively. When TDE_n (n = 0,1) is set to 1, down-counting is stopped and TMDR_n is freely read or written. TDE1 and TDE0 are cleared to 0 during RESET and TMDR_n does not decrement until TDE_n is set to 1.

DMA MEMORY ADDRESS REGISTER CHANNEL 1

The DMA Memory Address Register Channel 1 specifies the physical memory address for channel 1 transfers. The address may be a destination or a source memory location. The register contains 20 bits and may specify up to 1024 KB memory addresses.

DMA Memory Address Register, Channel 1L

Mnemonic MAR1L
Address 28H



Figure 65. DMA Memory Address Register, Channel 1L

DMA Memory Address Register, Channel 1H

Mnemonic MAR1H
Address 29H



Figure 66. DMA Memory Address Register, Channel 1H

DMA Memory Address Register, Channel 1B

Mnemonic MAR1B
Address 2AH

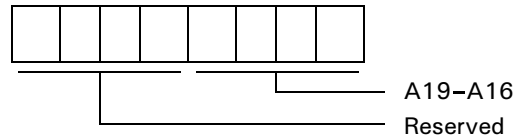


Figure 67. DMA Memory Address Register, Channel 1B

MMU COMMON BASE REGISTER

The Common Base Register (CBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical

address for Common Area 1 accesses. All bits of CBR are reset to 0 during RESET.

MMU Common Base Register

Mnemonic CBR
Address 38H

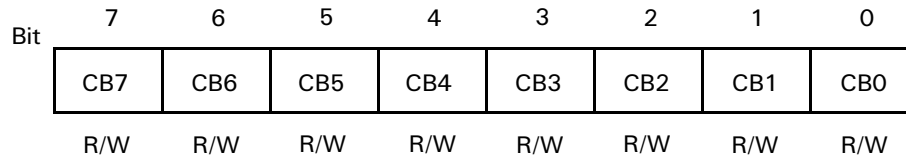


Figure 78. MMU Common Base Register (CBR: I/O Address = 38H)

MMU BANK BASE REGISTER

The Bank Base Register (BBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical ad-

dress for Bank Area accesses. All bits of BBR are reset to 0 during RESET.

MMU Bank Base Register

Mnemonic BBR
Address 39H

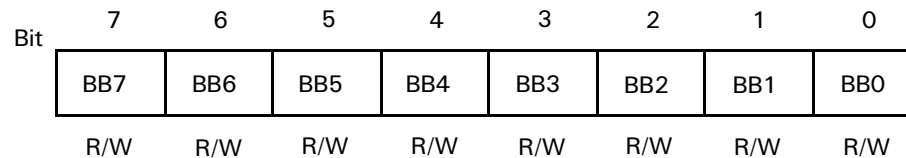


Figure 79. MMU Bank Base Register (BBR: I/O Address = 39H)

MMU COMMON/BANK AREA REGISTER

The Common/Bank Area Register (CBAR) specifies boundaries within the Z8S180/Z8L180 64-KB logical address

space for up to three areas; Common Area), Bank Area and Common Area 1.

MMU Common/Bank Area Register

Mnemonic CBAR
Address 3AH

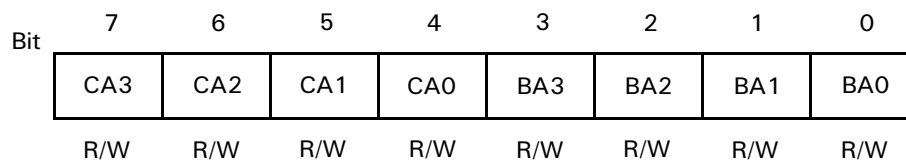


Figure 80. MMU Common/Bank Area Register (CBAR: I/O Address = 3AH)

PACKAGE INFORMATION

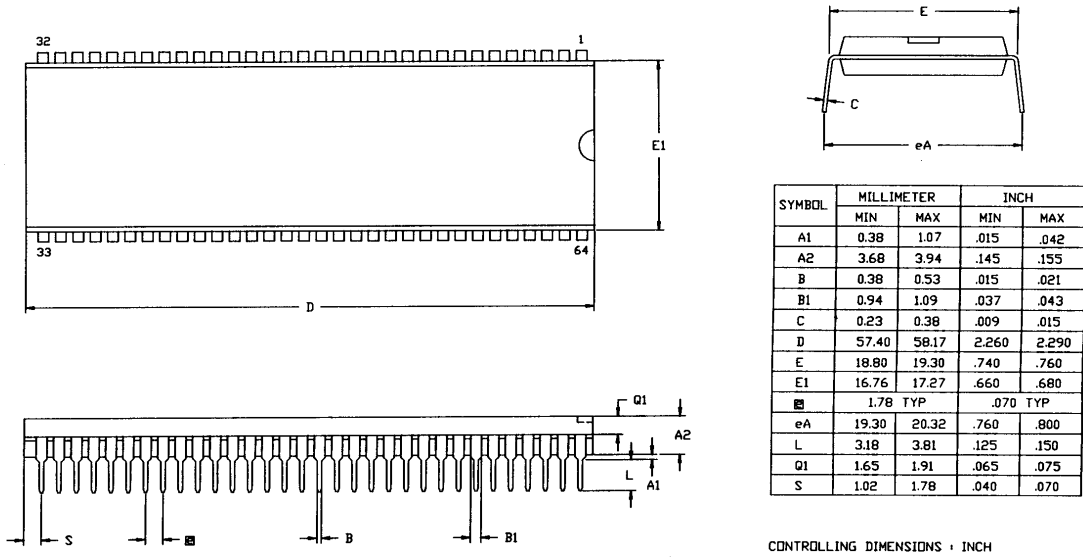


Figure 85. 64-Pin DIP Package Diagram

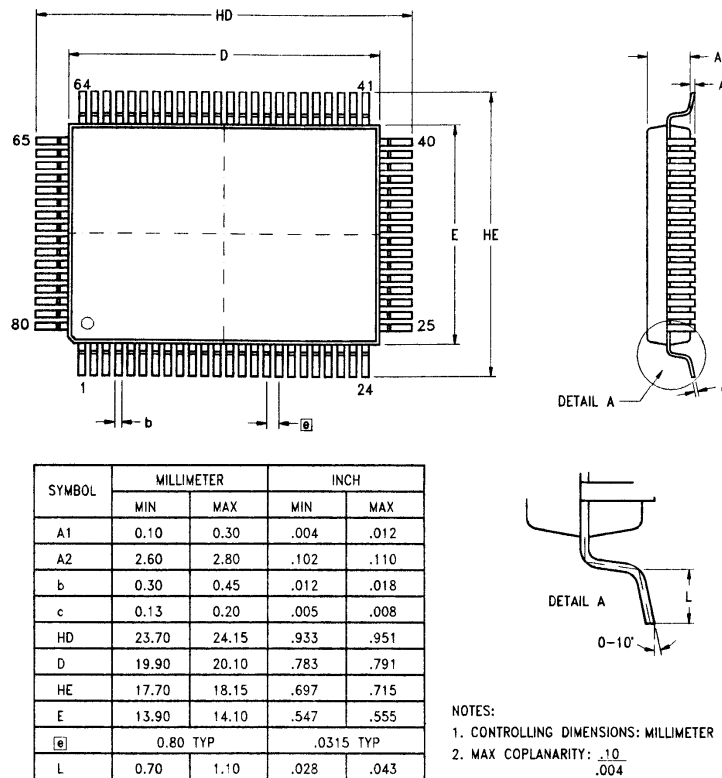


Figure 86. 80-Pin QFP Package Diagram

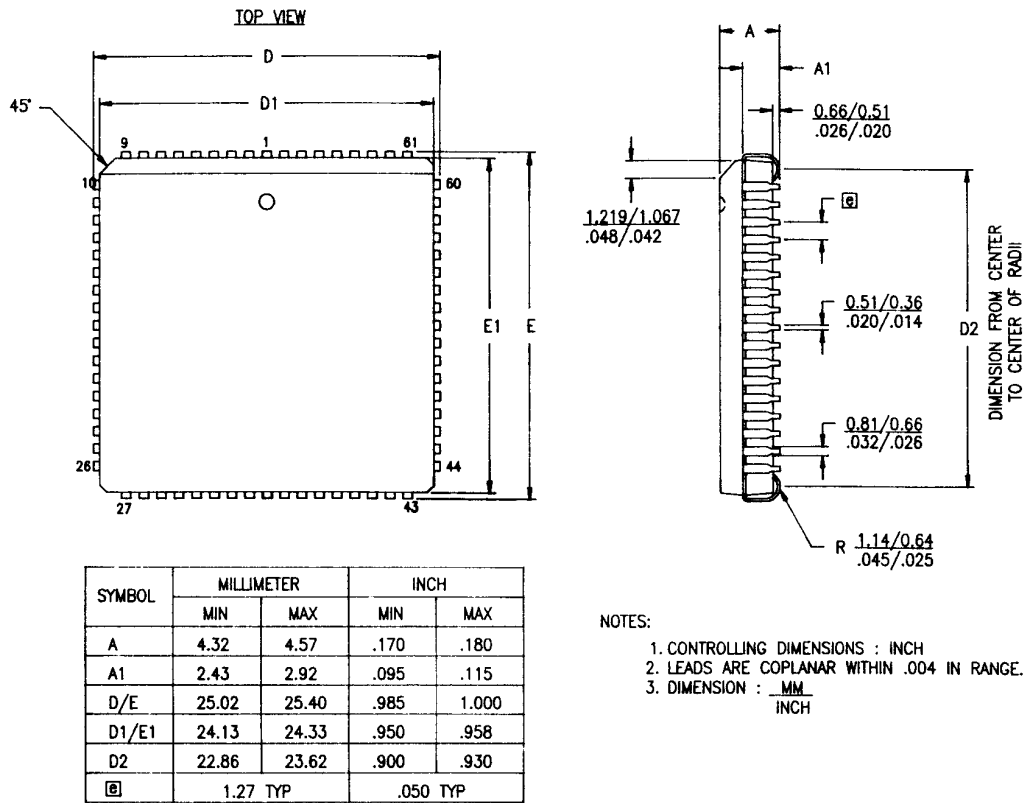


Figure 87. 68-Pin PLCC Package Diagram