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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	10MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8s18010vsc

PIN IDENTIFICATION (Continued)

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
1	9	8	$\overline{NMI}$		IN	IN	IN
2			NC				
3			NC				
4	10	9	$\overline{INT0}$		IN	IN	IN
5	11	10	$\overline{INT1}$		IN	IN	IN
6	12	11	$\overline{INT2}$		IN	IN	IN
7	13	12	ST		High	High	High
8	14	13	A0		3T	3T	High
9	15	14	A1		3T	3T	High
10	16	15	A2		3T	3T	High
11	17	16	A3		3T	3T	High
12	18		V_{SS}		V_{SS}	V_{SS}	V_{SS}
13	19	17	A4		3T	3T	High
14			NC				
15	20	18	A5		3T	3T	High
16	21	19	A6		3T	3T	High
17	22	20	A7		3T	3T	High
18	23	21	A8		3T	3T	High
19	24	22	A9		3T	3T	High
20	25	23	A10		3T	3T	High
21	26	24	A11		3T	3T	High
22			NC				
23			NC				
24	27	25	A12		3T	3T	High
25	28	26	A13		3T	3T	High
26	29	27	A14		3T	3T	High
27	30	28	A15		3T	3T	High
28	31	29	A16		3T	3T	High
29	32	30	A17		3T	3T	High
30			NC				
31	33	31	A18		3T	3T	High
			T_{OUT}		N/A	OUT	OUT
32	34	32	V_{DD}		V_{DD}	V_{DD}	V_{DD}
33	35		A19		3T	3T	High
34	36	33	V_{SS}		V_{SS}	V_{SS}	V_{SS}
35	37	34	D0		3T	3T	3T
36	38	35	D1		3T	3T	3T
37	39	36	D2		3T	3T	3T
38	40	37	D3		3T	3T	3T

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
39	41	38	D4		3T	3T	3T
40	42	39	D5		3T	3T	3T
41	43	40	D6		3T	3T	3T
42			NC				
43			NC				
44	44	41	D7		3T	3T	3T
45	45	42	$\overline{RTS0}$		High	OUT	High
46	46	43	$\overline{CTS0}$		IN	OUT	IN
47	47	44	$\overline{DCD0}$		IN	IN	IN
48	48	45	TXA0		High	OUT	OUT
49	49	46	RXA0		IN	IN	IN
50	50	47	CKA0		3T	I/O	I/O
			$\overline{DREQ0}$		N/A	IN	IN
51			NC				
52	51	48	TXA1		High	OUT	OUT
53	52		TEST				
54	53	49	RXA1		IN	IN	IN
55	54	50	CKA1		3T	I/O	I/O
			$\overline{TEND0}$		N/A	High	High
56	55	51	TXS		High	OUT	OUT
57	56	52	RXS		IN	IN	IN
			$\overline{CTS1}$		N/A	IN	IN
58	57	53	CKS		3T	I/O	I/O
59	58	54	$\overline{DREQ1}$		IN	3T	IN
60	59	55	$\overline{TEND1}$		High	OUT	High
61	60	56	$\overline{HALT}$		High	High	Low
62			NC				
63			NC				
64	61	57	$\overline{RFSH}$		High	OUT	High
65	62	58	$\overline{IORQ}$		High	3T	High
66	63	59	$\overline{MREQ}$		High	3T	High
67	64	60	E		Low	OUT	OUT
68	65	61	$\overline{M1}$		High	High	High
69	66	62	$\overline{WR}$		High	3T	High
70	67	63	$\overline{RD}$		High	3T	High
71	68	64	PHI		OUT	OUT	OUT
72	1	1	V_{SS}		GND	GND	GND
73	2		V_{SS}		GND	GND	GND
74	3	2	XTAL		OUT	OUT	OUT
75			NC				

OPERATION MODES

Z80 versus 64180 Compatibility. The Z8S180/Z8L180 is descended from two different "ancestor" processors, ZiLOG's original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR), illustrated in Figure 8, can be programmed to select between certain Z80 and 64180 differences.

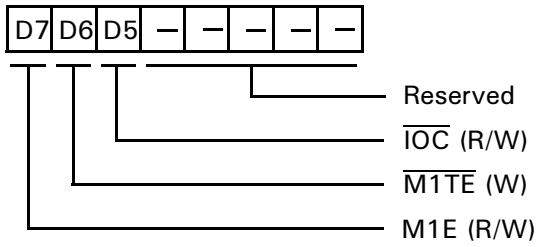


Figure 8. Operating Control Register (OMCR: I/O Address = 3EH)

M1E ($\overline{M1}$ Enable). This bit controls the $\overline{M1}$ output and is set to a 1 during RESET.

When M1E = 1, the $\overline{M1}$ output is asserted Low during opcode fetch cycles, Interrupt Acknowledge cycles, and the first machine cycle of an $\overline{NMI}$ acknowledge.

On the Z8S180/Z8L180, this choice makes the processor fetch a RETI instruction one time. When fetching a RETI from a zero-wait-state memory location, the processor uses three clock bus cycles. These bus cycles are not fully Z80-timing compatible.

When M1E = 0, the processor does not drive $\overline{M1}$ Low during the instruction fetch cycles. After fetching a RETI instruction with normal timing, the processor goes back and refetches the instruction using fully Z80-compatible cycles that include driving $\overline{M1}$ Low. This option may be required by some external Z80 peripherals to properly decode the RETI instruction. Figure 9 and Table 5 show the RETI sequence when M1E is 0.

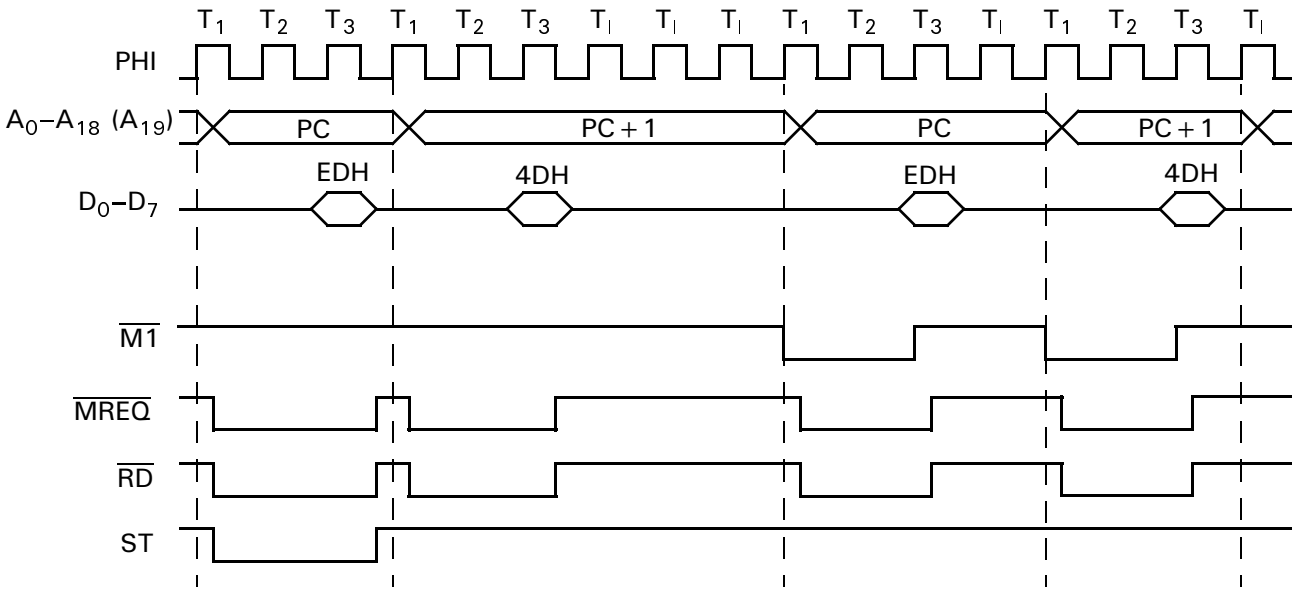


Figure 9. RETI Instruction Sequence with M1E = 0

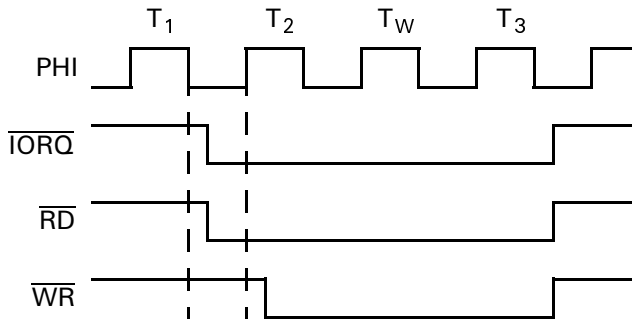


Figure 11. I/O Read and Write Cycles with $\overline{IOC}$ = 1

When $\overline{IOC}$ = 0, the timing of the $\overline{IORQ}$ and $\overline{RD}$ signals match the timing of the Z80. The $\overline{IORQ}$ and $\overline{RD}$ signals go active as a result of the rising edge of T2. (Figure 12.)

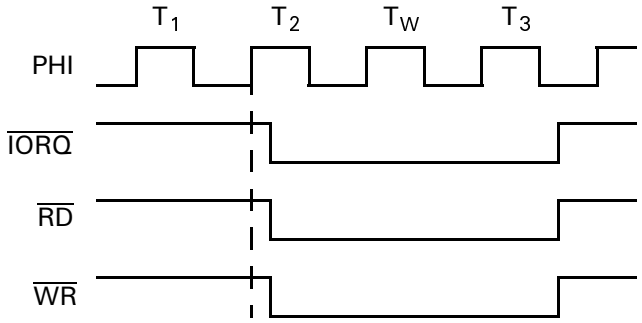


Figure 12. I/O Read and Write Cycles with $\overline{IOC}$ = 0

HALT and Low-Power Operating Modes. The Z8S180/Z8L180 can operate in seven modes with respect to activity and power consumption:

- Normal Operation
- HALT Mode
- IOSTOP Mode
- SLEEP Mode
- SYSTEM STOP Mode
- IDLE Mode
- STANDBY Mode (with or without QUICK RECOVERY)

Normal Operation. In this state, the Z8S180/Z8L180 processor is fetching and running a program. All enabled functions and portions of the device are active, and the $\overline{HALT}$ pin is High.

HALT Mode. This mode is entered by the HALT instruction. Thereafter, the Z8S180/Z8L180 processor continually fetches the following opcode but does not execute it and drives the $\overline{HALT}$, ST and $\overline{M1}$ pins all Low. The oscillator and PHI pin remain Active. Interrupts and bus granting to external Masters, and DRAM refresh can occur, and all on-chip I/O devices continue to operate including the DMA channels.

This condition provides a technique for synchronization with high-speed external events without incurring the latency imposed by an interrupt-response sequence. Figure 14 depicts the timing for exiting SLEEP mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes about 1.5 clock ticks to restart.

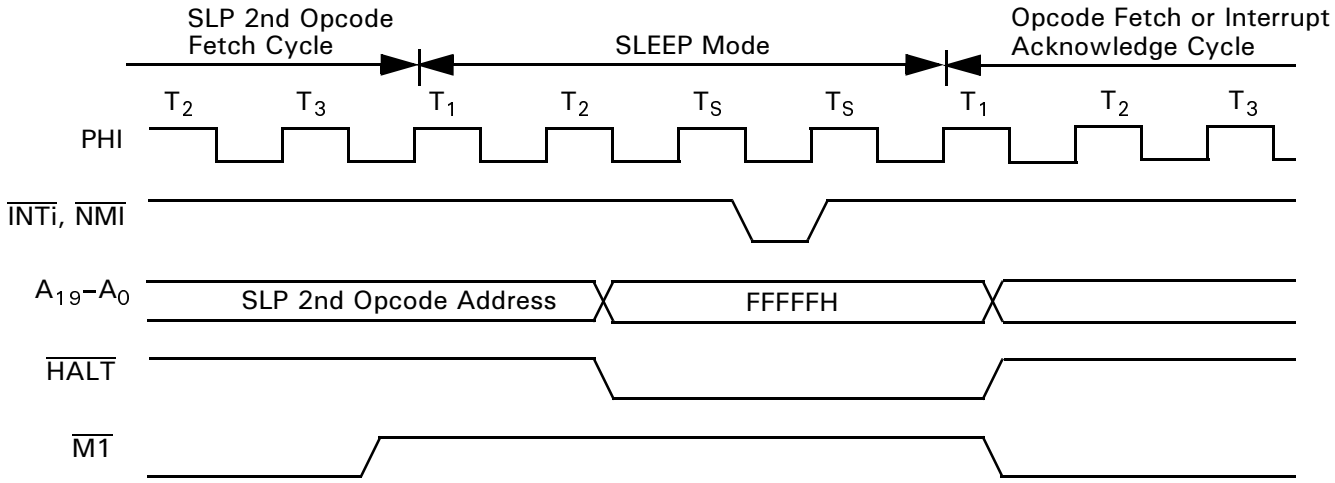


Figure 14. SLEEP Timing

IOSTOP Mode. IOSTOP mode is entered by setting the IOSTOP bit of the I/O Control Register (ICR) to 1. In this case, on-chip I/O (ASCI, CSI/O, PRT) stops operating. However, the CPU continues to operate. Recovery from IOSTOP mode is performed by resetting the IOSTOP bit in ICR to 0.

SYSTEM STOP Mode. SYSTEM STOP mode is the combination of SLEEP and IOSTOP modes. SYSTEM STOP mode is entered by setting the IOSTOP bit in ICR to 1 followed by execution of the SLP instruction. In this mode, on-chip I/O and CPU stop operating, reducing power consumption, but the PHI output continues to operate. Recovery from SYSTEM STOP mode is the same as recovery from SLEEP mode except that internal I/O sources (disabled by IOSTOP) cannot generate a recovery interrupt.

IDLE Mode. Software puts the Z8S180/Z8L180 into this mode by performing the following actions:

- Set the IOSTOP bit (ICR5) to 1
- Set CCR6 to 0
- Set CCR3 to 1
- Execute the SLP instruction

The oscillator keeps operating but its output is blocked to all circuitry including the PHI pin. DRAM refresh and all internal devices stop, but external interrupts can occur. Bus granting to external Masters can occur if the BREST bit in the CPU control Register (CCR5) was set to 1 before IDLE mode was entered.

The Z8S180/Z8L180 leaves IDLE mode in response to a Low on $\overline{\text{RESET}}$, an external interrupt request on $\overline{\text{NMI}}$, or an external interrupt request on $\overline{\text{INT0}}$, $\overline{\text{INT1}}$ or $\overline{\text{INT2}}$ that is enabled in the INT/TRAP Control Register. As previously described for SLEEP mode, when the Z8S180/Z8L180 leaves IDLE mode due to an $\overline{\text{NMI}}$, or due to an enabled external interrupt request when the $\overline{\text{IEF}}$ flag is 1 due to an EI instruction, the device starts by performing the interrupt with the return address of the instruction after the SLP instruction.

If an external interrupt enables the INT/TRAP control register while the IEF1 bit is 0, Z8S180/Z8L180 leaves IDLE mode; specifically, the processor restarts by executing the instructions following the SLP instruction.

Figure 15 indicates the timing for exiting IDLE mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes about 9.5 clocks to restart.

ing the bus to an external Master during STANDBY mode, when the BREXT bit in the CPU Control Register (CCR5) is 1.

As described previously for SLEEP and IDLE modes, when the MPU leaves STANDBY mode due to $\overline{NMI}$ Low or an enabled $\overline{INT0}$–$\overline{INT2}$ Low when the IEF, flag is 1 due to an IE instruction, it starts by performing the interrupt with the return address being that of the instruction following the SLP instruction. If the Z8S180/Z8L180 leaves STANDBY mode due to an external interrupt request that's enabled in the INT/TRAP Control Register, but the IEF, bit is 0 due to a DI instruction, the processor restarts by executing the instruction(s) following the SLP instruction. If $\overline{INT0}$, or $\overline{INT1}$ or $\overline{INT2}$ goes inactive before the end of the clock stabilization delay, the Z8S180/Z8L180 stays in STANDBY mode.

Figure 17 indicates the timing for leaving STANDBY mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes either 64 or 2^{17} (131,072) clocks to restart, depending on the CCR3 bit.

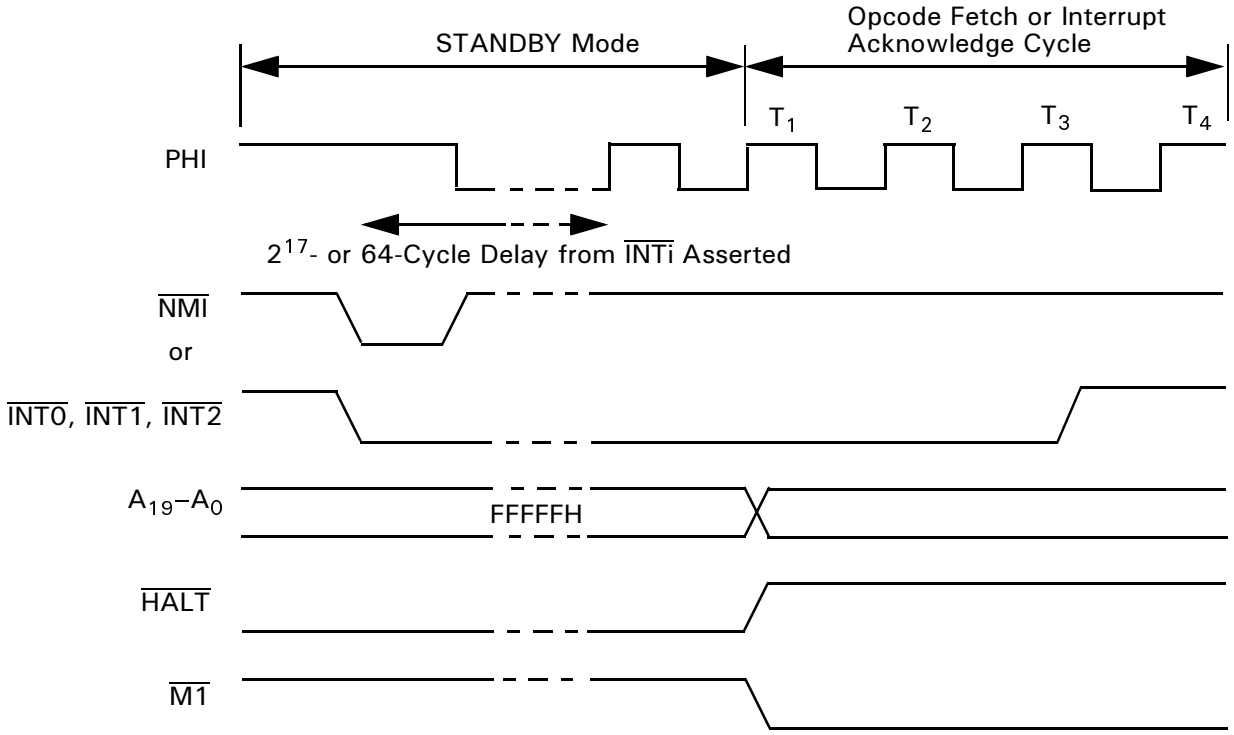


Figure 17. Z8S180/Z8L180 STANDBY Mode Exit Due to External Interrupt

While the Z8S180/Z8L180 is in STANDBY mode, it grants the bus to an external Master if the BREXT bit (CCR5) is 1. Figure 18 indicates the timing of this sequence. The device takes 64 or 2^{17} (131,072) clock cycles to grant the bus depending on the CCR3 bit. The latter (not the QUICK RECOVERY) case may be prohibitive for many demand-driven external Masters. If so, QUICK RECOVERY or IDLE mode can be used.

DC CHARACTERISTICS—Z8S180

Table 6. Z8S180 DC Characteristics
V_{DD} = 5V ±10%; V_{SS} = 0V

Symbol	Item	Condition	Min	Typ	Max	Unit
V_{IH1}	Input H Voltage $\overline{RESET}$, EXTAL, $\overline{NMI}$		V_{DD} –0.6	—	V_{DD} +0.3	V
V_{IH2}	Input H Voltage Except $\overline{RESET}$, EXTAL, $\overline{NMI}$		2.0	—	V_{DD} +0.3	V
V_{IH3}	Input H Voltage CKS, CKA0, CKA1		2.4	—	V_{DD} +0.3	V
V_{IL1}	Input L Voltage RESET, EXTAL, NMI		–0.3	—	0.6	V
V_{IL2}	Input L Voltage Except RESET, EXTAL, NMI		–0.3	—	0.8	V
V_{OH}	Outputs H Voltage All outputs	I_{OH} = –200 µA	2.4	—	—	V
		I_{OH} = –20 µA	V_{DD} –1.2	—	—	
V_{OL}	Outputs L Voltage All outputs	I_{OL} = 2.2 mA	—	—	0.45	V
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL	V_{IN} = 0.5 ~ V_{DD} –0.5	—	—	1.0	µA
I_{TL}	Three State Leakage Current	V_{IN} = 0.5 ~ V_{DD} –0.5	—	—	1.0	µA
I_{DD}[1]	Power Dissipation (Normal Operation)	F = 10 MHz	—	25	60	mA
		20		30	50	
		33		60	100	
	Power Dissipation (SYSTEM STOP mode)	F = 10 MHz	—	2	5	
		20		3	6	
		33		5	9	
C_P	Pin Capacitance	V_{IN} = 0_V, f = 1 MHz T_A = 25°C	—	—	12	pF

Note:
1. V_{IHmin} = V_{DD}–1.0V, V_{ILmax} = 0.8V (All output terminals are at NO LOAD.) V_{DD} = 5.0V.

AC CHARACTERISTICS—Z8S180 (Continued)

Table 8. Z8S180 AC Characteristics (Continued)
V_{DD} = 5V ±10% or V_{DD} = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation

			Z8S180—20 MHz		Z8S180—33 MHz		
Number	**Symbol**	**Item**	**Min**	**Max**	**Min**	**Max**	**Unit**
32	t_{INTH}	$\overline{INT}$ Hold Time from PHI Fall	10	—	10	—	ns
33	t_{NMIW}	$\overline{NMI}$ Pulse Width	35	—	25	—	ns
34	t_{BRS}	$\overline{BUSREQ}$ Set-up Time to PHI Fall	10	—	10	—	ns
35	t_{BRH}	$\overline{BUSREQ}$ Hold Time from PHI Fall	10	—	10		ns
36	t_{BAD1}	PHI Rise to $\overline{BUSACK}$ Fall Delay	—	25	—	15	ns
37	t_{BAD2}	PHI Fall to $\overline{BUSACK}$ Rise Delay	—	25	—	15	ns
38	t_{BZD}	PHI Rise to Bus Floating Delay Time	—	40	—	30	ns
39	t_{MEWH}	$\overline{MREQ}$ Pulse Width (High)	35	—	25	—	ns
40	t_{MEWL}	$\overline{MREQ}$ Pulse Width (Low)	35	—	25	—	ns
41	t_{RFD1}	PHI Rise to $\overline{RFSH}$ Fall Delay	—	20	—	15	ns
42	t_{RFD2}	PHI Rise to $\overline{RFSH}$ Rise Delay	—	20	—	15	ns
43	t_{HAD1}	PHI Rise to $\overline{HALT}$ Fall Delay	—	15	—	15	ns
44	t_{HAD2}	PHI Rise to $\overline{HALT}$ Rise Delay	—	15	—	15	ns
45	t_{DRQS}	$\overline{DREQ1}$ Set-up Time to PHI Rise	20	—	15	—	ns
46	t_{DRQH}	$\overline{DREQ1}$ Hold Time from PHI Rise	20	—	15	—	ns
47	t_{TED1}	PHI Fall to $\overline{TENDi}$ Fall Delay	—	25	—	15	ns
48	t_{TED2}	PHI Fall to $\overline{TENDi}$ Rise Delay	—	25	—	15	ns
49	t_{ED1}	PHI Rise to E Rise Delay	—	30	—	15	ns
50	t_{ED2}	PHI Fall or Rise to E Fall Delay	—	30	—	15	ns
51	P_{WEH}	E Pulse Width (High)	25	—	20	—	ns
52	P_{WEL}	E Pulse Width (Low)	50	—	40	—	ns
53	t_{Er}	Enable Rise Time	—	10	—	10	ns
54	t_{Ef}	Enable Fall Time	—	10	—	10	ns
55	t_{TOD}	PHI Fall to Timer Output Delay	—	75	—	50	ns
56	t_{STDI}	CSI/O Transmit Data Delay Time (Internal Clock Operation)	—	2	—	2	tcyc
57	t_{STDE}	CSI/O Transmit Data Delay Time (External Clock Operation)	—	7.5 t_{CYC} +75	—	75 t_{CYC} +60	ns
58	t_{SRSI}	CSI/O Receive Data Set-up Time (Internal Clock Operation)	1	—	1	—	tcyc
59	t_{SRHI}	CSI/O Receive Data Hold Time (Internal Clock Operation)	1	—	1	—	tcyc
60	t_{SRSE}	CSI/O Receive Data Set-up Time (External Clock Operation)	1	—	1	—	tcyc
61	t_{SRHE}	CSI/O Receive Data Hold Time (External Clock Operation)	1	—	1	—	tcyc
62	t_{RES}	$\overline{RESET}$ Set-up Time to PHI Fall	40	—	25	—	ns

Table 8. Z8S180 AC Characteristics (Continued)
V_{DD} = 5V ±10% or V_{DD} = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation

			Z8S180—20 MHz		Z8S180—33 MHz		
Number	**Symbol**	**Item**	**Min**	**Max**	**Min**	**Max**	**Unit**
63	t_{REH}	$\overline{RESET}$ Hold Time from PHI Fall	25	—	15	—	ns
64	t_{OSC}	Oscillator Stabilization Time	—	20	—	20	ns
65	t_{EXR}	External Clock Rise Time (EXTAL)	—	5	—	5	ns
66	t_{EXF}	External Clock Fall Time (EXTAL)	—	5	—	5	ns
67	t_{RR}	$\overline{RESET}$ Rise Time	—	50	—	50	ms
68	t_{RF}	$\overline{RESET}$ Fall Time	—	50	—	50	ms
69	t_{IR}	Input Rise Time (except EXTAL, $\overline{RESET}$)	—	50	—	50	ns
70	t_{IF}	Input Fall Time (except EXTAL, $\overline{RESET}$)	—	50	—	50	ns

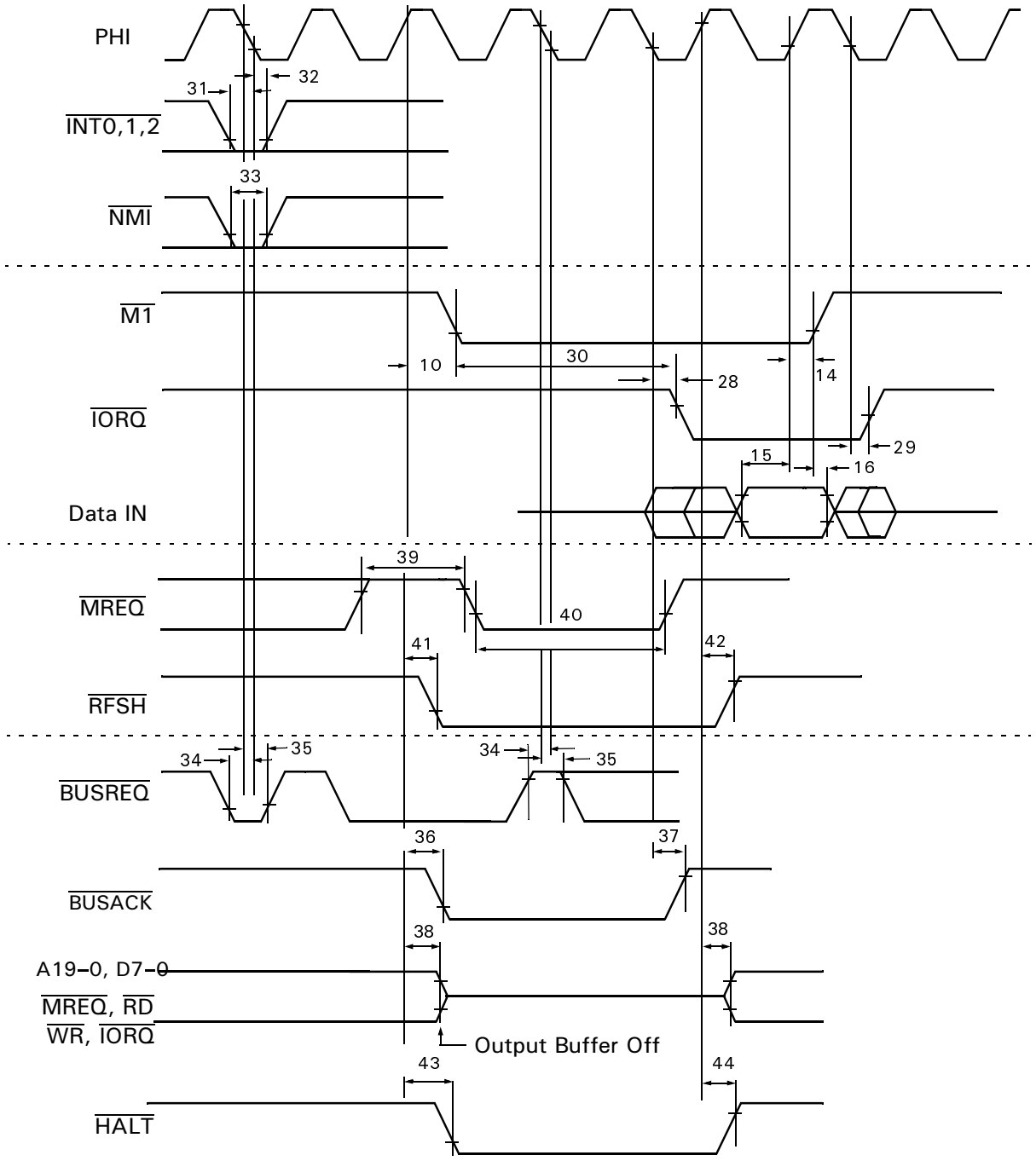


Figure 21. CPU Timing
(INT0 Acknowledge Cycle, Refresh Cycle, BUS RELEASE Mode, HALT Mode, SLEEP Mode, SYSTEM STOP Mode)

TIMING DIAGRAMS (Continued)

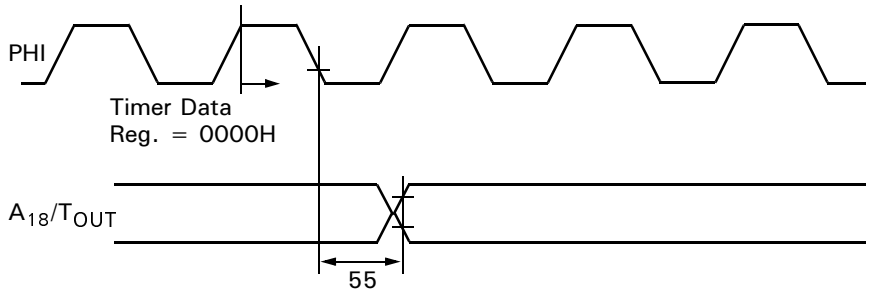


Figure 27. Timer Output Timing

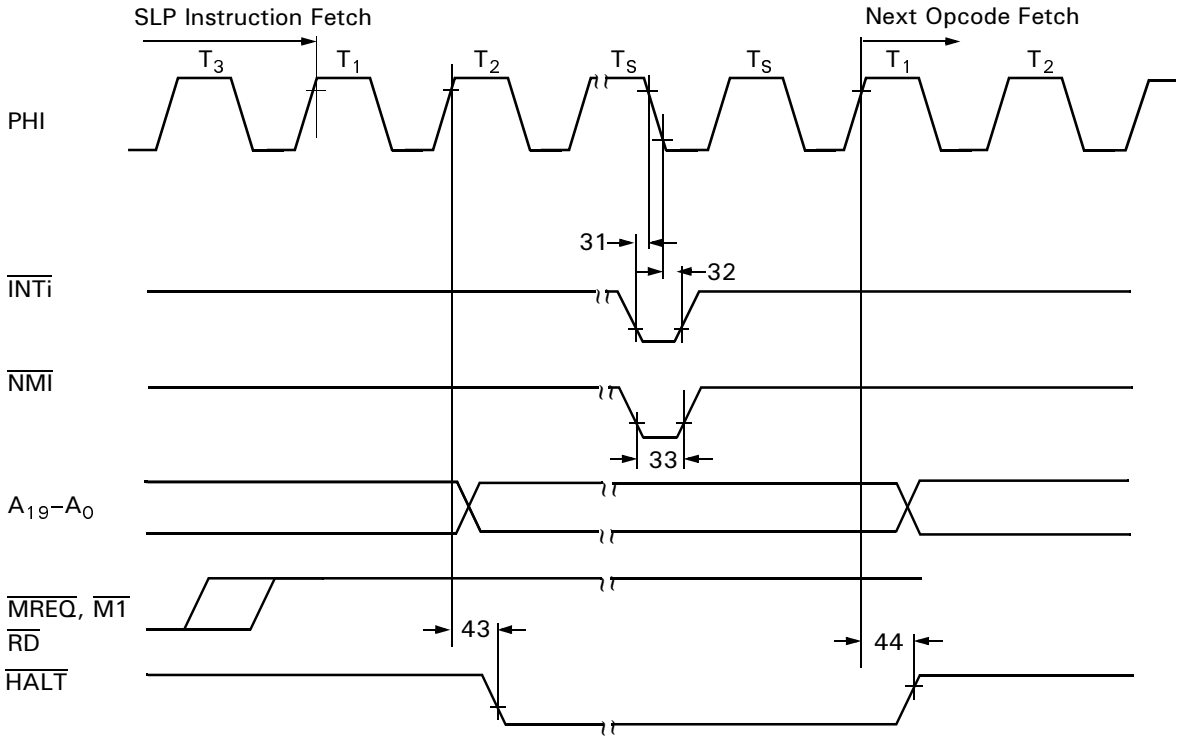


Figure 28. SLP Execution Cycle

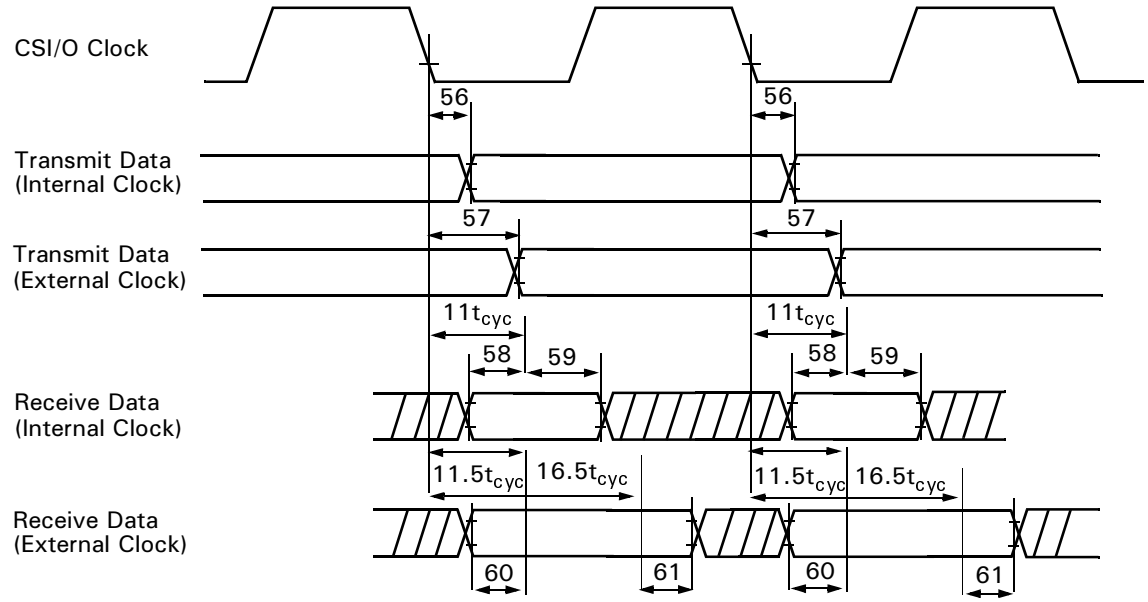


Figure 29. CSI/O Receive/Transmit Timing

External Clock Rise Time and Fall Time

Input Rise Time and Fall Time (Except EXTAL, $\overline{\text{RESET}}$)

Figure 30. Rise Time and Fall Times

Bit 2 LNIO. This bit controls the drive capability of certain external I/O pins of the Z8S180/Z8L180. When this bit is set to 1, the output drive capability of the following pins is reduced to 33 percent of the original drive capability:

$\overline{RTS0}$	TxS
CKA1/$\overline{TEND0}$	CKA0/$\overline{DREQ0}$
TXA0	TXA1
$\overline{TENDi}$	CKS

Bit 1 LNCPUCTL. This bit controls the drive capability of the CPU Control pins. When this bit is set to 1, the output drive capability of the following pins is reduced to 33 percent of the original drive capability:

$\overline{BUSACK}$	$\overline{RD}$
$\overline{WR}$	$\overline{M1}$
$\overline{MREQ}$	$\overline{IORQ}$
$\overline{RFSH}$	$\overline{HALT}$
E	TEST
ST	

Bit 0 LNAD/DATA. This bit controls the drive capability of the Address/Data bus output drivers. If this bit is set to 1, the output drive capability of the Address and Data bus outputs is reduced to 33 percent of its original drive capability.

ASCI CHANNEL CONTROL REGISTER A (Continued)

vious contents of TDRE are held. TE is cleared to 0 in IOSTOP mode during RESET.

$\overline{\text{RTS0}}$: Request to Send Channel 0 (Bit 4 in CNTLA0 Only). If bit 4 of the System Configuration Register is 0, the $\overline{\text{RTS0}}$/TXS pin exhibits the $\overline{\text{RTS0}}$ function. $\overline{\text{RTS0}}$ allows the ASCI to control (start/stop) another communication devices transmission (for example, by connecting to that device's $\overline{\text{CTS}}$ input). $\overline{\text{RTS0}}$ is essentially a 1-bit output port, having no side effects on other ASCI registers or flags.

Bit 4 in CNTLA1 is used.

CKA1D = 1, CKA1/$\overline{\text{TEND0}}$ pin = $\overline{\text{TEND0}}$

CKA1D = 0, CKA1/$\overline{\text{TEND0}}$ pin = CKA1

These bits are cleared to 0 on reset.

MPBR/EFR: Multiprocessor Bit Receive/Error Flag Reset (Bit 3). When multiprocessor mode is enabled (MP in CNTLB = 1), MPBR, when read, contains the value of the MPB bit for the most recent receive operation. When written to 0, the EFR function is selected to reset all error flags (OVRN, FE, PE and BRK in the ASEXT Register) to 0. MPBR/EFR is undefined during RESET.

MOD2, 1, 0: ASCI Data Format Mode 2,1,0 (bits 2–0).

These bits program the ASCI data format as follows.

MOD2

= 0→7 bit data

= 1→8 bit data

MOD1

= 0→No parity

= 1→Parity enabled

MOD0

= 0→1 stop bit

= 1→2 stop bits

The data formats available based on all combinations of MOD2, MOD1, and MOD0 are indicated in Table 9.

Table 9. Data Formats

MOD2	MOD1	MOD0	Data Format
0	0	0	Start + 7 bit data + 1 stop
0	0	1	Start + 7 bit data + 2 stop
0	1	0	Start + 7 bit data + parity + 1 stop
0	1	1	Start + 7 bit data + parity + 2 stop
1	0	0	Start + 8 bit data + 1 stop
1	0	1	Start + 8 bit data + 2 stop
1	1	0	Start + 8 bit data + parity + 1 stop
1	1	1	Start + 8 bit data + parity + 2 stop

ASCI0 requests an interrupt when $\overline{DCD0}$ goes High. RIE is cleared to 0 by RESET.

$\overline{DCD0}$: Data Carrier Detect (Bit 2 STAT0). This bit is set to 1 when the pin is High. It is cleared to 0 on the first READ of STAT0 following the pin's transition from High to Low and during RESET. When bit 6 of the ASEXT0 register is 0 to select auto-enabling, and the pin is negated (High), the receiver is reset and its operation is inhibited.

$\overline{CTS1E}$: Clear To Send (Bit 2 STAT1). Channel 1 features an external $\overline{CTS1}$ input, which is multiplexed with the receive data pin RSX for the CSI/O. Setting this bit to 1 selects the CTS1 function; clearing the bit to 0 selects the RXS function.

TDRE: Transmit Data Register Empty (Bit 1). TDRE = 1 indicates that the TDR is empty and the next transmit data byte is written to TDR. After the byte is written to TDR, TDRE is cleared to 0 until the ASCI transfers the byte from TDR to the TSR and then TDRE is again set to 1. TDRE is set to 1 in IOSTOP mode and during RESET. On ASCI0, if the $\overline{CTS0}$ pin is auto-enabled in the ASEXT0 register and the pin is High, TDRE is reset to 0.

TIE: Transmit Interrupt Enable (Bit 0). TIE should be set to 1 to enable ASCI transmit interrupt requests. If TIE = 1, an interrupt is requested when TDRE = 1. TIE is cleared to 0 during RESET.

ASCI TRANSMIT DATA REGISTERS

Register addresses 06H and 07H hold the ASCI transmit data for channel 0 and channel 1, respectively.

ASCI Transmit Data Registers Channel 0

Mnemonic TDR0
Address 06H

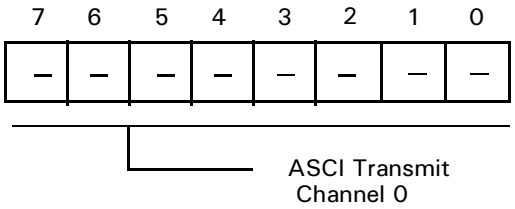


Figure 36. ASCI Register

ASCI Transmit Data Registers Channel 1

Mnemonic TDR1
Address 07H

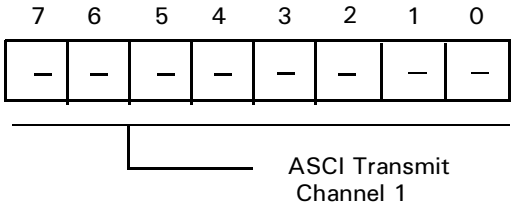


Figure 37. ASCI Register

DMA MEMORY ADDRESS REGISTER CHANNEL 1

The DMA Memory Address Register Channel 1 specifies the physical memory address for channel 1 transfers. The address may be a destination or a source memory location. The register contains 20 bits and may specify up to 1024 KB memory addresses.

DMA Memory Address Register, Channel 1L

Mnemonic MAR1L
Address 28H

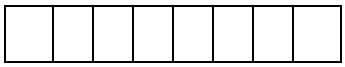


Figure 65. DMA Memory Address Register, Channel 1L

DMA Memory Address Register, Channel 1H

Mnemonic MAR1H
Address 29H

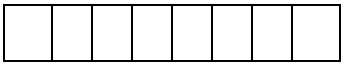


Figure 66. DMA Memory Address Register, Channel 1H

DMA Memory Address Register, Channel 1B

Mnemonic MAR1B
Address 2AH

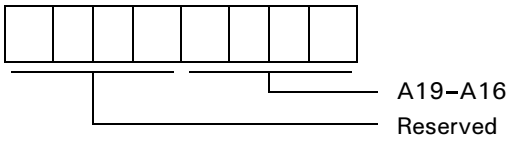


Figure 67. DMA Memory Address Register, Channel 1B

Table 16 indicates all DMA transfer mode combinations of DM0, DM1, SM0, and SM1. Because I/O to/from I/O transfers are not implemented, 12 combinations are available.

Table 16. Transfer Mode Combinations

DM1	DM0	SM1	SM0	Transfer Mode	Address Increment/Decrement
0	0	0	0	Memory→Memory	SAR0 + 1, DAR0 + 1
0	0	0	1	Memory→Memory	SAR0–1, DAR0 + 1
0	0	1	0	Memory*→Memory	SAR0 fixed, DAR0 + 1
0	0	1	1	I/O→Memory	SAR0 fixed, DAR0 + 1
0	1	0	0	Memory→Memory	SAR0 + 1, DAR0–1
0	1	0	1	Memory→Memory	SAR0–1, DAR0–1
0	1	1	0	Memory*→Memory	SAR0 fixed, DAR0–1
0	1	1	1	I/O→Memory	SAR0 fixed, DAR0–1
1	0	0	0	Memory→Memory*	SAR0 + 1, DAR0 fixed
1	0	0	1	Memory→Memory*	SAR0–1, DAR0 fixed
1	0	1	0	Reserved	
1	0	1	1	Reserved	
1	1	0	0	Memory→I/O	SAR0 + 1, DAR0 fixed
1	1	0	1	Memory→I/O	SAR0–1, DAR0 fixed
1	1	1	0	Reserved	
1	1	1	1	Reserved	

Note: * Includes memory mapped I/O.

MMOD: Memory Mode Channel 0 (Bit 1). When channel 0 is configured for memory to/from memory transfers there is no Request Handshake signal to control the transfer timing. Instead, two automatic transfer timing modes are selectable: burst (MMOD = 1) and cycle steal (MMOD = 0). For burst memory to/from memory transfers, the DMAC takes control of the bus continuously until the DMA transfer completes (as indicated by the byte count register = 0). In cycle steal mode, the CPU is provided a cycle for each DMA byte transfer cycle until the transfer is completed.

For channel 0 DMA with I/O source or destination, the selected Request signal times the transfer ignoring MMOD. MMOD is cleared to 0 during RESET.

DMA/WAIT CONTROL REGISTER

The DMA/WAIT Control Register (DCNTL) controls the insertion of wait states into DMAC (and CPU) accesses of memory or I/O. Also, the register defines the Request signal for each channel as level or edge sense. DCNTL also sets the DMA transfer mode for channel 1, which is limited to memory to/from I/O transfers.

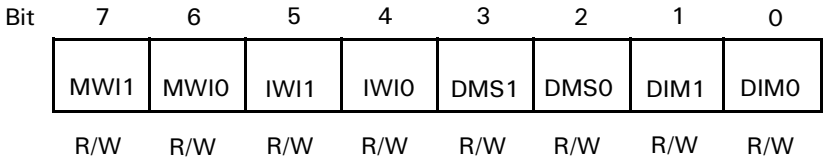


Figure 73. DMA/WAIT Control Register (DCNTL: I/O Address = 32H)

MWI1, MWI0: Memory Wait Insertion (Bits 7–6). This bit specifies the number of wait states introduced into CPU or DMAC memory access cycles. MWI1 and MWI0 are set to 1 during RESET.

MWI1	MWI0	Wait State
0	0	0
0	1	1
1	0	2
1	1	3

IWI1, IWI0: I/O Wait Insertion (Bits 5–4). This bit specifies the number of wait states introduced into CPU or DMAC I/O access cycles. IWI1 and IWI0 are set to 1 during RESET.

IWI1	IWI0	Wait State
0	0	1
0	1	2
1	0	3
1	1	4

Note: These wait states are added to the 3-clock I/O cycle that is used to access the on-chip I/O registers. It is equally valid to regard these as 0 to 3 wait states added to a 4-clock external I/O cycle.

DMS1, DMS0: DMA Request Sense (Bits 3–2). DMS1 and DMS0 specify the DMA request sense for channel 0 and channel 1 respectively. When reset to 0, the input is level sense. When set to 1, the input is edge sense. DMS1 and DMS0 are cleared to 0 during RESET.

DMSi	Sense
1	Edge Sense
0	Level Sense

Typically, for an input/source device, the associated DMS bit should be programmed as 0 for level sense. The device takes a relatively long time to update its Request signal after the DMA channel reads data (in the first of the two machine cycles involved in transferring a byte).

An output/destination device takes much less time to update its Request signal after the DMA channel starts a WRITE operation to it (the second machine cycle of the two cycles involved in transferring a byte). With zero-wait state I/O cycles, a device cannot update its request signal in the required time, so edge sensing must be used.

A one-wait-state I/O cycle also does not provide sufficient time for updating, so edge sensing is again required.

DIM1, DIM0: DMA Channel 1 I/O and Memory Mode (Bits 1–0). Specifies the source/destination and address modifier for channel 1 memory to/from I/O transfer modes. DIM1 and DIM0 are cleared to 0 during RESET.

Table 17. Channel 1 Transfer Mode

DIM1	DMI0	Transfer Mode	Address Increment/Decrement
0	0	Memory→I/O	MAR1 +1, IAR1 fixed
0	1	Memory→I/O	MAR1 –1, IAR1 fixed
1	0	I/O→Memory	IAR1 fixed, MAR1 +1
1	1	I/O→Memory	IAR1 fixed, MAR1 –1

MMU COMMON BASE REGISTER

The Common Base Register (CBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical address for Common Area 1 accesses. All bits of CBR are reset to 0 during RESET.

MMU Common Base Register

Mnemonic CBR
Address 38H

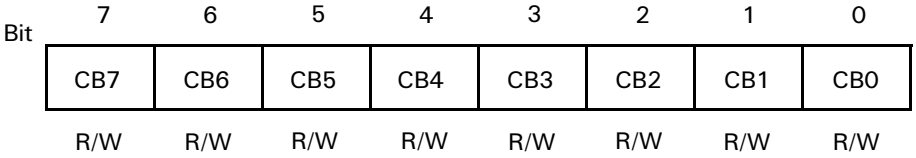


Figure 78. MMU Common Base Register (CBR: I/O Address = 38H)

MMU BANK BASE REGISTER

The Bank Base Register (BBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical address for Bank Area accesses. All bits of BBR are reset to 0 during RESET.

MMU Bank Base Register

Mnemonic BBR
Address 39H

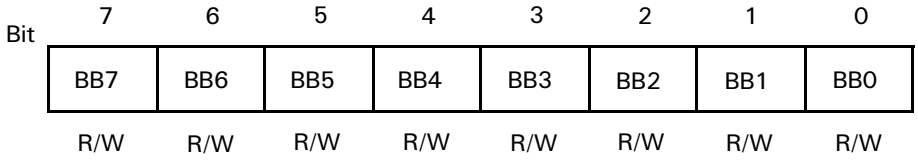


Figure 79. MMU Bank Base Register (BBR: I/O Address = 39H)

MMU COMMON/BANK AREA REGISTER

The Common/Bank Area Register (CBAR) specifies boundaries within the Z8S180/Z8L180 64-KB logical address space for up to three areas; Common Area), Bank Area and Common Area 1.

MMU Common/Bank Area Register

Mnemonic CBAR
Address 3AH

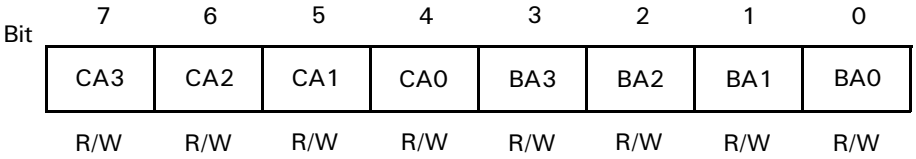
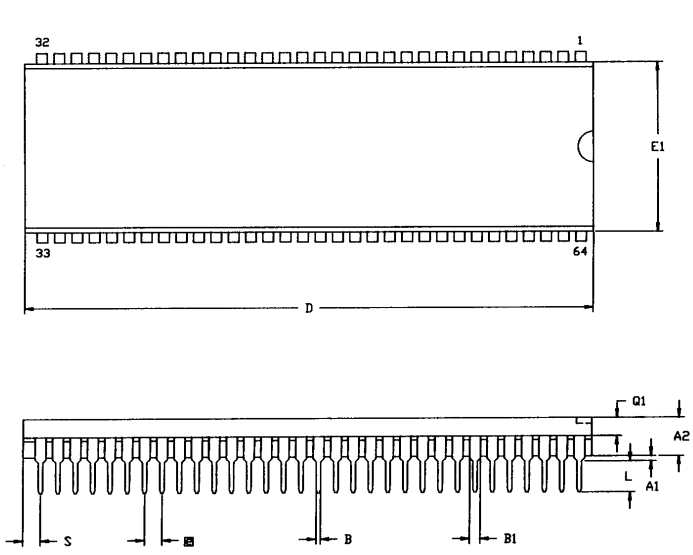


Figure 80. MMU Common/Bank Area Register (CBAR: I/O Address = 3AH)

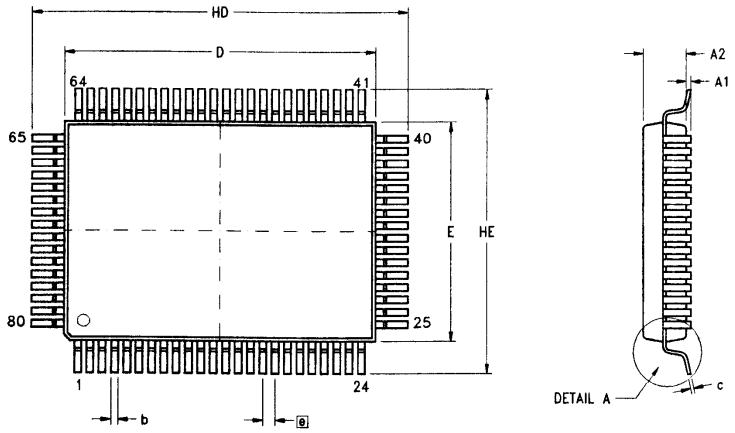
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	1.07	.015	.042
A2	3.68	3.94	.145	.155
B	0.38	0.53	.015	.021
B1	0.94	1.09	.037	.043
C	0.23	0.38	.009	.015
D	57.40	58.17	2.260	2.290
E	18.80	19.30	.740	.760
E1	16.76	17.27	.660	.680
e	1.78 TYP		.070 TYP	
eA	19.30	20.32	.760	.800
L	3.18	3.81	.125	.150
Q1	1.65	1.91	.065	.075
S	1.02	1.78	.040	.070

CONTROLLING DIMENSIONS : INCH

Figure 85. 64-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.10	0.30	.004	.012
A2	2.60	2.80	.102	.110
b	0.30	0.45	.012	.018
c	0.13	0.20	.005	.008
HD	23.70	24.15	.933	.951
D	19.90	20.10	.783	.791
HE	17.70	18.15	.697	.715
E	13.90	14.10	.547	.555
e	0.80 TYP		.0315 TYP	
L	0.70	1.10	.028	.043

NOTES:
1. CONTROLLING DIMENSIONS: MILLIMETER
2. MAX COPLANARITY: .10 / .004

Figure 86. 80-Pin QFP Package Diagram