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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z8S180 |
| Number of Cores/Bus Width | 1 Core, 8-Bit |
| Speed | 10MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 5.0V |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Security Features | - |
| Package / Case | 68-LCC (J-Lead) |
| Supplier Device Package | 68-PLCC |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8s18010vsc00tr |

**Table 1. Z8S180/Z8L180 Pin Identification (Continued)**

| Pin Number and Package Type | | | Default | Secondary | |
|---|---|---|---|---|---|
| QFP | PLCC | DIP | Function | Function | Control |
| 53 | 52 | | TEST | | |
| 54 | 53 | 49 | RXA1 | | |
| 55 | 54 | 50 | CKA1 | $\overline{\text{TEND0}}$ | Bit 4 of CNTLA1 |
| 56 | 55 | 51 | TXS | | |
| 57 | 56 | 52 | RXS | $\overline{\text{CTS1}}$ | Bit 2 of STAT1 |
| 58 | 57 | 53 | CKS | | |
| 59 | 58 | 54 | $\overline{\text{DREQ1}}$ | | |
| 60 | 59 | 55 | $\overline{\text{TEND1}}$ | | |
| 61 | 60 | 56 | $\overline{\text{HALT}}$ | | |
| 62 | | | NC | | |
| 63 | | | NC | | |
| 64 | 61 | 57 | $\overline{\text{RFSH}}$ | | |
| 65 | 62 | 58 | $\overline{\text{IORQ}}$ | | |
| 66 | 63 | 59 | $\overline{\text{MREQ}}$ | | |
| 67 | 64 | 60 | E | | |
| 68 | 65 | 61 | $\overline{\text{M1}}$ | | |
| 69 | 66 | 62 | $\overline{\text{WR}}$ | | |
| 70 | 67 | 63 | $\overline{\text{RD}}$ | | |
| 71 | 68 | 64 | PHI | | |
| 72 | 1 | 1 | $V_{SS}$ | | |
| 73 | 2 | | $V_{SS}$ | | |
| 74 | 3 | 2 | XTAL | | |
| 75 | | | NC | | |
| 76 | 4 | 3 | EXTAL | | |
| 77 | 5 | 4 | $\overline{\text{WAIT}}$ | | |
| 78 | 6 | 5 | $\overline{\text{BUSACK}}$ | | |
| 79 | 7 | 6 | $\overline{\text{BUSREQ}}$ | | |
| 80 | 8 | 7 | $\overline{\text{RESET}}$ | | |

## PIN IDENTIFICATION (Continued)

**Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes**

| Pin Number and Package Type | | | | | Pin Status | | |
|---|---|---|---|---|---|---|---|
| QFP | PLCC | DIP | Default Function | Secondary Function | RESET | BUSACK | SLEEP |
| 1 | 9 | 8 | $\overline{NMI}$ | | IN | IN | IN |
| 2 | | | NC | | | | |
| 3 | | | NC | | | | |
| 4 | 10 | 9 | $\overline{INT0}$ | | IN | IN | IN |
| 5 | 11 | 10 | $\overline{INT1}$ | | IN | IN | IN |
| 6 | 12 | 11 | $\overline{INT2}$ | | IN | IN | IN |
| 7 | 13 | 12 | ST | | High | High | High |
| 8 | 14 | 13 | A0 | | 3T | 3T | High |
| 9 | 15 | 14 | A1 | | 3T | 3T | High |
| 10 | 16 | 15 | A2 | | 3T | 3T | High |
| 11 | 17 | 16 | A3 | | 3T | 3T | High |
| 12 | 18 | | $V_{SS}$ | | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ |
| 13 | 19 | 17 | A4 | | 3T | 3T | High |
| 14 | | | NC | | | | |
| 15 | 20 | 18 | A5 | | 3T | 3T | High |
| 16 | 21 | 19 | A6 | | 3T | 3T | High |
| 17 | 22 | 20 | A7 | | 3T | 3T | High |
| 18 | 23 | 21 | A8 | | 3T | 3T | High |
| 19 | 24 | 22 | A9 | | 3T | 3T | High |
| 20 | 25 | 23 | A10 | | 3T | 3T | High |
| 21 | 26 | 24 | A11 | | 3T | 3T | High |
| 22 | | | NC | | | | |
| 23 | | | NC | | | | |
| 24 | 27 | 25 | A12 | | 3T | 3T | High |
| 25 | 28 | 26 | A13 | | 3T | 3T | High |
| 26 | 29 | 27 | A14 | | 3T | 3T | High |
| 27 | 30 | 28 | A15 | | 3T | 3T | High |
| 28 | 31 | 29 | A16 | | 3T | 3T | High |
| 29 | 32 | 30 | A17 | | 3T | 3T | High |
| 30 | | | NC | | | | |
| 31 | 33 | 31 | A18 | | 3T | 3T | High |
| | | | $T_{OUT}$ | | N/A | OUT | OUT |
| 32 | 34 | 32 | $V_{DD}$ | | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ |
| 33 | 35 | | A19 | | 3T | 3T | High |
| 34 | 36 | 33 | $V_{SS}$ | | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ |
| 35 | 37 | 34 | D0 | | 3T | 3T | 3T |
| 36 | 38 | 35 | D1 | | 3T | 3T | 3T |
| 37 | 39 | 36 | D2 | | 3T | 3T | 3T |
| 38 | 40 | 37 | D3 | | 3T | 3T | 3T |

**Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)**

| Pin Number and Package Type | | | | | Pin Status | | |
|---|---|---|---|---|---|---|---|
| QFP | PLCC | DIP | Default Function | Secondary Function | RESET | BUSACK | SLEEP |
| 39 | 41 | 38 | D4 | | 3T | 3T | 3T |
| 40 | 42 | 39 | D5 | | 3T | 3T | 3T |
| 41 | 43 | 40 | D6 | | 3T | 3T | 3T |
| 42 | | | NC | | | | |
| 43 | | | NC | | | | |
| 44 | 44 | 41 | D7 | | 3T | 3T | 3T |
| 45 | 45 | 42 | $\overline{RTS0}$ | | High | OUT | High |
| 46 | 46 | 43 | $\overline{CTS0}$ | | IN | OUT | IN |
| 47 | 47 | 44 | $\overline{DCD0}$ | | IN | IN | IN |
| 48 | 48 | 45 | TXA0 | | High | OUT | OUT |
| 49 | 49 | 46 | RXA0 | | IN | IN | IN |
| 50 | 50 | 47 | CKA0 | | 3T | I/O | I/O |
| | | | $\overline{DREQ0}$ | | N/A | IN | IN |
| 51 | | | NC | | | | |
| 52 | 51 | 48 | TXA1 | | High | OUT | OUT |
| 53 | 52 | | TEST | | | | |
| 54 | 53 | 49 | RXA1 | | IN | IN | IN |
| 55 | 54 | 50 | CKA1 | | 3T | I/O | I/O |
| | | | $\overline{TEND0}$ | | N/A | High | High |
| 56 | 55 | 51 | TXS | | High | OUT | OUT |
| 57 | 56 | 52 | RXS | | IN | IN | IN |
| | | | $\overline{CTS1}$ | | N/A | IN | IN |
| 58 | 57 | 53 | CKS | | 3T | I/O | I/O |
| 59 | 58 | 54 | $\overline{DREQ1}$ | | IN | 3T | IN |
| 60 | 59 | 55 | $\overline{TEND1}$ | | High | OUT | High |
| 61 | 60 | 56 | $\overline{HALT}$ | | High | High | Low |
| 62 | | | NC | | | | |
| 63 | | | NC | | | | |
| 64 | 61 | 57 | $\overline{RFSH}$ | | High | OUT | High |
| 65 | 62 | 58 | $\overline{IORQ}$ | | High | 3T | High |
| 66 | 63 | 59 | $\overline{MREQ}$ | | High | 3T | High |
| 67 | 64 | 60 | E | | Low | OUT | OUT |
| 68 | 65 | 61 | $\overline{M1}$ | | High | High | High |
| 69 | 66 | 62 | $\overline{WR}$ | | High | 3T | High |
| 70 | 67 | 63 | $\overline{RD}$ | | High | 3T | High |
| 71 | 68 | 64 | PHI | | OUT | OUT | OUT |
| 72 | 1 | 1 | $V_{SS}$ | | GND | GND | GND |
| 73 | 2 | | $V_{SS}$ | | GND | GND | GND |
| 74 | 3 | 2 | XTAL | | OUT | OUT | OUT |
| 75 | | | NC | | | | |

## OPERATION MODES (Continued)

The Z8S180/Z8L180 leaves HALT mode in response to:

- Low on $\overline{\text{RESET}}$
- Interrupt from an enabled on-chip source
- External request on $\overline{\text{NMI}}$
- Enabled external request on $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, or $\overline{\text{INT2}}$

In case of an interrupt, the return address is the instruction following the HALT instruction. The program can either branch back to the HALT instruction to wait for another interrupt or can examine the new state of the system/application and respond appropriately.

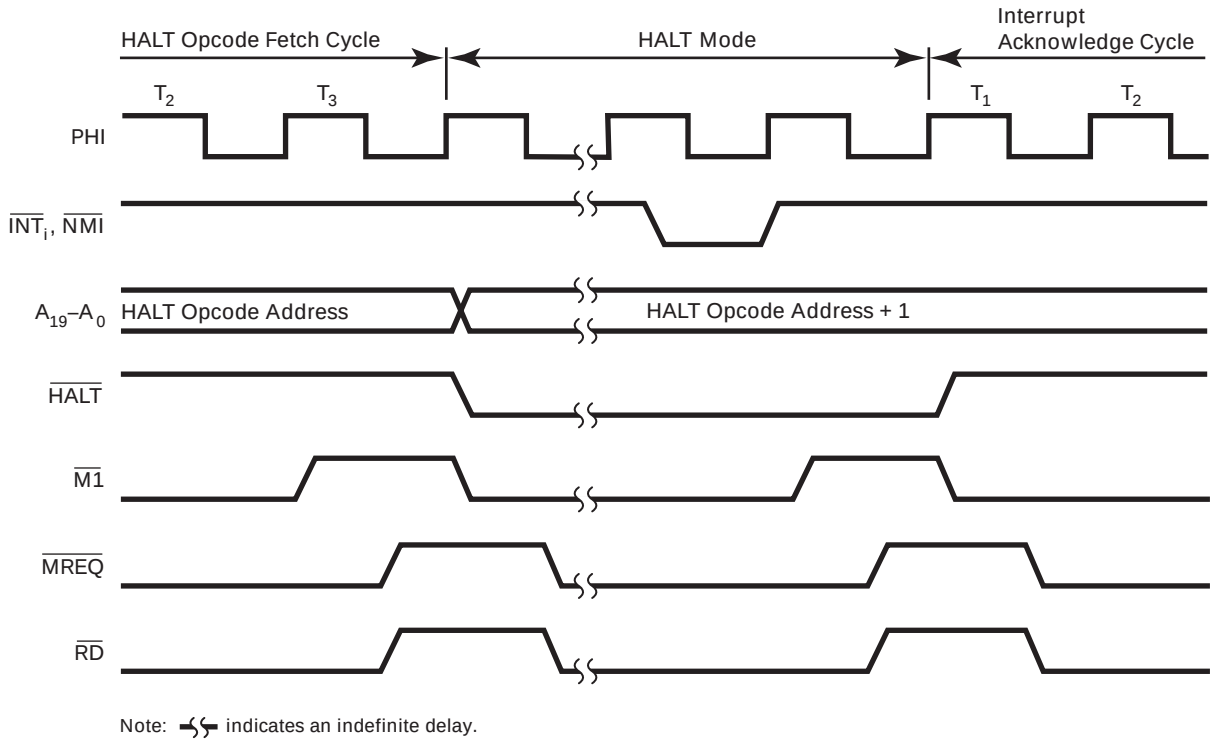


**Figure 13. HALT Timing**

**SLEEP Mode.** This mode is entered by keeping the IOSTOP bit (ICR5) and bits 3 and 6 of the CPU Control Register (CCR3, CCR6) all zero and executing the SLP instruction. The oscillator and PHI output continue operating, but are blocked from the CPU core and DMA channels to reduce power consumption. DRAM refresh stops, but interrupts and granting to an external Master can occur. Except when the bus is granted to an external Master, A19–0 and all control signals except $\overline{\text{HALT}}$ are maintained High. $\overline{\text{HALT}}$ is Low. I/O operations continue as before the SLP instruction, except for the DMA channels.

The Z8S180/Z8L180 leaves SLEEP mode in response to a Low on $\overline{\text{RESET}}$, an interrupt request from an on-chip source, an external request on $\overline{\text{NMI}}$, or an external request on $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, or $\overline{\text{INT2}}$.

If an interrupt source is individually disabled, it cannot bring the Z8S180/Z8L180 out of SLEEP mode. If an interrupt source is individually enabled, and the IEF bit is 1 so that interrupts are globally enabled (by an EI instruction), the highest priority active interrupt occurs with the return address being the instruction after the SLP instruction. If an interrupt source is individually enabled, but the IEF bit is 0 so that interrupts are globally disabled (by a DI instruction), the Z8S180/Z8L180 leaves SLEEP mode by simply executing the following instruction(s).

## OPERATION MODES (Continued)

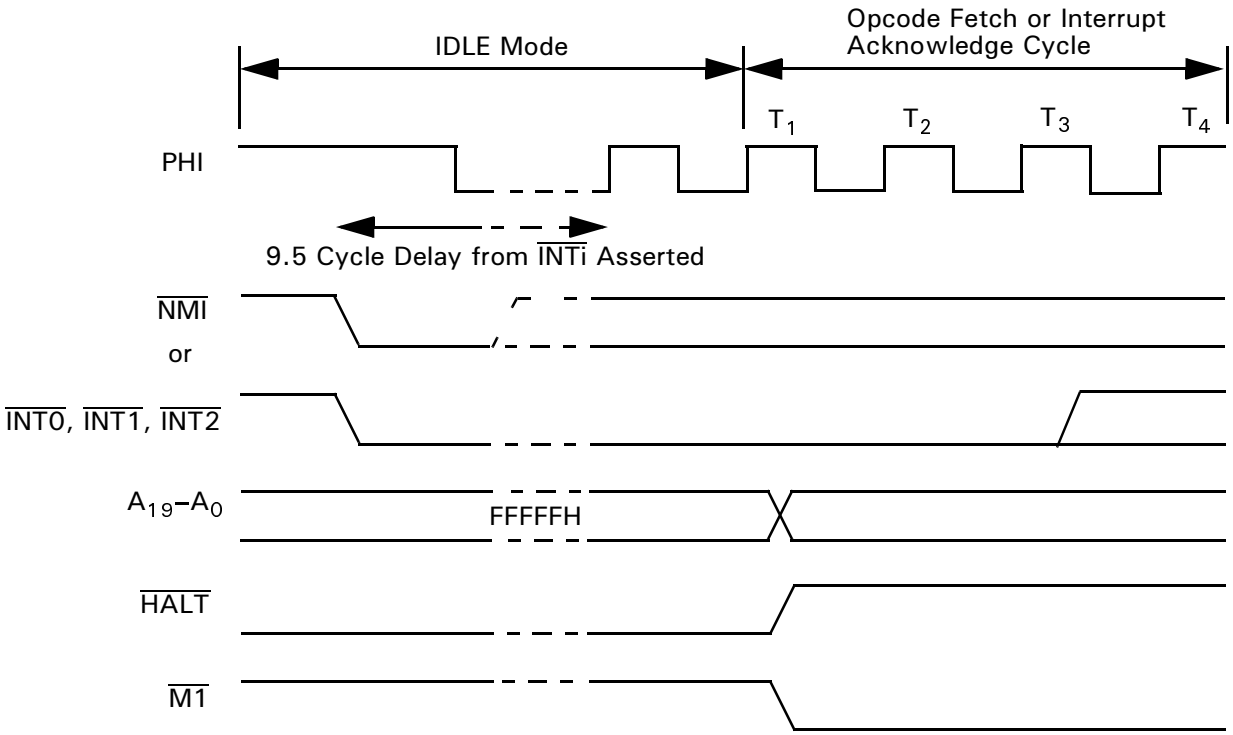


**Figure 15. Z8S180/Z8L180 IDLE Mode Exit Due To External Interrupt**

While the Z8S180/Z8L180 is in IDLE mode, it grants the bus to an external Master if the BREXT bit (CCR5) is 1. Figure 16 depicts the timing for this sequence.

**Note:** A response to a bus request takes 8 clock cycles longer than in normal operation.

After the external Master negates the Bus Request, the Z8S180/Z8L180 disables the PHI clock and remains in IDLE mode.

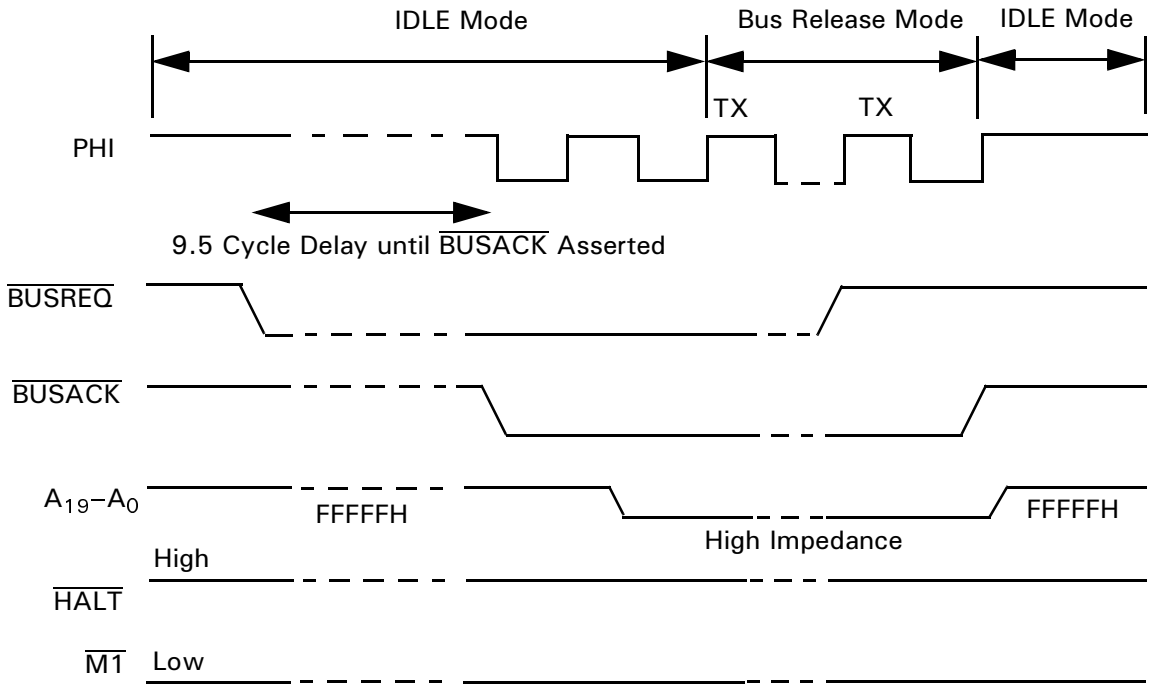


**Figure 16. Bus Granting to External Master in IDLE Mode**

**STANDBY Mode (With or Without QUICK RECOVERY).**

Software can put the Z8S180/Z8L180 into this mode by setting the IOSTOP bit (ICR5) to 1, CCR6 to 1, and executing the SLP instruction. This mode stops the on-chip oscillator and thus draws the least power of any mode, less than 10µA.

As with IDLE mode, the Z8S180/Z8L180 leaves STANDBY mode in response to a Low on $\overline{\text{RESET}}$, on $\overline{\text{NMI}}$, or a Low on $\overline{\text{INT0–2}}$ that is enabled by a 1 in the corresponding bit in the INT/TRAP Control Register. This action grants the bus to an external Master if the BREXT bit in the CPU Control Register (CCR5) is 1. The time required for all of these operations is greatly increased by the necessity for restarting the on-chip oscillator, and ensuring that it stabilizes to square-wave operation.

When an external clock is connected to the EXTAL pin rather than a crystal to the XTAL and EXTAL pins and the external clock runs continuously, there is little necessity to use STANDBY mode because no time is required to restart the oscillator, and other modes restart faster. However, if external logic stops the clock during STANDBY mode (for example, by decoding $\overline{\text{HALT}}$ Low and $\overline{\text{M1}}$ High for several clock cycles), then STANDBY mode can be useful to allow the external clock source to stabilize after it is re-enabled.

When external logic drives $\overline{\text{RESET}}$ Low to bring the device out of STANDBY mode, and a crystal is in use or an external clock source is stopped, the external logic must hold $\overline{\text{RESET}}$ Low until the on-chip oscillator or external clock source is restarted and stabilized.

The clock-stability requirements of the Z8S180/Z8L180 are much less in the divide-by-two mode that is selected by a RESET sequence and controlled by the Clock Divide bit in the CPU Control Register (CCR7). As a result, software performs the following actions:

1. Sets CCR7 to 0 for divide-by-two mode before an SLP instruction and STANDBY mode.
2. Delays setting CCR7 back to 1 for divide-by-one mode as long as possible to allow additional clock stabilization time after a RESET, interrupt, or in-line RESTART after an SLP 01 instruction.

If CCR6 is set to 1 before the SLP instruction places the MPU in STANDBY mode, the value of the CCR3 bit determines the length of the delay before the oscillator restarts and stabilizes when it leaves STANDBY mode due to an external interrupt request. When CCR3 is 0, the Z8S180/Z8L180 waits $2^{17}$ (131,072) clock cycles. When CCR3 is 1, it waits 64 clock cycles. This state is called QUICK RECOVERY mode. The same delay applies to grant-

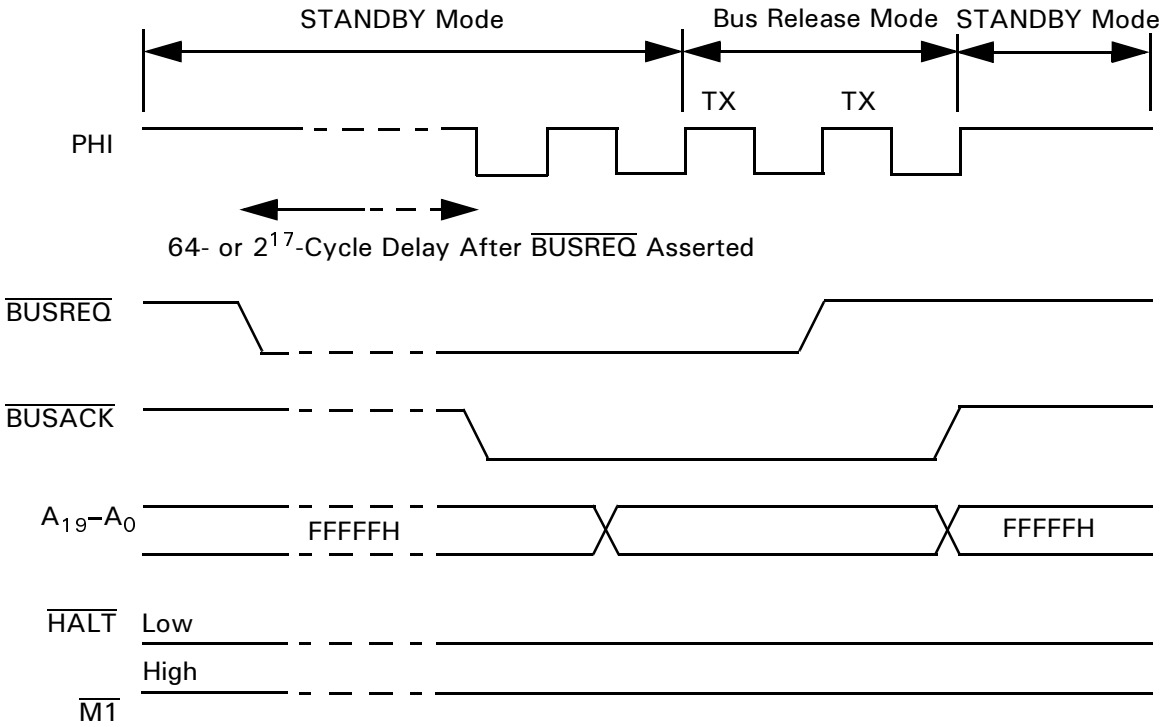


**Figure 18. Bus Granting to External Master During STANDBY Mode**

## STANDARD TEST CONDITIONS

The following standard test conditions apply to DC Characteristics, unless otherwise noted. All voltages are referenced to $V_{SS}$ (0V). Positive current flows into the referenced pin.

All AC parameters assume a load capacitance of 100 pF. Add a 10-ns delay for each 50-pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to $V_{OL}$ MAX or $V_{OL}$ MIN as indicated in Figures 20 through 30 (except for CLOCK, which is referenced to the 10% and 90% points). Ordering Information lists temperature ranges and product numbers. Find package drawings in Package Information.

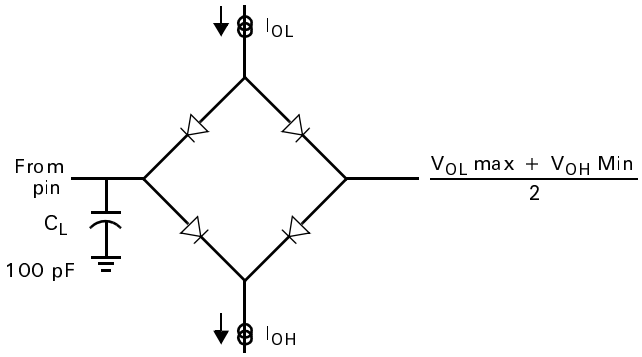


**Figure 19. AC Parameter Test Circuit**

## ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | –0.3 ~ +7.0 | V |
| Input Voltage | $V_{IN}$ | –0.3 ~ $V_{cc}$ +0.3 | V |
| Operating Temperature | $T_{OPR}$ | 0 ~ 70 | °C |
| Extended Temperature | $T_{EXT}$ | –40 ~ 85 | °C |
| Storage Temperature | $T_{STG}$ | –55 ~ +150 | °C |

**Note:** Permanent damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability.

## DC CHARACTERISTICS—Z8S180

**Table 6. Z8S180 DC Characteristics**
**$V_{DD}$ = 5V ±10%; $V_{SS}$ = 0V**

| Symbol | Item | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH1}$ | Input H Voltage<br>$\overline{RESET}$, EXTAL, $\overline{NMI}$ | | $V_{DD}$ –0.6 | — | $V_{DD}$ +0.3 | V |
| $V_{IH2}$ | Input H Voltage<br>Except $\overline{RESET}$, EXTAL, $\overline{NMI}$ | | 2.0 | — | $V_{DD}$ +0.3 | V |
| $V_{IH3}$ | Input H Voltage<br>CKS, CKA0, CKA1 | | 2.4 | — | $V_{DD}$ +0.3 | V |
| $V_{IL1}$ | Input L Voltage<br>RESET, EXTAL, NMI | | –0.3 | — | 0.6 | V |
| $V_{IL2}$ | Input L Voltage<br>Except RESET, EXTAL, NMI | | –0.3 | — | 0.8 | V |
| $V_{OH}$ | Outputs H Voltage<br>All outputs | $I_{OH}$ = –200 µA | 2.4 | — | — | V |
| | | $I_{OH}$ = –20 µA | $V_{DD}$ –1.2 | — | — | |
| $V_{OL}$ | Outputs L Voltage<br>All outputs | $I_{OL}$ = 2.2 mA | — | — | 0.45 | V |
| $I_{IL}$ | Input Leakage<br>Current All Inputs<br>Except XTAL, EXTAL | $V_{IN}$ = 0.5 ~ $V_{DD}$ –0.5 | — | — | 1.0 | µA |
| $I_{TL}$ | Three State Leakage<br>Current | $V_{IN}$ = 0.5 ~ $V_{DD}$ –0.5 | — | — | 1.0 | µA |
| $I_{DD}$[1] | Power Dissipation<br>(Normal Operation) | F = 10 MHz | — | 25 | 60 | mA |
| | | 20 | | 30 | 50 | |
| | | 33 | | 60 | 100 | |
| | Power Dissipation<br>(SYSTEM STOP mode) | F = 10 MHz | — | 2 | 5 | |
| | | 20 | | 3 | 6 | |
| | | 33 | | 5 | 9 | |
| $C_P$ | Pin Capacitance | $V_{IN}$ = $0_V$, f = 1 MHz<br>$T_A$ = 25°C | — | — | 12 | pF |

**Note:**
1. $V_{IHmin}$ = $V_{DD}$–1.0V, $V_{ILmax}$ = 0.8V (All output terminals are at NO LOAD.) $V_{DD}$ = 5.0V.

## AC CHARACTERISTICS—Z8S180 (Continued)

**Table 8. Z8S180 AC Characteristics (Continued)**
**$V_{DD}$ = 5V ±10% or $V_{DD}$ = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation**

| | | | Z8S180—20 MHz | | Z8S180—33 MHz | | |
|---|---|---|---|---|---|---|---|
| **Number** | **Symbol** | **Item** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| 32 | $t_{INTH}$ | $\overline{INT}$ Hold Time from PHI Fall | 10 | — | 10 | — | ns |
| 33 | $t_{NMIW}$ | $\overline{NMI}$ Pulse Width | 35 | — | 25 | — | ns |
| 34 | $t_{BRS}$ | $\overline{BUSREQ}$ Set-up Time to PHI Fall | 10 | — | 10 | — | ns |
| 35 | $t_{BRH}$ | $\overline{BUSREQ}$ Hold Time from PHI Fall | 10 | — | 10 | | ns |
| 36 | $t_{BAD1}$ | PHI Rise to $\overline{BUSACK}$ Fall Delay | — | 25 | — | 15 | ns |
| 37 | $t_{BAD2}$ | PHI Fall to $\overline{BUSACK}$ Rise Delay | — | 25 | — | 15 | ns |
| 38 | $t_{BZD}$ | PHI Rise to Bus Floating Delay Time | — | 40 | — | 30 | ns |
| 39 | $t_{MEWH}$ | $\overline{MREQ}$ Pulse Width (High) | 35 | — | 25 | — | ns |
| 40 | $t_{MEWL}$ | $\overline{MREQ}$ Pulse Width (Low) | 35 | — | 25 | — | ns |
| 41 | $t_{RFD1}$ | PHI Rise to $\overline{RFSH}$ Fall Delay | — | 20 | — | 15 | ns |
| 42 | $t_{RFD2}$ | PHI Rise to $\overline{RFSH}$ Rise Delay | — | 20 | — | 15 | ns |
| 43 | $t_{HAD1}$ | PHI Rise to $\overline{HALT}$ Fall Delay | — | 15 | — | 15 | ns |
| 44 | $t_{HAD2}$ | PHI Rise to $\overline{HALT}$ Rise Delay | — | 15 | — | 15 | ns |
| 45 | $t_{DRQS}$ | $\overline{DREQ1}$ Set-up Time to PHI Rise | 20 | — | 15 | — | ns |
| 46 | $t_{DRQH}$ | $\overline{DREQ1}$ Hold Time from PHI Rise | 20 | — | 15 | — | ns |
| 47 | $t_{TED1}$ | PHI Fall to $\overline{TENDi}$ Fall Delay | — | 25 | — | 15 | ns |
| 48 | $t_{TED2}$ | PHI Fall to $\overline{TENDi}$ Rise Delay | — | 25 | — | 15 | ns |
| 49 | $t_{ED1}$ | PHI Rise to E Rise Delay | — | 30 | — | 15 | ns |
| 50 | $t_{ED2}$ | PHI Fall or Rise to E Fall Delay | — | 30 | — | 15 | ns |
| 51 | $P_{WEH}$ | E Pulse Width (High) | 25 | — | 20 | — | ns |
| 52 | $P_{WEL}$ | E Pulse Width (Low) | 50 | — | 40 | — | ns |
| 53 | $t_{Er}$ | Enable Rise Time | — | 10 | — | 10 | ns |
| 54 | $t_{Ef}$ | Enable Fall Time | — | 10 | — | 10 | ns |
| 55 | $t_{TOD}$ | PHI Fall to Timer Output Delay | — | 75 | — | 50 | ns |
| 56 | $t_{STDI}$ | CSI/O Transmit Data Delay Time (Internal Clock Operation) | — | 2 | — | 2 | tcyc |
| 57 | $t_{STDE}$ | CSI/O Transmit Data Delay Time (External Clock Operation) | — | 7.5 $t_{CYC}$ +75 | — | 75 $t_{CYC}$ +60 | ns |
| 58 | $t_{SRSI}$ | CSI/O Receive Data Set-up Time (Internal Clock Operation) | 1 | — | 1 | — | tcyc |
| 59 | $t_{SRHI}$ | CSI/O Receive Data Hold Time (Internal Clock Operation) | 1 | — | 1 | — | tcyc |
| 60 | $t_{SRSE}$ | CSI/O Receive Data Set-up Time (External Clock Operation) | 1 | — | 1 | — | tcyc |
| 61 | $t_{SRHE}$ | CSI/O Receive Data Hold Time (External Clock Operation) | 1 | — | 1 | — | tcyc |
| 62 | $t_{RES}$ | $\overline{RESET}$ Set-up Time to PHI Fall | 40 | — | 25 | — | ns |

## ASCI STATUS REGISTER 0,1

Each ASCI channel status register (STAT0,1) allows interrogation of ASCI communication, error and modem control signal status, and the enabling or disabling of ASCI interrupts.

ASCI Status Register 0 (STAT0: I/O Address = 04H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | RDRF | OVRN | PE | FE | RE | $\overline{DCD0}$ | TDRE | TIE |
| | R | R | R | R | R/W | R | R | R/W |

ASCI Status Register 1 (STAT1: I/O Address = 05H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | RDRF | OVRN | PE | FE | RE | CTS1E | TDRE | TIE |
| | R | R | R | R | R/W | R/W | R | R/W |

**Figure 35. ASCI Status Registers**

**RDRF: Receive Data Register Full (Bit 7).** RDRF is set to 1 when an incoming data byte is loaded into an empty Rx FIFO. If a framing or parity error occurs, RDRF is still set and the receive data (which generated the error) is still loaded into the FIFO. RDRF is cleared to 0 by reading RDR and most recently received character in the FIFO from IOSTOP mode, during RESET and for ASCI0 if the $\overline{DCD0}$ input is auto-enabled and is negated (High).

**OVRN: Overrun Error (Bit 6).** An overrun condition occurs if the receiver finishes assembling a character but the Rx FIFO is full so there is no room for the character. However, this status bit is not set until the most recent character received before the overrun becomes the oldest byte in the FIFO. This bit is cleared when software writes a 1 to the EFR bit in the CNTLA register. The bit may also be cleared by RESET in IOSTOP mode or ASCI0 if the $\overline{DCD0}$ pin is auto enabled and is negated (High).

**Note:** When an overrun occurs, the receiver does not place the character in the shift register into the FIFO, nor any subsequent characters, until the most recent good character enters the top of the FIFO so that OVRN is set. Software then writes a 1 to EFR to clear it.

**PE: Parity Error (Bit 5).** A parity error is detected when parity checking is enabled.When the MOD1 bit in the CNTLA register is 1, a character is assembled in which the parity does not match the PEO bit in the CNTLB register. However, this status bit is not set until or unless the error character becomes the oldest one in the Rx FIFO. PE is cleared when software writes a 1 to the EFR bit in the CNTRLA register. PE is also cleared by RESET in IOSTOP mode, or on ASCI0, if the $\overline{DCD0}$ pin is auto-enabled and is negated (High).

**FE: Framing Error (Bit 4).** A framing error is detected when the stop bit of a character is sampled as 0/SPACE. However, this status bit is not set until/unless the error character becomes the oldest one in the Rx FIFO. FE is cleared when software writes a 1 to the EFR bit in the CNTLA register. FE is also cleared by RESET in IOSTOP mode, or on ASCI0, if the $\overline{DCD0}$ pin is auto-enabled and is negated (High).

**REI: Receive Interrupt Enable (Bit 3).** RIE should be set to 1 to enable ASCI receive interrupt requests. When RIE is 1, the Receiver requests an interrupt when a character is received and RDRF is set, but only if neither DMA channel requires its request-routing field to be set to receive data from this ASCI. That is, if SM1–0 are 11 and SAR17–16 are 10, or DIM1 is 1 and IAR17–16 are 10, then ASCI1 does not request an interrupt for RDRF. If RIE is 1, either ASCI requests an interrupt when OVRN, PE or FE is set, and

ASCI0 requests an interrupt when $\overline{DCD0}$ goes High. RIE is cleared to 0 by RESET.

**$\overline{DCD0}$: Data Carrier Detect (Bit 2 STAT0).** This bit is set to 1 when the pin is High. It is cleared to 0 on the first READ of STAT0 following the pin's transition from High to Low and during RESET. When bit 6 of the ASEXT0 register is 0 to select auto-enabling, and the pin is negated (High), the receiver is reset and its operation is inhibited.

**$\overline{CTS1E}$: Clear To Send (Bit 2 STAT1).** Channel 1 features an external $\overline{CTS1}$ input, which is multiplexed with the receive data pin RSX for the CSI/O. Setting this bit to 1 selects the CTS1 function; clearing the bit to 0 selects the RXS function.

**TDRE: Transmit Data Register Empty (Bit 1).** TDRE = 1 indicates that the TDR is empty and the next transmit data byte is written to TDR. After the byte is written to TDR, TDRE is cleared to 0 until the ASCI transfers the byte from TDR to the TSR and then TDRE is again set to 1. TDRE is set to 1 in IOSTOP mode and during RESET. On ASCI0, if the $\overline{CTS0}$ pin is auto-enabled in the ASEXT0 register and the pin is High, TDRE is reset to 0.

**TIE: Transmit Interrupt Enable (Bit 0).** TIE should be set to 1 to enable ASCI transmit interrupt requests. If TIE = 1, an interrupt is requested when TDRE = 1. TIE is cleared to 0 during RESET.

## ASCI TRANSMIT DATA REGISTERS

Register addresses 06H and 07H hold the ASCI transmit data for channel 0 and channel 1, respectively.

### ASCI Transmit Data Registers Channel 0

**Mnemonic TDR0**
**Address 06H**

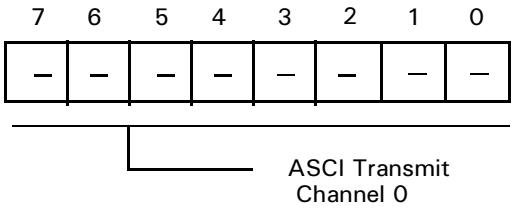


**Figure 36. ASCI Register**

### ASCI Transmit Data Registers Channel 1

**Mnemonic TDR1**
**Address 07H**

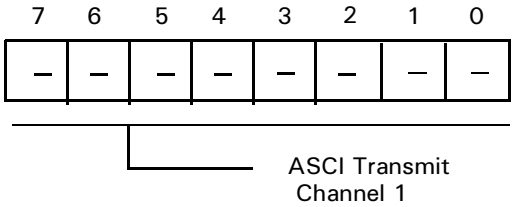


**Figure 37. ASCI Register**

## TIMER CONTROL REGISTER

The Timer Control Register (TCR) monitors both channels (PRT0, PRT1) TMDR status. It also controls the enabling and disabling of down-counting and interrupts, and controls the output pin A18/$T_{OUT}$ for PRT1.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | TIF1 | TIF0 | TIE1 | TIE0 | TOC1 | TOC0 | TDE1 | TDE0 |
| | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

**Figure 46. Timer Control Register (TCR: I/O Address = 10H)**

**TIF1: Timer Interrupt Flag 1 (Bit 7) .** When TMDR1 decrements to 0, TIF1 is set to 1. This condition generates an interrupt request if enabled by TIE1 = 1. TIF1 is reset to 0 when TCR is read and the higher or lower byte of TMDR1 is read. During RESET, TIF1 is cleared to 0.

**TIF0: Timer Interrupt Flag 0 (Bit 6).** When TMDR0 decrements to 0, TIF0 is set to 1. This condition generates an interrupt request if enabled by TIE0 = 1. TIF0 is reset to 0 when TCR is read and the higher or lower byte of TMDR0 is read. During RESET, TIF0 is cleared to 0.

**TIE1: Timer Interrupt Enable 1 (Bit 5).** When TIE0 is set to 1, TIF1 = 1 generates a CPU interrupt request. When TIE0 is reset to 0, the interrupt request is inhibited. During RESET, TIE0 is cleared to 0.

**TOC1, 0: Timer Output Control (Bits 3, 2).** TOC1 and TOC0 control the output of PRT1 using the multiplexed A18/$T_{OUT}$ pin as indicated in Table 12. During RESET, TOC1 and TOC0 are cleared to 0. If bit 3 of the IAR1B register is 1, the $T_{OUT}$ function is selected. By programming TOC1 and TOC0, the A18/$T_{OUT}$ pin can be forced High, Low, or toggled when TMDR1 decrements to 0.

**Table 12. Timer Output Control**

| TOC1 | TOC0 | Output | |
|---|---|---|---|
| 0 | 0 | Inhibited | The A18/$T_{OUT}$ pin is not affected by the PRT |
| 0 | 1 | Toggled | If bit 3 of IAR1B is 1, the A18/$T_{OUT}$ pin is toggled or set Low or High as indicated |
| 1 | 0 | 0 | |
| 1 | 1 | 1 | |

**TDE1, 0: Timer Down Count Enable (Bits 1, 0).** TDE1 and TDE0 enable and disable down-counting for TMDR1 and TMDR0, respectively. When TDEn (n = 0,1) is set to 1, down-counting is stopped and TMDRn is freely read or written. TDE1 and TDE0 are cleared to 0 during RESET and TMDRn does not decrement until TDEn is set to 1.

## DMA DESTINATION ADDRESS REGISTER CHANNEL 0

The DMA Destination Address Register Channel 0 specifies the physical destination address for channel 0 transfers. The register contains 20 bits and can specify up to 1024-KB memory addresses or up to 64-KB I/O addresses. Channel 0 destination can be memory, I/O, or memory mapped I/O. For I/O, the MS bits of this register identify the Request Handshake signal for channel 0.

### DMA Destination Address Register Channel 0 Low

**Mnemonic DAR0L**
**Address 23H**

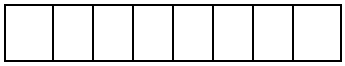

**Figure 58. DMA Destination Address Register Channel 0 Low**

### DMA Destination Address Register Channel 0 High

**Mnemonic DAR0H**
**Address 24H**

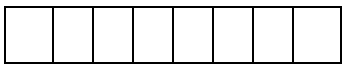

**Figure 59. DMA Destination Address Register Channel 0 High**

### DMA Destination Address Register Channel 0B

**Mnemonic DAR0B**
**Address 25H**

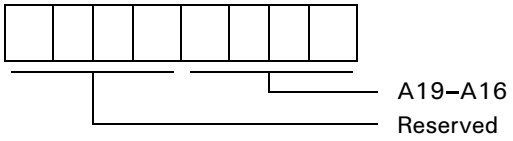


**Figure 60. DMA Destination Address Register Channel 0B**

If the DMA destination is in I/O space, bits 1–0 of this register select the DMA request signal for DMA0, as follows:

| Bit 1 (A17) | Bit 0 (A16) | DMA Transfer Request |
|---|---|---|
| 0 | 0 | DREQ0 (external) |
| 0 | 1 | TDR0 (ASCI0) |
| 1 | 0 | TDR1 (ASCI1) |
| 1 | 1 | Not Used |

## DMA BYTE COUNT REGISTER CHANNEL 0

The DMA Byte Count Register Channel 0 specifies the number of bytes to be transferred. This register contains 16 bits and may specify up to 64-KB transfers. When one byte is transferred, the register is decremented by one. If n bytes should be transferred, n must be stored before the DMA operation.

**Note:** All DMA Count Register channels are undefined during RESET.

### DMA Byte Count Register Channel 0 Low

**Mnemonic BCR0L**
**Address 26H**

**Figure 61. DMA Byte Count Register 0 Low**

### DMA Byte Count Register Channel 0 High

**Mnemonic BCR0H**
**Address 27H**

**Figure 62. DMA Byte Count Register 0 High**

### DMA Byte Count Register Channel 1 Low

**Mnemonic BCR1L**
**Address 2EH**

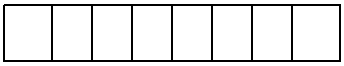

**Figure 63. DMA Byte Count Register 1 Low**

### DMA Byte Count Register Channel 1 High

**Mnemonic BCR1H**
**Address 2FH**

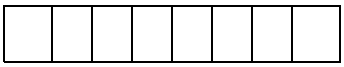

**Figure 64. DMA Byte Count Register 1 High**

## DMA MEMORY ADDRESS REGISTER CHANNEL 1

The DMA Memory Address Register Channel 1 specifies the physical memory address for channel 1 transfers. The address may be a destination or a source memory location. The register contains 20 bits and may specify up to 1024 KB memory addresses.

### DMA Memory Address Register, Channel 1L

**Mnemonic MAR1L**
**Address 28H**

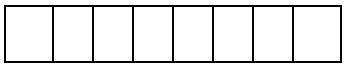

**Figure 65. DMA Memory Address Register, Channel 1L**

### DMA Memory Address Register, Channel 1H

**Mnemonic MAR1H**
**Address 29H**

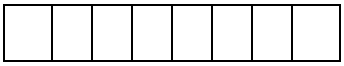

**Figure 66. DMA Memory Address Register, Channel 1H**

### DMA Memory Address Register, Channel 1B

**Mnemonic MAR1B**
**Address 2AH**

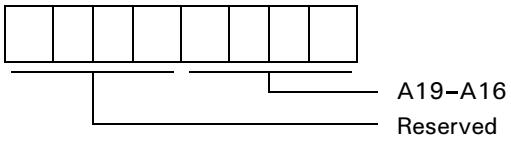


**Figure 67. DMA Memory Address Register, Channel 1B**

## DMA MODE REGISTER

The DMA Mode Register (DMODE) is used to set the addressing and transfer mode for channel 0.

### DMA Mode Register

**Mnemonic DMODE**
**Address 31H**

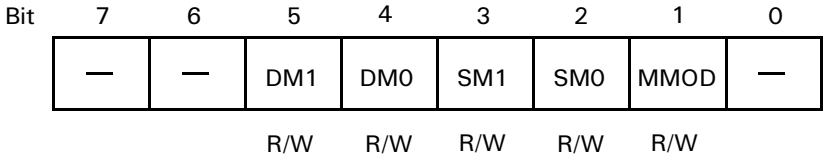


**Figure 72. DMA Mode Register (DMODE: I/O Address = 31H)**

**DM1, DM0: Destination Mode Channel 0 (Bits 5,4).** This mode specifies whether the destination for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred. DM1 and DM0 are cleared to 0 during RESET.

**Table 14. Channel 0 Destination**

| DM1 | DM0 | Memory I/O | Memory Increment/Decrement |
|---|---|---|---|
| 0 | 0 | Memory | +1 |
| 0 | 1 | Memory | –1 |
| 1 | 0 | Memory | fixed |
| 1 | 1 | I/O | fixed |

**SM1, SM0: Source Mode Channel 0 (Bits 3, 2) .** This mode specifies whether the source for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred.

**Table 15. Channel 0 Source**

| SM1 | SM0 | Memory I/O | Memory Increment/Decrement |
|---|---|---|---|
| 0 | 0 | Memory | +1 |
| 0 | 1 | Memory | –1 |
| 1 | 0 | Memory | fixed |
| 1 | 1 | I/O | fixed |

Table 16 indicates all DMA transfer mode combinations of DM0, DM1, SM0, and SM1. Because I/O to/from I/O transfers are not implemented, 12 combinations are available.

**Table 16. Transfer Mode Combinations**

| DM1 | DM0 | SM1 | SM0 | Transfer Mode | Address Increment/Decrement |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Memory→Memory | SAR0 + 1, DAR0 + 1 |
| 0 | 0 | 0 | 1 | Memory→Memory | SAR0–1, DAR0 + 1 |
| 0 | 0 | 1 | 0 | Memory*→Memory | SAR0 fixed, DAR0 + 1 |
| 0 | 0 | 1 | 1 | I/O→Memory | SAR0 fixed, DAR0 + 1 |
| 0 | 1 | 0 | 0 | Memory→Memory | SAR0 + 1, DAR0–1 |
| 0 | 1 | 0 | 1 | Memory→Memory | SAR0–1, DAR0–1 |
| 0 | 1 | 1 | 0 | Memory*→Memory | SAR0 fixed, DAR0–1 |
| 0 | 1 | 1 | 1 | I/O→Memory | SAR0 fixed, DAR0–1 |
| 1 | 0 | 0 | 0 | Memory→Memory* | SAR0 + 1, DAR0 fixed |
| 1 | 0 | 0 | 1 | Memory→Memory* | SAR0–1, DAR0 fixed |
| 1 | 0 | 1 | 0 | Reserved | |
| 1 | 0 | 1 | 1 | Reserved | |
| 1 | 1 | 0 | 0 | Memory→I/O | SAR0 + 1, DAR0 fixed |
| 1 | 1 | 0 | 1 | Memory→I/O | SAR0–1, DAR0 fixed |
| 1 | 1 | 1 | 0 | Reserved | |
| 1 | 1 | 1 | 1 | Reserved | |

**Note:** * Includes memory mapped I/O.

**MMOD: Memory Mode Channel 0 (Bit 1).** When channel 0 is configured for memory to/from memory transfers there is no Request Handshake signal to control the transfer timing. Instead, two automatic transfer timing modes are selectable: burst (MMOD = 1) and cycle steal (MMOD = 0). For burst memory to/from memory transfers, the DMAC takes control of the bus continuously until the DMA transfer completes (as indicated by the byte count register = 0). In cycle steal mode, the CPU is provided a cycle for each DMA byte transfer cycle until the transfer is completed.

For channel 0 DMA with I/O source or destination, the selected Request signal times the transfer ignoring MMOD. MMOD is cleared to 0 during RESET.

## REFRESH CONTROL REGISTER

**Mnemonic RCR**
**Address 36H**

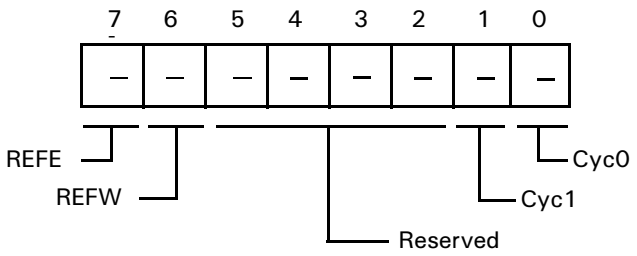


**Figure 77. Refresh Control Register (RCR: I/O Address = 36H)**

The Refresh Control Register (RCR) specifies the interval and length of refresh cycles, while enabling or disabling the refresh function.

**REFE: Refresh Enable (Bit 7).** REFE = 0 disables the refresh controller, while REFE = 1 enables refresh cycle insertion. REFE is set to 1 during RESET.

**REFW: Refresh Wait (Bit 6).** REFW = 0 causes the refresh cycle to be two clocks in duration. REFW = 1 causes the refresh cycle to be three clocks in duration by adding a refresh wait cycle (TRW). REFW is set to 1 during RESET.

**CYC1, 0: Cycle Interval (Bit 1,0).** CYC1 and CYC0 specify the interval (in clock cycles) between refresh cycles. When dynamic RAM requires 128 refresh cycles every 2 ms (or 256 cycles in every 4 ms), the required refresh interval is less than or equal to 15.625 µs. Thus, the underlined values indicate the best refresh interval depending on CPU clock frequency. CYC0 and CYC1 are cleared to 0 during RESET (see Table 18).

**Table 18. DRAM Refresh Intervals**

| | | | Time Interval | | | | |
|---|---|---|---|---|---|---|---|
| **CYC1** | **CYC0** | **Insertion Interval** | **PHI: 10 MHz** | **8 MHz** | **6 MHz** | **4 MHz** | **2.5 MHz** |
| 0 | 0 | 10 states | (1.0 µs)* | (1.25 µs)* | 1.66 µs | 2.5 µs | 4.0 µs |
| 0 | 1 | 20 states | (2.0 µs)* | (2.5 µs)* | 3.3 µs | 5.0 µs | 8.0 µs |
| 1 | 0 | 40 states | (4.0 µs)* | (5.0 µs)* | 6.6 µs | 10.0 µs | 16.0 µs |
| 1 | 1 | 80 states | (8.0 µs)* | (10.0 µs)* | 13.3 µs | 20.0 µs | 32.0 µs |

**Note:** *calculated interval.

**Refresh Control and Reset.** After RESET, based on the initialized value of RCR, refresh cycles occur with an interval of 10 clock cycles and be 3 clock cycles in duration.

### Dynamic RAM Refresh Operation

1. Refresh Cycle insertion is stopped when the CPU is in the following states:
   a. During RESET
   b. When the bus is released in response to $\overline{\text{BUSREQ}}$
   c. During SLEEP mode
   d. During $\overline{\text{WAIT}}$ states
2. Refresh cycles are suppressed when the bus is released in response to $\overline{\text{BUSREQ}}$. However, the refresh timer continues to operate. The time at which the first refresh cycle occurs after the Z8S180/Z8L180 reacquires the bus depends on the refresh timer. This cycle offers no timing relationship with the bus exchange.
3. Refresh cycles are suppressed during SLEEP mode. If a refresh cycle is requested during SLEEP mode, the refresh cycle request is internally latched (until replaced with the next refresh request). The latched refresh cycle is inserted at the end of the first machine cycle after SLEEP mode is exited. After this initial cycle, the time at which the next refresh cycle occurs depends on the refresh time and offers no relationship with the exit from SLEEP mode.
4. The refresh address is incremented by one for each successful refresh cycle, not for each refresh. Thus, independent of the number of missed refresh requests, each refresh bus cycle uses a refresh address incremented by one from that of the previous refresh bus cycles.

**CA3–CA0:CA (Bits 7–4).** CA specifies the start (Low) address (on 4-KB boundaries) for Common Area 1. This condition also determines the most recent address of the Bank Area. All bits of CA are set to 1 during RESET.

**BA3–BA0 (Bits 3–0).** BA specifies the start (Low) address (on 4-KB boundaries) for the Bank Area. This condition also determines the most recent address of Common Area 0. All bits of BA are set to 1 during RESET.

## OPERATION MODE CONTROL REGISTER

The Z8S180/Z8L180 is descended from two different ancestor processors, ZiLOG's original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR) can be programmed to select between certain differences between the Z80 and the 64180.

### Operation Mode Control Register

**Mnemonic OMCR**
**Address 3EH**

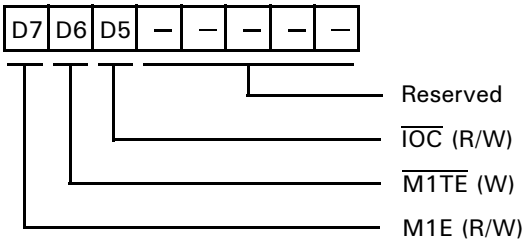


**Figure 81. Operating Control Register (OMCR: I/O Address = 3EH)**

**M1E ($\overline{M1}$ Enable).** This bit controls the $\overline{M1}$ output and is set to a 1 during reset.

When M1E = 1, the $\overline{M1}$ output is asserted Low during the opcode fetch cycle, the $\overline{INT0}$ acknowledge cycle, and the first machine cycle of the $\overline{NMI}$ acknowledge.

On the Z8S180/Z8L180, this choice makes the processor fetch one RETI instruction. When fetching a RETI from zero-wait-state memory, the processor uses three clock machine cycles that are not fully Z80-timing-compatible.

When M1E = 0, the processor does not drive $\overline{M1}$ Low during instruction fetch cycles. After fetching one RETI instruction with normal timing, the processor returns and refetches the instruction using Z80-compatible cycles that drive $\overline{M1}$ Low. This timing compatibility may be required by external Z80 peripherals to properly decode the RETI instruction.

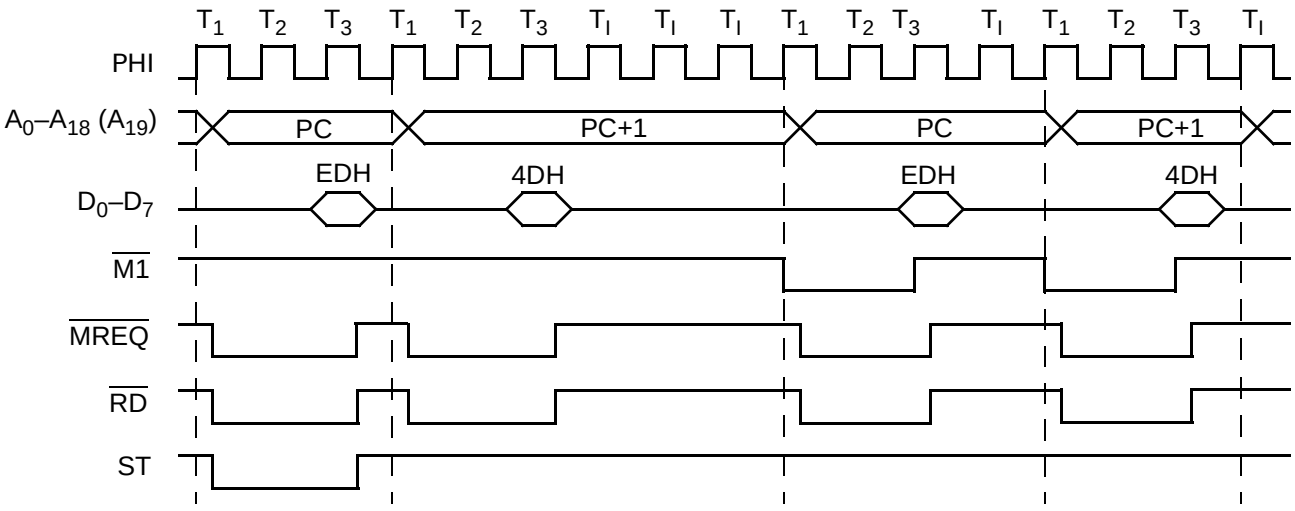


**Figure 82. RETI Instruction Sequence with M1E = 0**