# Zilog - Z8S18020FEC1960 Datasheet


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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z8S180 |
| Number of Cores/Bus Width | 1 Core, 8-Bit |
| Speed | 20MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 5.0V |
| Operating Temperature | -40°C ~ 100°C (TA) |
| Security Features | - |
| Package / Case | 80-BQFP |
| Supplier Device Package | 80-QFP |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8s18020fec1960 |

## PIN IDENTIFICATION (Continued)

**Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes**

| Pin Number and Package Type | | | | | Pin Status | | |
|---|---|---|---|---|---|---|---|
| QFP | PLCC | DIP | Default Function | Secondary Function | RESET | BUSACK | SLEEP |
| 1 | 9 | 8 | $\overline{NMI}$ | | IN | IN | IN |
| 2 | | | NC | | | | |
| 3 | | | NC | | | | |
| 4 | 10 | 9 | $\overline{INT0}$ | | IN | IN | IN |
| 5 | 11 | 10 | $\overline{INT1}$ | | IN | IN | IN |
| 6 | 12 | 11 | $\overline{INT2}$ | | IN | IN | IN |
| 7 | 13 | 12 | ST | | High | High | High |
| 8 | 14 | 13 | A0 | | 3T | 3T | High |
| 9 | 15 | 14 | A1 | | 3T | 3T | High |
| 10 | 16 | 15 | A2 | | 3T | 3T | High |
| 11 | 17 | 16 | A3 | | 3T | 3T | High |
| 12 | 18 | | $V_{SS}$ | | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ |
| 13 | 19 | 17 | A4 | | 3T | 3T | High |
| 14 | | | NC | | | | |
| 15 | 20 | 18 | A5 | | 3T | 3T | High |
| 16 | 21 | 19 | A6 | | 3T | 3T | High |
| 17 | 22 | 20 | A7 | | 3T | 3T | High |
| 18 | 23 | 21 | A8 | | 3T | 3T | High |
| 19 | 24 | 22 | A9 | | 3T | 3T | High |
| 20 | 25 | 23 | A10 | | 3T | 3T | High |
| 21 | 26 | 24 | A11 | | 3T | 3T | High |
| 22 | | | NC | | | | |
| 23 | | | NC | | | | |
| 24 | 27 | 25 | A12 | | 3T | 3T | High |
| 25 | 28 | 26 | A13 | | 3T | 3T | High |
| 26 | 29 | 27 | A14 | | 3T | 3T | High |
| 27 | 30 | 28 | A15 | | 3T | 3T | High |
| 28 | 31 | 29 | A16 | | 3T | 3T | High |
| 29 | 32 | 30 | A17 | | 3T | 3T | High |
| 30 | | | NC | | | | |
| 31 | 33 | 31 | A18 | | 3T | 3T | High |
| | | | $T_{OUT}$ | | N/A | OUT | OUT |
| 32 | 34 | 32 | $V_{DD}$ | | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ |
| 33 | 35 | | A19 | | 3T | 3T | High |
| 34 | 36 | 33 | $V_{SS}$ | | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ |
| 35 | 37 | 34 | D0 | | 3T | 3T | 3T |
| 36 | 38 | 35 | D1 | | 3T | 3T | 3T |
| 37 | 39 | 36 | D2 | | 3T | 3T | 3T |
| 38 | 40 | 37 | D3 | | 3T | 3T | 3T |

**Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)**

| Pin Number and Package Type | | | | | Pin Status | | |
|---|---|---|---|---|---|---|---|
| QFP | PLCC | DIP | Default Function | Secondary Function | RESET | BUSACK | SLEEP |
| 39 | 41 | 38 | D4 | | 3T | 3T | 3T |
| 40 | 42 | 39 | D5 | | 3T | 3T | 3T |
| 41 | 43 | 40 | D6 | | 3T | 3T | 3T |
| 42 | | | NC | | | | |
| 43 | | | NC | | | | |
| 44 | 44 | 41 | D7 | | 3T | 3T | 3T |
| 45 | 45 | 42 | $\overline{RTS0}$ | | High | OUT | High |
| 46 | 46 | 43 | $\overline{CTS0}$ | | IN | OUT | IN |
| 47 | 47 | 44 | $\overline{DCD0}$ | | IN | IN | IN |
| 48 | 48 | 45 | TXA0 | | High | OUT | OUT |
| 49 | 49 | 46 | RXA0 | | IN | IN | IN |
| 50 | 50 | 47 | CKA0 | | 3T | I/O | I/O |
| | | | $\overline{DREQ0}$ | | N/A | IN | IN |
| 51 | | | NC | | | | |
| 52 | 51 | 48 | TXA1 | | High | OUT | OUT |
| 53 | 52 | | TEST | | | | |
| 54 | 53 | 49 | RXA1 | | IN | IN | IN |
| 55 | 54 | 50 | CKA1 | | 3T | I/O | I/O |
| | | | $\overline{TEND0}$ | | N/A | High | High |
| 56 | 55 | 51 | TXS | | High | OUT | OUT |
| 57 | 56 | 52 | RXS | | IN | IN | IN |
| | | | $\overline{CTS1}$ | | N/A | IN | IN |
| 58 | 57 | 53 | CKS | | 3T | I/O | I/O |
| 59 | 58 | 54 | $\overline{DREQ1}$ | | IN | 3T | IN |
| 60 | 59 | 55 | $\overline{TEND1}$ | | High | OUT | High |
| 61 | 60 | 56 | $\overline{HALT}$ | | High | High | Low |
| 62 | | | NC | | | | |
| 63 | | | NC | | | | |
| 64 | 61 | 57 | $\overline{RFSH}$ | | High | OUT | High |
| 65 | 62 | 58 | $\overline{IORQ}$ | | High | 3T | High |
| 66 | 63 | 59 | $\overline{MREQ}$ | | High | 3T | High |
| 67 | 64 | 60 | E | | Low | OUT | OUT |
| 68 | 65 | 61 | $\overline{M1}$ | | High | High | High |
| 69 | 66 | 62 | $\overline{WR}$ | | High | 3T | High |
| 70 | 67 | 63 | $\overline{RD}$ | | High | 3T | High |
| 71 | 68 | 64 | PHI | | OUT | OUT | OUT |
| 72 | 1 | 1 | $V_{SS}$ | | GND | GND | GND |
| 73 | 2 | | $V_{SS}$ | | GND | GND | GND |
| 74 | 3 | 2 | XTAL | | OUT | OUT | OUT |
| 75 | | | NC | | | | |

## PIN IDENTIFICATION (Continued)

**Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)**

| Pin Number and Package Type | | | | | Pin Status | | |
|---|---|---|---|---|---|---|---|
| QFP | PLCC | DIP | Default Function | Secondary Function | RESET | BUSACK | SLEEP |
| 76 | 4 | 3 | EXTAL | | IN | IN | IN |
| 77 | 5 | 4 | $\overline{\text{WAIT}}$ | | IN | IN | IN |
| 78 | 6 | 5 | $\overline{\text{BUSACK}}$ | | High | OUT | OUT |
| 79 | 7 | 6 | $\overline{\text{BUSREQ}}$ | | IN | IN | IN |
| 80 | 8 | 7 | $\overline{\text{RESET}}$ | | IN | IN | IN |

## ARCHITECTURE

The Z180 combines a high-performance CPU core with a variety of system and I/O resources useful in a broad range of applications. The CPU core consists of five functional blocks: clock generator, bus state controller, Interrupt controller, memory management unit (MMU), and the central processing unit (CPU). The integrated I/O resources make up the remaining four functional blocks: direct memory access (DMA) control (2 channels), asynchronous serial communication interface (ASCI, 2 channels) programmable reload timers (PRT, 2 channels), and a clock serial I/O (CSI/O) channel.

**Clock Generator.** This logic generates a system clock from an external crystal or clock input. The external clock is divided by 2 or 1 and provides the timing for both internal and external devices.

**Bus State Controller.** This logic performs all of the status and bus-control activity associated with the CPU and some on-chip peripherals. Also includes wait-state timing, reset cycles, DRAM refresh, and DMA bus exchanges.

**Interrupt Controller.** This logic monitors and prioritizes the variety of internal and external interrupts and traps to provide the correct responses from the CPU. To maintain compatibility with the Z80 CPU, three different interrupts modes are supported.

**Memory Management Unit.** The MMU allows the user to map the memory used by the CPU (logically only 64KB) into the 1-MB addressing range supported by the Z8S180/Z8L180. The organization of the MMU object code maintains compatibility with the Z80 CPU, while offering access to an extended memory space. Accomplished by using an effective common-area/banked-area scheme.

**Central Processing Unit.** The CPU is microcoded to provide a core that is object-code compatible with the Z80 CPU. It also provides a superset of the Z80 instruction set, including 8-bit multiplication. The core is modified to allow many of the instructions to execute in fewer clock cycles.

**DMA Controller.** The DMA controller provides high-speed transfers between memory and I/O devices. Transfer operations supported are memory-to-memory, memory to/from I/O, and I/O-to-I/O. Transfer modes supported are request, burst, and cycle steal. DMA transfers can access the full 1-MB address range with a block length up to 64 KB, and can cross over 64K boundaries.

**Asynchronous Serial Communication Interface (ASCI).**

The ASCI logic provides two individual full-duplex UARTs. Each channel includes a programmable baud rate generator and modem control signals. The ASCI channels can also support a multiprocessor communication format as well as break detection and generation

**Programmable Reload Timers (PRT).** This logic consists of two separate channels, each containing a 16-bit counter (timer) and count reload register. The time base for the counters is derived from the system clock (divided by 20) before reaching the counter. PRT channel 1 provides an optional output to allow for waveform generation.

## OPERATION MODES (Continued)

**Table 5. RETI Control Signal States**

| Machine Cycle | States | Address | Data | $\overline{RD}$ | $\overline{WR}$ | $\overline{MREQ}$ | $\overline{IORQ}$ | $\overline{M1}$ M1E = 1 | $\overline{M1}$ M1E = 0 | $\overline{HALT}$ | ST |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | T1–T3 | 1st Opcode | EDH | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 2 | T1–T3 | 2nd Opcode | 4DH | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| | Ti | NA | 3-state | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Ti | NA | 3-state | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Ti | NA | 3-state | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 3 | T1–T3 | 1st Opcode | EDH | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| | Ti | NA | 3-state | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 4 | T1–T3 | 2nd Opcode | 4DH | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 5 | T1–T3 | SP | Data | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 6 | T1–T3 | SP + 1 | Data | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |

**$\overline{M1TE}$ ($\overline{M1}$ Temporary Enable).** This bit controls the temporary assertion of the $\overline{M1}$ signal. It is always read back as a 1 and is set to 1 during RESET.

When M1E is set to 0 to accommodate certain external Z80 peripheral(s), those same device(s) may require a pulse on $\overline{M1}$ after programming certain of their registers to complete the function being programmed.

For example, when a control word is written to the Z80 PIO to enable interrupts, no enable actually takes place until the PIO sees an active $\overline{M1}$ signal. When $\overline{M1TE}$ = 1, there is no change in the operation of the $\overline{M1}$ signal, and M1E controls its function. When $\overline{M1TE}$ = 0, the $\overline{M1}$ output is asserted during the next opcode fetch cycle regardless of the state programmed into the M1E bit. This condition is only momentary (one time) and it is not necessary to preprogram a 1 to disable the function (see Figure 10).

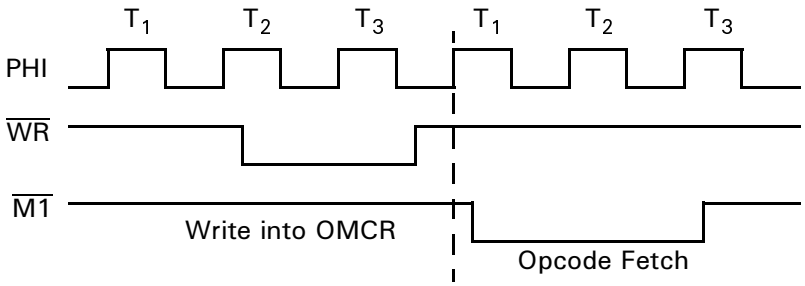


**Figure 10. M1 Temporary Enable Timing**

**IOC (I/O Compatibility).** This bit controls the timing of the $\overline{IORQ}$ and $\overline{RD}$ signals. The bit is set to 1 by RESET.

When $\overline{IOC}$ = 1, the $\overline{IORQ}$ and $\overline{RD}$ signals function the same as the Z64180 (Figure 11).

## OPERATION MODES (Continued)

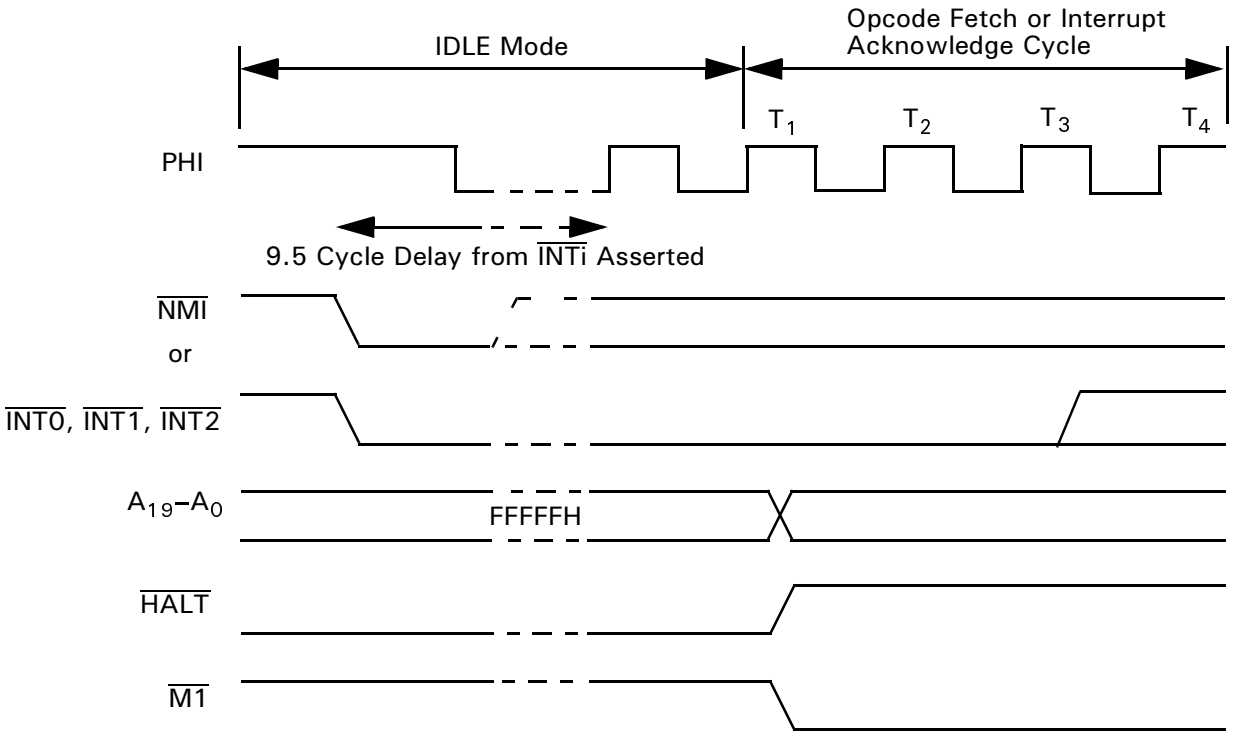


**Figure 15. Z8S180/Z8L180 IDLE Mode Exit Due To External Interrupt**

While the Z8S180/Z8L180 is in IDLE mode, it grants the bus to an external Master if the BREXT bit (CCR5) is 1. Figure 16 depicts the timing for this sequence.

**Note:** A response to a bus request takes 8 clock cycles longer than in normal operation.

After the external Master negates the Bus Request, the Z8S180/Z8L180 disables the PHI clock and remains in IDLE mode.

ing the bus to an external Master during STANDBY mode, when the BREXT bit in the CPU Control Register (CCR5) is 1.

As described previously for SLEEP and IDLE modes, when the MPU leaves STANDBY mode due to $\overline{NMI}$ Low or an enabled $\overline{INT0}$–$\overline{INT2}$ Low when the IEF, flag is 1 due to an IE instruction, it starts by performing the interrupt with the return address being that of the instruction following the SLP instruction. If the Z8S180/Z8L180 leaves STANDBY mode due to an external interrupt request that's enabled in the INT/TRAP Control Register, but the IEF, bit is 0 due to a DI instruction, the processor restarts by executing the instruction(s) following the SLP instruction. If $\overline{INT0}$, or $\overline{INT1}$ or $\overline{INT2}$ goes inactive before the end of the clock stabilization delay, the Z8S180/Z8L180 stays in STANDBY mode.

Figure 17 indicates the timing for leaving STANDBY mode due to an interrupt request.

**Note:** The Z8S180/Z8L180 takes either 64 or $2^{17}$ (131,072) clocks to restart, depending on the CCR3 bit.

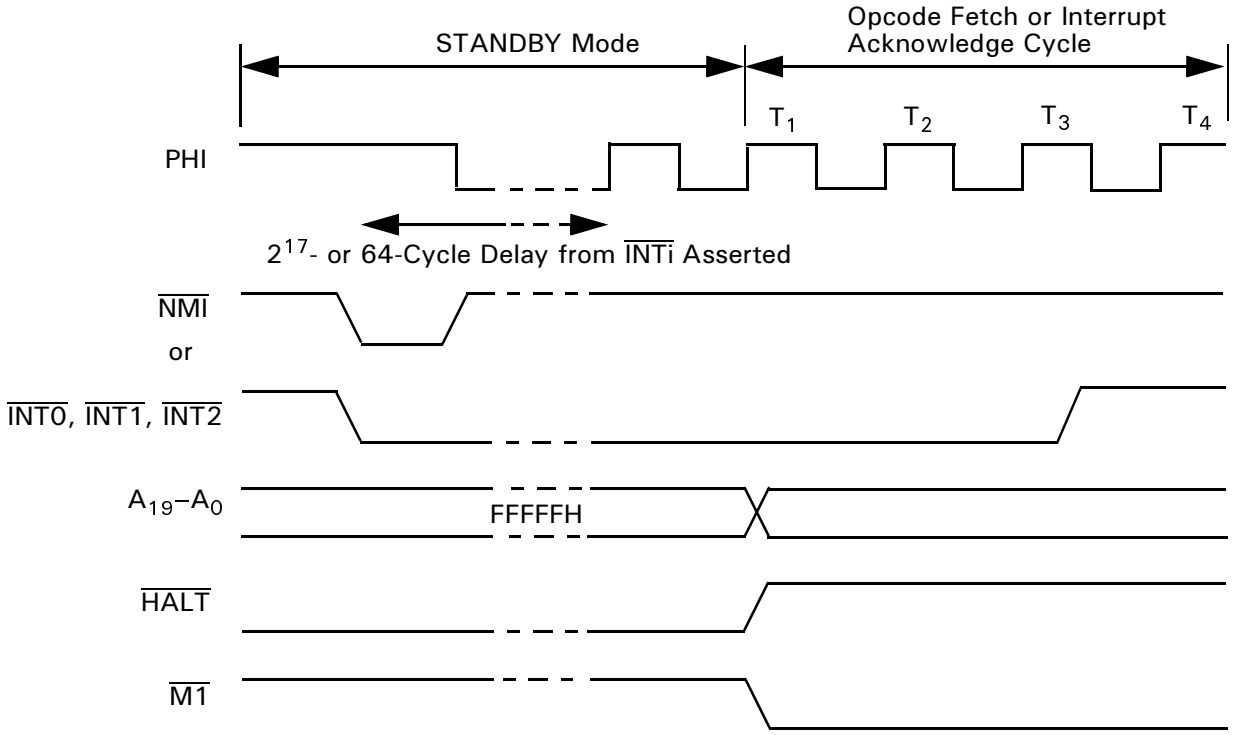


**Figure 17. Z8S180/Z8L180 STANDBY Mode Exit Due to External Interrupt**

While the Z8S180/Z8L180 is in STANDBY mode, it grants the bus to an external Master if the BREXT bit (CCR5) is 1. Figure 18 indicates the timing of this sequence. The device takes 64 or $2^{17}$ (131,072) clock cycles to grant the bus depending on the CCR3 bit. The latter (not the QUICK RECOVERY) case may be prohibitive for many demand-driven external Masters. If so, QUICK RECOVERY or IDLE mode can be used.

## STANDARD TEST CONDITIONS

The following standard test conditions apply to DC Characteristics, unless otherwise noted. All voltages are referenced to $V_{SS}$ (0V). Positive current flows into the referenced pin.

All AC parameters assume a load capacitance of 100 pF. Add a 10-ns delay for each 50-pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to $V_{OL}$ MAX or $V_{OL}$ MIN as indicated in Figures 20 through 30 (except for CLOCK, which is referenced to the 10% and 90% points). Ordering Information lists temperature ranges and product numbers. Find package drawings in Package Information.

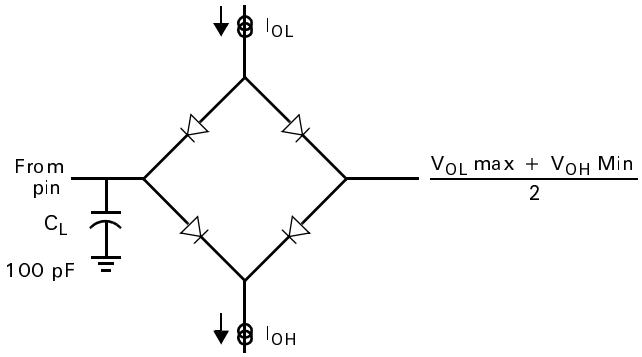


**Figure 19. AC Parameter Test Circuit**

## ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | –0.3 ~ +7.0 | V |
| Input Voltage | $V_{IN}$ | –0.3 ~ $V_{cc}$ +0.3 | V |
| Operating Temperature | $T_{OPR}$ | 0 ~ 70 | °C |
| Extended Temperature | $T_{EXT}$ | –40 ~ 85 | °C |
| Storage Temperature | $T_{STG}$ | –55 ~ +150 | °C |

**Note:** Permanent damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability.

## AC CHARACTERISTICS—Z8S180

**Table 8. Z8S180 AC Characteristics**
**$V_{DD}$ = 5V ±10% or $V_{DD}$ = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation**

| | | | Z8S180—20 MHz | | Z8S180—33 MHz | | |
|---|---|---|---|---|---|---|---|
| **Number** | **Symbol** | **Item** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| 1 | $t_{CYC}$ | Clock Cycle Time | 50 | DC | 30 | DC | ns |
| 2 | $t_{CHW}$ | Clock "H" Pulse Width | 15 | — | 10 | — | ns |
| 3 | $t_{CLW}$ | Clock "L" Pulse Width | 15 | — | 10 | — | ns |
| 4 | $t_{CF}$ | Clock Fall Time | — | 10 | — | 5 | ns |
| 5 | $t_{CR}$ | Clock Rise Time | — | 10 | — | 5 | ns |
| 6 | $t_{AD}$ | PHI Rise to Address Valid Delay | — | 30 | — | 15 | ns |
| 7 | $t_{AS}$ | Address Valid to $\overline{MREQ}$ Fall or $\overline{IORQ}$ Fall) | 5 | — | 5 | — | ns |
| 8 | $t_{MED1}$ | PHI Fall to $\overline{MREQ}$ Fall Delay | — | 25 | — | 15 | ns |
| 9 | $t_{RDD1}$ | PHI Fall to $\overline{RD}$ Fall Delay $\overline{IOC}$ = 1 | — | 25 | — | 15 | ns |
| | | PHI Rise to $\overline{RD}$ Rise Delay $\overline{IOC}$ = 0 | — | 25 | — | 15 | |
| 10 | $t_{M1D1}$ | PHI Rise to $\overline{M1}$ Fall Delay | — | 35 | — | 15 | ns |
| 11 | $t_{AH}$ | Address Hold Time from $\overline{MREQ}$, $\overline{IOREQ}$, $\overline{RD}$, $\overline{WR}$ High | 5 | — | 5 | — | ns |
| 12 | $t_{MED2}$ | PHI Fall to $\overline{MREQ}$ Rise Delay | — | 25 | — | 15 | ns |
| 13 | $t_{RDD2}$ | PHI Fall to $\overline{RD}$ Rise Delay | — | 25 | — | 15 | ns |
| 14 | $t_{M1D2}$ | PHI Rise to $\overline{M1}$ Rise Delay | — | 40 | — | 15 | ns |
| 15 | $t_{DRS}$ | Data Read Set-up Time | 10 | — | 5 | — | ns |
| 16 | $t_{DRH}$ | Data Read Hold Time | 0 | — | 0 | — | ns |
| 17 | $t_{STD1}$ | PHI Fall to ST Fall Delay | — | 30 | — | 15 | ns |
| 18 | $t_{STD2}$ | PHI Fall to ST Rise Delay | — | 30 | — | 15 | ns |
| 19 | $t_{WS}$ | $\overline{WAIT}$ Set-up Time to PHI Fall | 15 | — | 10 | — | ns |
| 20 | $t_{WH}$ | $\overline{WAIT}$ Hold Time from PHI Fall | 10 | — | 5 | — | ns |
| 21 | $t_{WDZ}$ | PHI Rise to Data Float Delay | — | 35 | — | 20 | ns |
| 22 | $t_{WRD1}$ | PHI Rise to $\overline{WR}$ Fall Delay | — | 25 | — | 15 | ns |
| 23 | $t_{WDD}$ | PHI Fall to Write Data Delay Time | — | 25 | — | 15 | ns |
| 24 | $t_{WDS}$ | Write Data Set-up Time to $\overline{WR}$ Fall | 10 | — | 10 | — | ns |
| 25 | $t_{WRD2}$ | PHI Fall to $\overline{WR}$ Rise Delay | — | 25 | — | 15 | ns |
| 26 | $t_{WRP}$ | $\overline{WR}$ Pulse Width (Memory Write Cycle) | 80 | — | 45 | — | ns |
| 26a | | $\overline{WR}$ Pulse Width (I/O Write Cycle) | 150 | — | 70 | — | ns |
| 27 | $t_{WDH}$ | Write Data Hold Time from $\overline{WR}$ Rise | 10 | — | 5 | — | ns |
| 28 | $t_{IOD1}$ | PHI Fall to $\overline{IORQ}$ Fall Delay $\overline{IOC}$ = 1 | — | 25 | — | 15 | ns |
| | | PHI Rise to $\overline{IORQ}$ Fall Delay $\overline{IOC}$ = 0 | — | 25 | — | 15 | |
| 29 | $t_{IOD2}$ | PHI Fall to $\overline{IORQ}$ Rise Delay | — | 25 | — | 15 | ns |
| 30 | $t_{IOD3}$ | $\overline{M1}$ Fall to $\overline{IORQ}$ Fall Delay | 125 | — | 80 | — | ns |
| 31 | $t_{INTS}$ | $\overline{INT}$ Set-up Time to PHI Fall | 20 | — | 15 | — | ns |

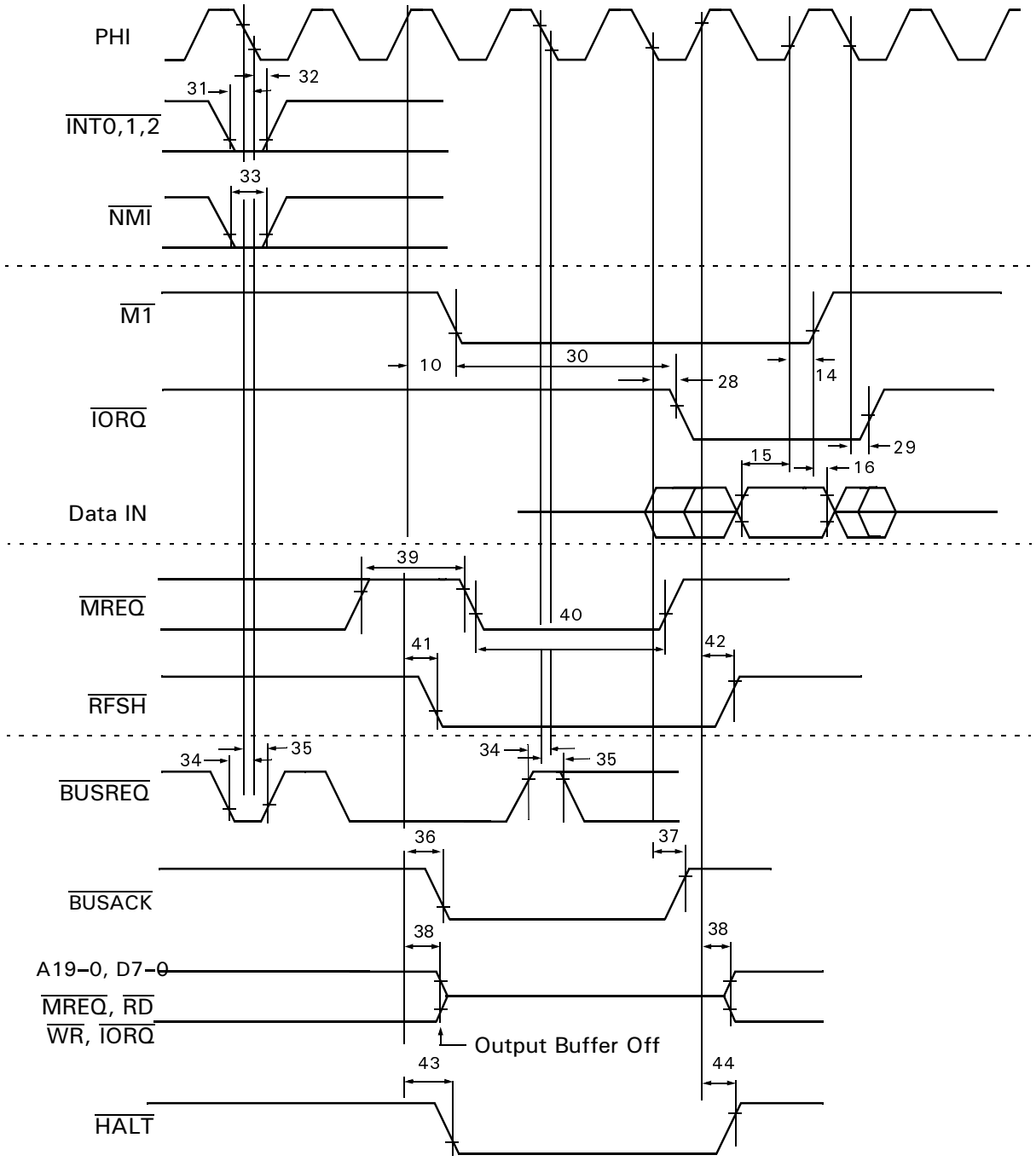


**Figure 21. CPU Timing**
**(INT0 Acknowledge Cycle, Refresh Cycle, BUS RELEASE Mode, HALT Mode, SLEEP Mode, SYSTEM STOP Mode)**

## ASCI CHANNEL CONTROL REGISTER B

ASCI Control Register B 0 (CNTLB0: I/O Address = 02H)
ASCI Control Register B 1 (CNTLB1: I/O Address = 03H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | MPBT | MP | $\overline{CTS}$/PS | PEO | DR | SS2 | SS1 | SS0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Figure 34. ASCI Channel Control Register B**

**MPBT: Multiprocessor Bit Transmit (Bit 7).** When multiprocessor communication format is selected (MP bit = 1), MPBT is used to specify the MPB data bit for transmission. If MPBT = 1, then MPB = 1 is transmitted. If MPBT = 0, then MPB = 0 is transmitted. The MPBT state is undefined during and after RESET.

**MP: Multiprocessor Mode (Bit 6).** When MP is set to 1, the data format is configured for multiprocessor mode based on MOD2 (number of data bits) and MOD0 (number of stop bits) in CNTLA. The format is as follows:

Start bit + 7 or 8 data bits + MPB bit + 1 or 2 stop bits

Multiprocessor (MP = 1) format offers no provision for parity. If MP = 0, the data format is based on MOD0, MOD1, MOD2, and may include parity. The MP bit is cleared to 0 during RESET.

**$\overline{CTS}$/PS: Clear to Send/Prescale (Bit 5).** When read, $\overline{CTS}$/PS reflects the state of the external $\overline{CTS}$ input. If the $\overline{CTS}$ input pin is High, $\overline{CTS}$/PS is read as 1.

**Note:** When the $\overline{CTS}$ input pin is High, the TDRE bit is inhibited (that is, held at 0).

For channel 1, the $\overline{CTS}$ input is multiplexed with RXS pin (Clocked Serial Receive Data). Thus, $\overline{CTS}$/PS is only valid when read if the channel 1 CTS1E bit = 1 and the $\overline{CTS}$ input pin function is selected. The READ data of $\overline{CTS}$/PS is not affected by $\overline{RESET}$.

If the SS2–0 bits in this register are not 111, and the BRG mode bit in the ASEXT register is 0, then writing to this bit sets the prescale (PS) control. Under those circumstances, a 0 indicates a divide-by-10 prescale function while a 1 indicates divide-by-30. The bit resets to 0.

**PEO: Parity Even Odd (Bit 4) .** PEO selects oven or odd parity. PEO does not affect the enabling/disabling of parity (MOD1 bit of CNTLA). If PEO is cleared to 0, even parity is selected. If PEO is set to 1, odd parity is selected. PEO is cleared to 0 during RESET.

**DR: Divide Ratio (Bit 3).** If the X1 bit in the ASEXT register is 0, this bit specifies the divider used to obtain baud rate from the data sampling clock. If DR is reset to 0, divide-by-16 is used, while if DR is set to 1, divide-by-64 is used. DR is cleared to 0 during RESET.

**SS2,1,0: Source/Speed Select 2,1,0 (Bits 2–0).** First, if these bits are 111, as they are after a RESET, the CKA pin is used as a clock input, and is divided by 1, 16, or 64 depending on the DR bit and the X1 bit in the ASEXT register.

If these bits are not 111 and the BRG mode bit is ASEXT is 0, then these bits specify a power-of-two divider for the PHI clock as indicated in Table 10.

Setting or leaving these bits as 111 makes sense for a channel only when its CKA pin is selected for the CKA function. CKAO/CKS offers the CKAO function when bit 4 of the System Configuration Register is 0. $\overline{DCD0}$/CKA1 offers the CKA1 function when bit 0 of the Interrupt Edge register is 1.

**Table 10. Divide Ratio**

| SS2 | SS1 | SS0 | Divide Ratio |
|---|---|---|---|
| 0 | 0 | 0 | ÷1 |
| 0 | 0 | 1 | ÷2 |
| 0 | 1 | 0 | ÷4 |
| 0 | 1 | 1 | ÷8 |
| 1 | 0 | 0 | ÷16 |
| 1 | 0 | 1 | ÷32 |
| 1 | 1 | 0 | ÷64 |
| 1 | 1 | 1 | External Clock |

ASCI0 requests an interrupt when $\overline{DCD0}$ goes High. RIE is cleared to 0 by RESET.

**$\overline{DCD0}$: Data Carrier Detect (Bit 2 STAT0).** This bit is set to 1 when the pin is High. It is cleared to 0 on the first READ of STAT0 following the pin's transition from High to Low and during RESET. When bit 6 of the ASEXT0 register is 0 to select auto-enabling, and the pin is negated (High), the receiver is reset and its operation is inhibited.

**$\overline{CTS1E}$: Clear To Send (Bit 2 STAT1).** Channel 1 features an external $\overline{CTS1}$ input, which is multiplexed with the receive data pin RSX for the CSI/O. Setting this bit to 1 selects the CTS1 function; clearing the bit to 0 selects the RXS function.

**TDRE: Transmit Data Register Empty (Bit 1).** TDRE = 1 indicates that the TDR is empty and the next transmit data byte is written to TDR. After the byte is written to TDR, TDRE is cleared to 0 until the ASCI transfers the byte from TDR to the TSR and then TDRE is again set to 1. TDRE is set to 1 in IOSTOP mode and during RESET. On ASCI0, if the $\overline{CTS0}$ pin is auto-enabled in the ASEXT0 register and the pin is High, TDRE is reset to 0.

**TIE: Transmit Interrupt Enable (Bit 0).** TIE should be set to 1 to enable ASCI transmit interrupt requests. If TIE = 1, an interrupt is requested when TDRE = 1. TIE is cleared to 0 during RESET.

## ASCI TRANSMIT DATA REGISTERS

Register addresses 06H and 07H hold the ASCI transmit data for channel 0 and channel 1, respectively.

### ASCI Transmit Data Registers Channel 0

**Mnemonic TDR0**
**Address 06H**

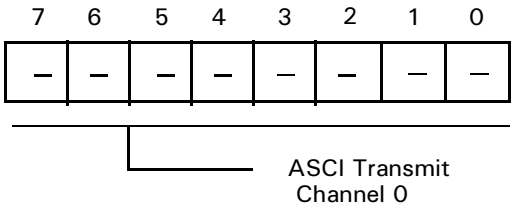


**Figure 36. ASCI Register**

### ASCI Transmit Data Registers Channel 1

**Mnemonic TDR1**
**Address 07H**

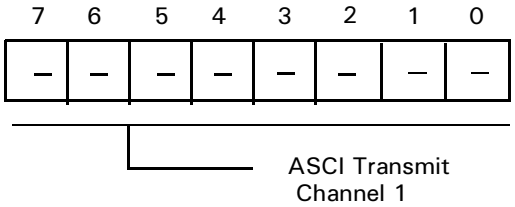


**Figure 37. ASCI Register**

## ASCI RECEIVE REGISTER

Register addresses 08H and 09H hold the ASCI receive data for channel 0 and channel 1, respectively.

### ASCI Receive Register Channel 0

**Mnemonic RDR0**
**Address 08H**

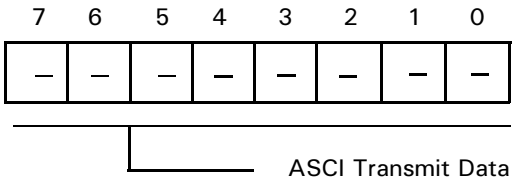


**Figure 38. ASCI Receive Register Channel 0**

### ASCI Receive Register Channel 1

**Mnemonic RDR1**
**Address 09H**

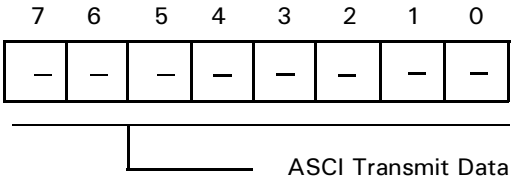


**Figure 39. ASCI Receive Register Channel 1**

## CSI/O CONTROL/STATUS REGISTER

The CSI/O Control/Status Register (CNTR) is used to monitor CSI/O status, enable and disable the CSI/O, enable and disable interrupt generation, and select the data clock speed and source.

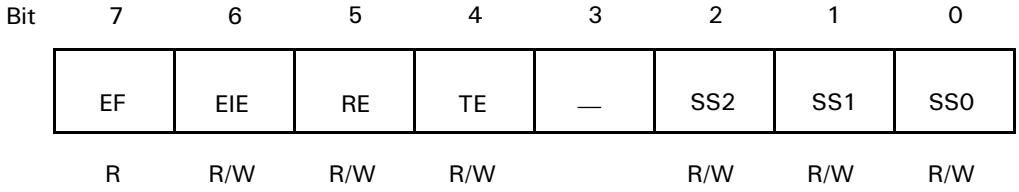


**Figure 40. CSI/O Control Register (CNTR: I/O Address = 000AH)**

**EF: End Flag (Bit 7).** EF is set to 1 by the CSI/O to indicate completion of an 8-bit data transmit or receive operation. If End Interrupt Enable (EIE) bit = 1 when EF is set to 1, a CPU interrupt request is generated. Program access of TRDR only occurs if EF = 1. The CSI/O clears EF to 0 when TRDR is read or written. EF is cleared to 0 during RESET and IOSTOP mode.

**EIE: End Interrupt Enable (Bit 6).** EIE is set to 1 to generate a CPU interrupt request. The interrupt request is inhibited if EIE is reset to 0. EIE is cleared to 0 during RESET.

**RE: Receive Enable (Bit 5).** A CSI/O receive operation is started by setting RE to 1. When RE is set to 1, the data clock is enabled. In internal clock mode, the data clock is output from the CKS pin. In external clock mode, the clock is input on the CKS pin. In either case, data is shifted in on the RXS pin in synchronization with the (internal or external) data clock. After receiving 8 bits of data, the CSI/O automatically clears RE to 0, EF is set to 1, and an interrupt (if enabled by EIE = 1) is generated. RE and TE are never both set to 1 at the same time. RE is cleared to 0 during RESET and IOSTOP mode.

**TE: Transmit Enable (Bit 4).** A CSI/O transmit operation is started by setting TE to 1. When TE is set to 1, the data clock is enabled. When in internal clock mode, the data clock is output from the CKS pin. In external clock mode, the clock is input on the CKS pin. In either case, data is shifted out on the TXS pin synchronous with the (internal or external) data clock. After transmitting 8 bits of data, the CSI/O automatically clears TE to 0, sets EF to 1, and requests an interrupt if enabled by EIE = 1. TE and RE are

## TIMER CONTROL REGISTER

The Timer Control Register (TCR) monitors both channels (PRT0, PRT1) TMDR status. It also controls the enabling and disabling of down-counting and interrupts, and controls the output pin A18/$T_{OUT}$ for PRT1.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | TIF1 | TIF0 | TIE1 | TIE0 | TOC1 | TOC0 | TDE1 | TDE0 |
| | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

**Figure 46. Timer Control Register (TCR: I/O Address = 10H)**

**TIF1: Timer Interrupt Flag 1 (Bit 7) .** When TMDR1 decrements to 0, TIF1 is set to 1. This condition generates an interrupt request if enabled by TIE1 = 1. TIF1 is reset to 0 when TCR is read and the higher or lower byte of TMDR1 is read. During RESET, TIF1 is cleared to 0.

**TIF0: Timer Interrupt Flag 0 (Bit 6).** When TMDR0 decrements to 0, TIF0 is set to 1. This condition generates an interrupt request if enabled by TIE0 = 1. TIF0 is reset to 0 when TCR is read and the higher or lower byte of TMDR0 is read. During RESET, TIF0 is cleared to 0.

**TIE1: Timer Interrupt Enable 1 (Bit 5).** When TIE0 is set to 1, TIF1 = 1 generates a CPU interrupt request. When TIE0 is reset to 0, the interrupt request is inhibited. During RESET, TIE0 is cleared to 0.

**TOC1, 0: Timer Output Control (Bits 3, 2).** TOC1 and TOC0 control the output of PRT1 using the multiplexed A18/$T_{OUT}$ pin as indicated in Table 12. During RESET, TOC1 and TOC0 are cleared to 0. If bit 3 of the IAR1B register is 1, the $T_{OUT}$ function is selected. By programming TOC1 and TOC0, the A18/$T_{OUT}$ pin can be forced High, Low, or toggled when TMDR1 decrements to 0.

**Table 12. Timer Output Control**

| TOC1 | TOC0 | Output | |
|---|---|---|---|
| 0 | 0 | Inhibited | The A18/$T_{OUT}$ pin is not affected by the PRT |
| 0 | 1 | Toggled | If bit 3 of IAR1B is 1, the A18/$T_{OUT}$ pin is toggled or set Low or High as indicated |
| 1 | 0 | 0 | |
| 1 | 1 | 1 | |

**TDE1, 0: Timer Down Count Enable (Bits 1, 0).** TDE1 and TDE0 enable and disable down-counting for TMDR1 and TMDR0, respectively. When TDEn (n = 0,1) is set to 1, down-counting is stopped and TMDRn is freely read or written. TDE1 and TDE0 are cleared to 0 during RESET and TMDRn does not decrement until TDEn is set to 1.

## CLOCK MULTIPLIER REGISTER

**(Z180 MPU Address 1EH)**

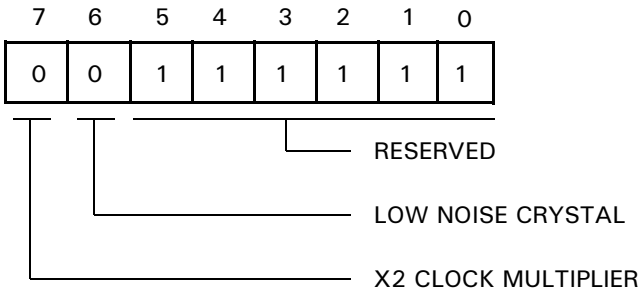


**Figure 54. Clock Multiplier Register**

**Bit 7. X2 Clock Multiplier Mode.** When this bit is set to 1, the programmer can double the internal clock speed from the speed of the external clock. This feature only operates effectively with frequencies of 10–16 MHz (20–32 MHz internal). When this bit is set to 0, the Z8S180/Z8L180 device operates in normal mode. At power-up, this feature is disabled.

**Bit 6. Low Noise Crystal Option.** Setting this bit to 1 enables the low-noise option for the EXTAL and XTAL pins. This option reduces the gain in addition to reducing the output drive capability to 30% of its original drive capability. The Low Noise Crystal Option is recommended in the use of crystals for PCMCIA applications, where the crystal may be driven too hard by the oscillator. Setting this bit to 0 is selected for normal operation of the EXTAL and XTAL pins. The default for this bit is 0.

**Note:** Operating restrictions for device operation are listed below. If a low-noise option is required, and normal device operation is required, use the clock multiplier feature.

**Table 13. Low Noise Option**

| Low Noise ADDR 1E, bit 6 = 1 | Normal ADDR 1E, bit 6 = 0 |
|---|---|
| 20 MHz @ 4.5V, 100°C | 33 MHz @ 4.5V, 100°C |
| 10 MHz @ 3.0V, 100°C | 20 MHz @ 3.0V, 100°C |

## DMA MODE REGISTER

The DMA Mode Register (DMODE) is used to set the addressing and transfer mode for channel 0.

### DMA Mode Register

**Mnemonic DMODE**
**Address 31H**

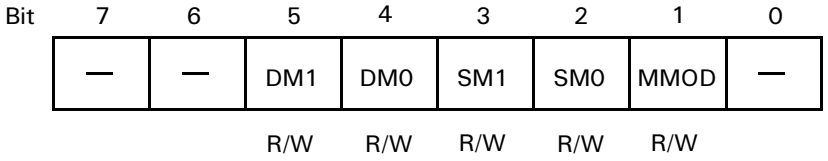


**Figure 72. DMA Mode Register (DMODE: I/O Address = 31H)**

**DM1, DM0: Destination Mode Channel 0 (Bits 5,4).** This mode specifies whether the destination for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred. DM1 and DM0 are cleared to 0 during RESET.

**Table 14. Channel 0 Destination**

| DM1 | DM0 | Memory I/O | Memory Increment/Decrement |
|---|---|---|---|
| 0 | 0 | Memory | +1 |
| 0 | 1 | Memory | –1 |
| 1 | 0 | Memory | fixed |
| 1 | 1 | I/O | fixed |

**SM1, SM0: Source Mode Channel 0 (Bits 3, 2) .** This mode specifies whether the source for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred.

**Table 15. Channel 0 Source**

| SM1 | SM0 | Memory I/O | Memory Increment/Decrement |
|---|---|---|---|
| 0 | 0 | Memory | +1 |
| 0 | 1 | Memory | –1 |
| 1 | 0 | Memory | fixed |
| 1 | 1 | I/O | fixed |

## DMA/WAIT CONTROL REGISTER

The DMA/WAIT Control Register (DCNTL) controls the insertion of wait states into DMAC (and CPU) accesses of memory or I/O. Also, the register defines the Request signal for each channel as level or edge sense. DCNTL also sets the DMA transfer mode for channel 1, which is limited to memory to/from I/O transfers.

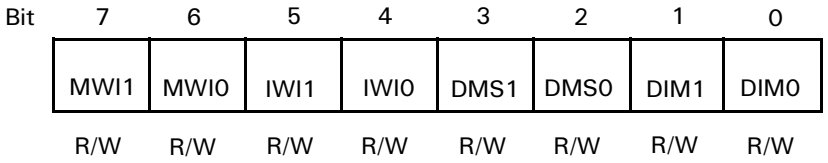


**Figure 73. DMA/WAIT Control Register (DCNTL: I/O Address = 32H)**

**MWI1, MWI0: Memory Wait Insertion (Bits 7–6).** This bit specifies the number of wait states introduced into CPU or DMAC memory access cycles. MWI1 and MWI0 are set to 1 during RESET.

| MWI1 | MWI0 | Wait State |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 |

**IWI1, IWI0: I/O Wait Insertion (Bits 5–4).** This bit specifies the number of wait states introduced into CPU or DMAC I/O access cycles. IWI1 and IWI0 are set to 1 during RESET.

| IWI1 | IWI0 | Wait State |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |

**Note:** These wait states are added to the 3-clock I/O cycle that is used to access the on-chip I/O registers. It is equally valid to regard these as 0 to 3 wait states added to a 4-clock external I/O cycle.

**DMS1, DMS0: DMA Request Sense (Bits 3–2).** DMS1 and DMS0 specify the DMA request sense for channel 0 and channel 1 respectively. When reset to 0, the input is level sense. When set to 1, the input is edge sense. DMS1 and DMS0 are cleared to 0 during RESET.

| DMSi | Sense |
|---|---|
| 1 | Edge Sense |
| 0 | Level Sense |

Typically, for an input/source device, the associated DMS bit should be programmed as 0 for level sense. The device takes a relatively long time to update its Request signal after the DMA channel reads data (in the first of the two machine cycles involved in transferring a byte).

An output/destination device takes much less time to update its Request signal after the DMA channel starts a WRITE operation to it (the second machine cycle of the two cycles involved in transferring a byte). With zero-wait state I/O cycles, a device cannot update its request signal in the required time, so edge sensing must be used.

A one-wait-state I/O cycle also does not provide sufficient time for updating, so edge sensing is again required.

**DIM1, DIM0: DMA Channel 1 I/O and Memory Mode (Bits 1–0).** Specifies the source/destination and address modifier for channel 1 memory to/from I/O transfer modes. DIM1 and DIM0 are cleared to 0 during RESET.

**Table 17. Channel 1 Transfer Mode**

| DIM1 | DMI0 | Transfer Mode | Address Increment/Decrement |
|---|---|---|---|
| 0 | 0 | Memory→I/O | MAR1 +1, IAR1 fixed |
| 0 | 1 | Memory→I/O | MAR1 –1, IAR1 fixed |
| 1 | 0 | I/O→Memory | IAR1 fixed, MAR1 +1 |
| 1 | 1 | I/O→Memory | IAR1 fixed, MAR1 –1 |

All TRAPs occur after fetching an undefined second opcode byte following one of the prefix opcodes (CBH, DDH, EDH, or FDH) or after fetching an undefined third opcode byte following one of the double-prefix opcodes (DDCBH or FDCBH).

The state of the Undefined Fetch Object (UFO) bit in ITC allows TRAP software to correctly *adjust* the stacked PC, depending on whether the second or third byte of the opcode generated the TRAP. If UFO = 0, the starting address of the invalid instruction is the stacked PC–1. If UFO = 1, the starting address of the invalid instruction is equal to the stacked PC–2.

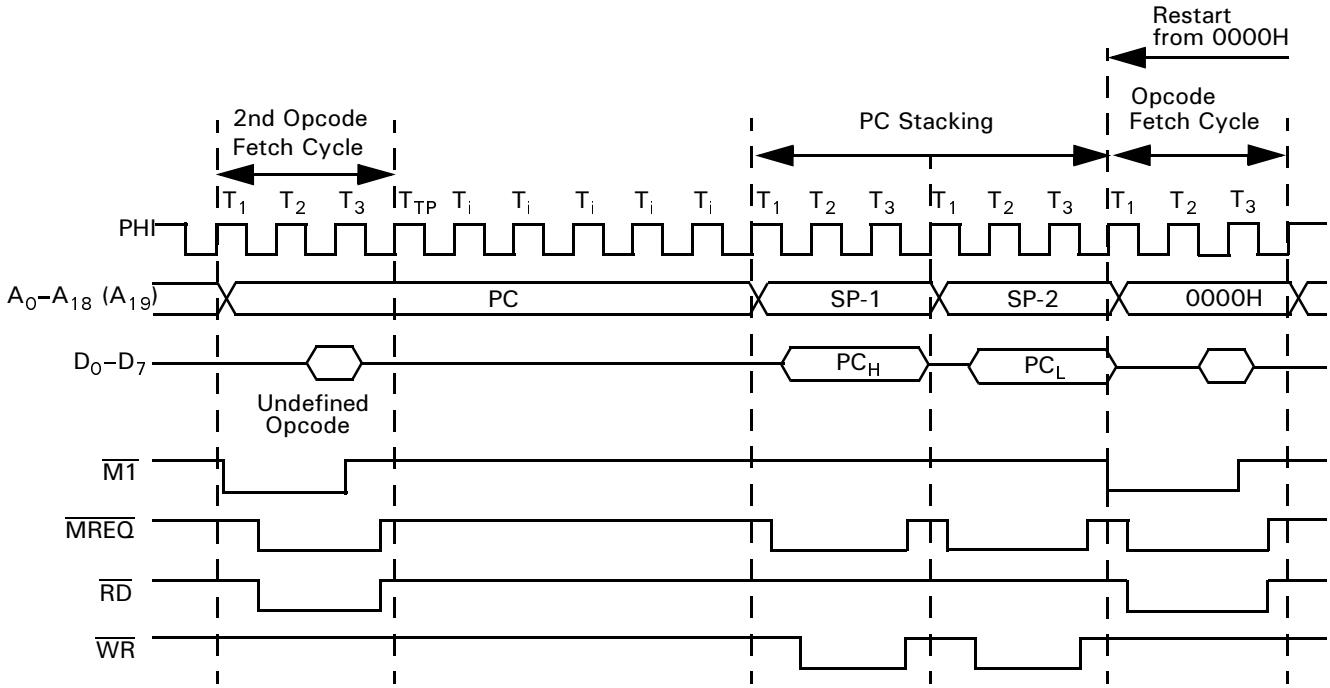


**Figure 75. TRAP Timing—2nd Opcode Undefined**

## REFRESH CONTROL REGISTER

**Mnemonic RCR**
**Address 36H**

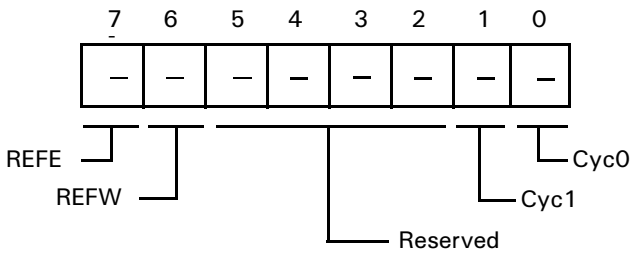


**Figure 77. Refresh Control Register (RCR: I/O Address = 36H)**

The Refresh Control Register (RCR) specifies the interval and length of refresh cycles, while enabling or disabling the refresh function.

**REFE: Refresh Enable (Bit 7).** REFE = 0 disables the refresh controller, while REFE = 1 enables refresh cycle insertion. REFE is set to 1 during RESET.

**REFW: Refresh Wait (Bit 6).** REFW = 0 causes the refresh cycle to be two clocks in duration. REFW = 1 causes the refresh cycle to be three clocks in duration by adding a refresh wait cycle (TRW). REFW is set to 1 during RESET.

**CYC1, 0: Cycle Interval (Bit 1,0).** CYC1 and CYC0 specify the interval (in clock cycles) between refresh cycles. When dynamic RAM requires 128 refresh cycles every 2 ms (or 256 cycles in every 4 ms), the required refresh interval is less than or equal to 15.625 µs. Thus, the underlined values indicate the best refresh interval depending on CPU clock frequency. CYC0 and CYC1 are cleared to 0 during RESET (see Table 18).

**Table 18. DRAM Refresh Intervals**

| | | | Time Interval | | | | |
|---|---|---|---|---|---|---|---|
| **CYC1** | **CYC0** | **Insertion Interval** | **PHI: 10 MHz** | **8 MHz** | **6 MHz** | **4 MHz** | **2.5 MHz** |
| 0 | 0 | 10 states | (1.0 µs)* | (1.25 µs)* | 1.66 µs | 2.5 µs | 4.0 µs |
| 0 | 1 | 20 states | (2.0 µs)* | (2.5 µs)* | 3.3 µs | 5.0 µs | 8.0 µs |
| 1 | 0 | 40 states | (4.0 µs)* | (5.0 µs)* | 6.6 µs | 10.0 µs | 16.0 µs |
| 1 | 1 | 80 states | (8.0 µs)* | (10.0 µs)* | 13.3 µs | 20.0 µs | 32.0 µs |

**Note:** *calculated interval.

**Refresh Control and Reset.** After RESET, based on the initialized value of RCR, refresh cycles occur with an interval of 10 clock cycles and be 3 clock cycles in duration.

### Dynamic RAM Refresh Operation

1. Refresh Cycle insertion is stopped when the CPU is in the following states:
   a. During RESET
   b. When the bus is released in response to $\overline{\text{BUSREQ}}$
   c. During SLEEP mode
   d. During $\overline{\text{WAIT}}$ states
2. Refresh cycles are suppressed when the bus is released in response to $\overline{\text{BUSREQ}}$. However, the refresh timer continues to operate. The time at which the first refresh cycle occurs after the Z8S180/Z8L180 reacquires the bus depends on the refresh timer. This cycle offers no timing relationship with the bus exchange.
3. Refresh cycles are suppressed during SLEEP mode. If a refresh cycle is requested during SLEEP mode, the refresh cycle request is internally latched (until replaced with the next refresh request). The latched refresh cycle is inserted at the end of the first machine cycle after SLEEP mode is exited. After this initial cycle, the time at which the next refresh cycle occurs depends on the refresh time and offers no relationship with the exit from SLEEP mode.
4. The refresh address is incremented by one for each successful refresh cycle, not for each refresh. Thus, independent of the number of missed refresh requests, each refresh bus cycle uses a refresh address incremented by one from that of the previous refresh bus cycles.

## I/O CONTROL REGISTER

The I/O Control Register (ICR) allows relocation of the internal I/O addresses. ICR also controls the enabling and disabling of IOSTOP mode (Figure 83).

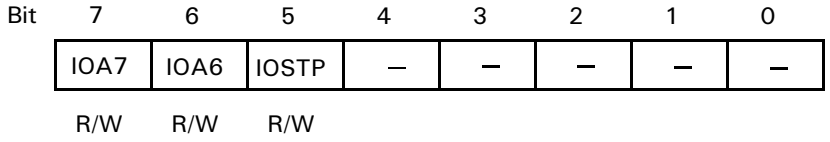


**Figure 83. I/O Control Register (ICR: I/O Address = 3FH)**

**IOA7, 6: I/O Address Relocation (Bits 7,6).** IOA7 and IOA6 relocate internal I/O as indicated in Figure 84.

**Note:** The high-order 8 bits of 16-bit internal I/O address are always 0. IOA7 and IOA6 are cleared to 0 during RESET.

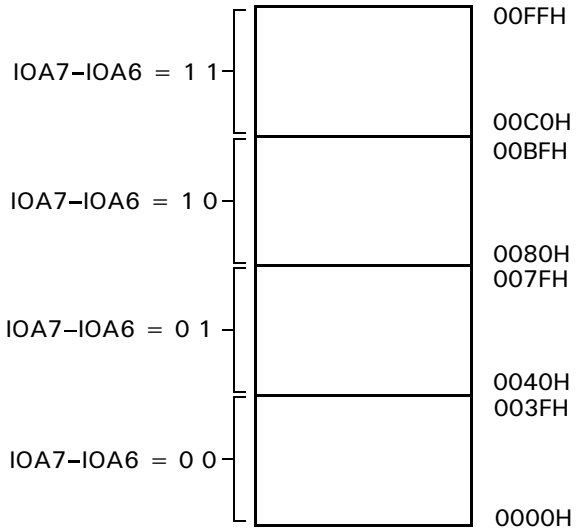


**Figure 84. I/O Address Relocation**

**IOSTP: IOSTOP Mode (Bit 5).** IOSTOP mode is enabled when IOSTP is set to 1. Normal I/O operation resumes when IOSTP is reprogrammed or RESET to 0.