Zilog - Z8S18020FEG1960 Datasheet

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Understanding Embedded - Microprocessors

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	20MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	80-BQFP
Supplier Device Package	80-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8s18020feg1960

Table 1. Z8S180/Z8L180 Pin Identification (Continued)

Pin Number and Package Type			Default	Secondary	
QFP	PLCC	DIP	Function	Function	Control
53	52		TEST		
54	53	49	RXA1		
55	54	50	CKA1	$\overline{\text{TEND0}}$	Bit 4 of CNTLA1
56	55	51	TXS		
57	56	52	RXS	$\overline{\text{CTS1}}$	Bit 2 of STAT1
58	57	53	CKS		
59	58	54	$\overline{\text{DREQ1}}$		
60	59	55	$\overline{\text{TEND1}}$		
61	60	56	$\overline{\text{HALT}}$		
62			NC		
63			NC		
64	61	57	$\overline{\text{RFSH}}$		
65	62	58	$\overline{\text{IORQ}}$		
66	63	59	$\overline{\text{MREQ}}$		
67	64	60	E		
68	65	61	$\overline{\text{M1}}$		
69	66	62	$\overline{\text{WR}}$		
70	67	63	$\overline{\text{RD}}$		
71	68	64	PHI		
72	1	1	V_{SS}		
73	2		V_{SS}		
74	3	2	XTAL		
75			NC		
76	4	3	EXTAL		
77	5	4	$\overline{\text{WAIT}}$		
78	6	5	$\overline{\text{BUSACK}}$		
79	7	6	$\overline{\text{BUSREQ}}$		
80	8	7	$\overline{\text{RESET}}$		

PIN IDENTIFICATION (Continued)

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
76	4	3	EXTAL		IN	IN	IN
77	5	4	$\overline{\text{WAIT}}$		IN	IN	IN
78	6	5	$\overline{\text{BUSACK}}$		High	OUT	OUT
79	7	6	$\overline{\text{BUSREQ}}$		IN	IN	IN
80	8	7	$\overline{\text{RESET}}$		IN	IN	IN

PIN DESCRIPTIONS (Continued)

ways recognized at the end of an instruction, regardless of the state of the interrupt-enable flip-flops. This signal forces CPU execution to continue at location 0066H.

PHI. System Clock (Output). The output is used as a reference clock for the MPU and the external system. The frequency of this output may be one-half, equal to, or twice the crystal or input clock frequency.

$\overline{RD}$. Read (Output, active Low, 3-state). $\overline{RD}$ indicates that the CPU wants to read data from either memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus.

$\overline{RFSH}$. Refresh (Output, active Low). Together with $\overline{MREQ}$, $\overline{RFSH}$ indicates that the current CPU machine cycle and the contents of the address bus should be used for refresh of dynamic memories. The low-order 8 bits of the address bus (A7–A0) contain the refresh address. *This signal is analogous to the $\overline{REF}$ signal of the Z64180.*

$\overline{RTS0}$. Request to Send 0 (Output, active Low); a programmable MODEM control signal for ASCI channel 0.

RXA0, RXA1. Receive Data 0 and 1 (Input). These signals are the receive data for the ASCI channels.

RXS. Clocked Serial Receive Data (Input). This line is the receive data for the CSI/O channel. RXS is multiplexed with the $\overline{CTS1}$ signal for ASCI channel 1.

ST. Status (Output). This signal is used with the $\overline{M1}$ and $\overline{HALT}$ output to decode the status of the CPU machine cycle. See Table 3.

Table 3. Status Summary

ST	$\overline{HALT}$	$\overline{M1}$	Operation
0	1	0	CPU Operation (1st Opcode Fetch)
1	1	0	CPU Operation (2nd Opcode and 3rd Opcode Fetch)
1	1	1	CPU Operation (MC Except Opcode Fetch)
0	X	1	DMA Operation
0	0	0	HALT Mode
1	0	1	SLEEP Mode (Including SYSTEM STOP Mode)

Notes:
X = Do not care.
MC = Machine Cycle.

$\overline{TEND0}$, $\overline{TEND1}$. Transfer End 0 and 1 (Outputs, active Low). This output is asserted active during the most recent WRITE cycle of a DMA operation. It is used to indicate the end of the block transfer. $\overline{TEND0}$ is multiplexed with CKA1.

TEST. Test (Output, not in DIP version). This pin is for test and should be left open.

T_{OUT}. Timer Out (Output). T_{OUT} is the output from PRT channel 1. This line is multiplexed with A18 of the address bus.

TXA0, TXA1. Transmit Data 0 and 1 (Outputs). These signals are the transmitted data from the ASCI channels. Transmitted data changes are with respect to the falling edge of the transmit clock.

TXS. Clocked Serial Transmit Data (Output). This line is the transmitted data from the CSI/O channel.

$\overline{WAIT}$. Wait (Input, active Low). $\overline{WAIT}$ indicates to the MPU that the addressed memory or I/O devices are not ready for data transfer. This input is sampled on the falling edge of T2 (and subsequent WAIT states). If the input is sampled Low, then the additional WAIT states are inserted until the $\overline{WAIT}$ input is sampled High, at which time execution continues.

$\overline{WR}$. WRITE (Output, active Low, 3-state). $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

XTAL. Crystal Oscillator Connection (Input). This pin should be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (see DC Characteristics).

Several pins are used for different conditions, depending on the circumstance.

ARCHITECTURE (Continued)

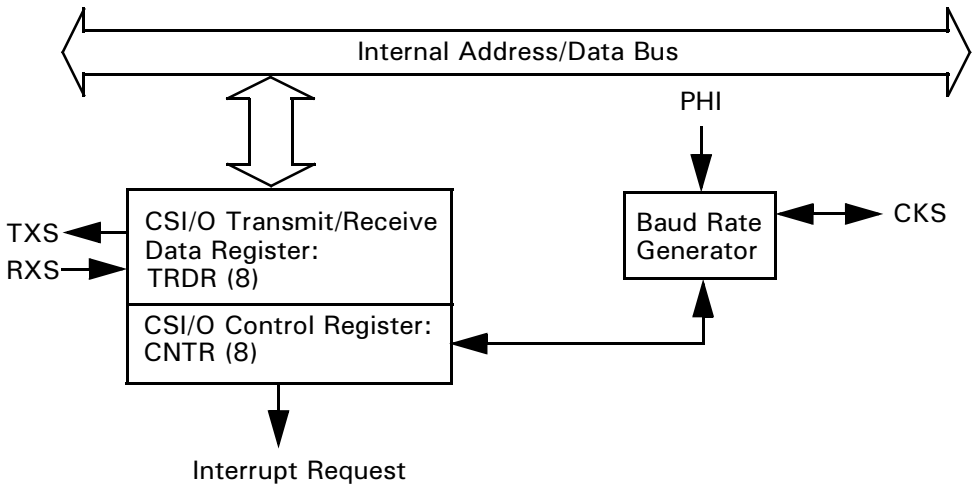


Figure 7. CSI/O Block Diagram

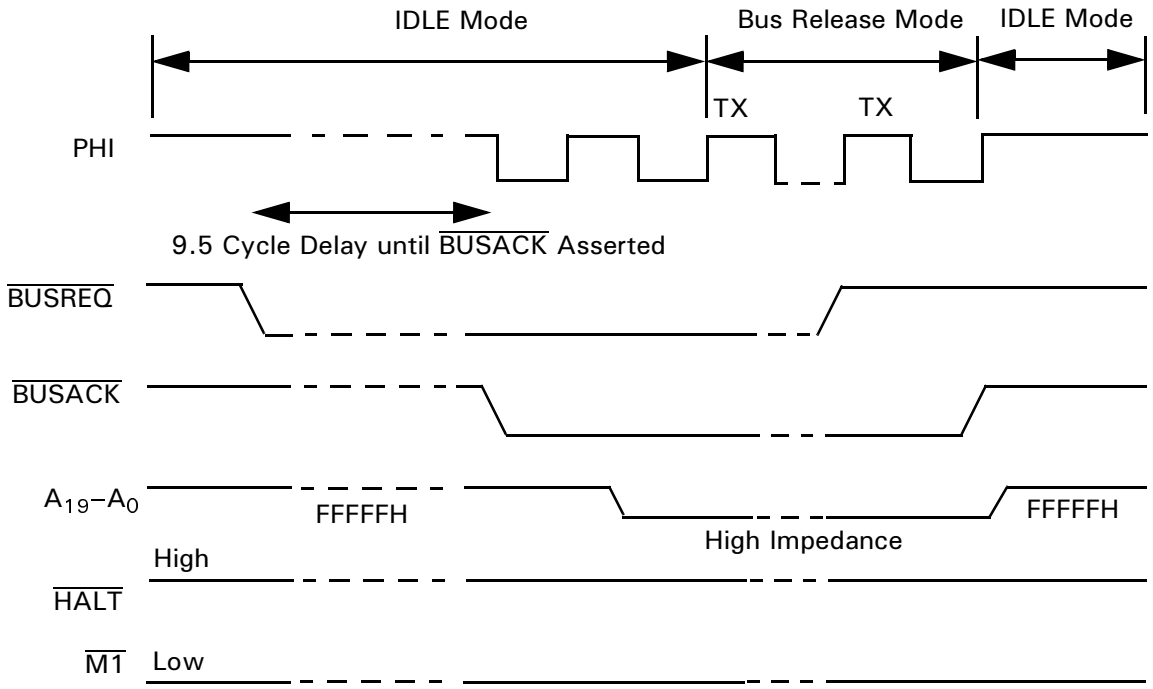


Figure 16. Bus Granting to External Master in IDLE Mode

STANDBY Mode (With or Without QUICK RECOVERY).

Software can put the Z8S180/Z8L180 into this mode by setting the IOSTOP bit (ICR5) to 1, CCR6 to 1, and executing the SLP instruction. This mode stops the on-chip oscillator and thus draws the least power of any mode, less than 10µA.

As with IDLE mode, the Z8S180/Z8L180 leaves STANDBY mode in response to a Low on $\overline{\text{RESET}}$, on $\overline{\text{NMI}}$, or a Low on $\overline{\text{INT0–2}}$ that is enabled by a 1 in the corresponding bit in the INT/TRAP Control Register. This action grants the bus to an external Master if the BREXT bit in the CPU Control Register (CCR5) is 1. The time required for all of these operations is greatly increased by the necessity for restarting the on-chip oscillator, and ensuring that it stabilizes to square-wave operation.

When an external clock is connected to the EXTAL pin rather than a crystal to the XTAL and EXTAL pins and the external clock runs continuously, there is little necessity to use STANDBY mode because no time is required to restart the oscillator, and other modes restart faster. However, if external logic stops the clock during STANDBY mode (for example, by decoding $\overline{\text{HALT}}$ Low and $\overline{\text{M1}}$ High for several clock cycles), then STANDBY mode can be useful to allow the external clock source to stabilize after it is re-enabled.

When external logic drives $\overline{\text{RESET}}$ Low to bring the device out of STANDBY mode, and a crystal is in use or an external clock source is stopped, the external logic must hold $\overline{\text{RESET}}$ Low until the on-chip oscillator or external clock source is restarted and stabilized.

The clock-stability requirements of the Z8S180/Z8L180 are much less in the divide-by-two mode that is selected by a RESET sequence and controlled by the Clock Divide bit in the CPU Control Register (CCR7). As a result, software performs the following actions:

1. Sets CCR7 to 0 for divide-by-two mode before an SLP instruction and STANDBY mode.
2. Delays setting CCR7 back to 1 for divide-by-one mode as long as possible to allow additional clock stabilization time after a RESET, interrupt, or in-line RESTART after an SLP 01 instruction.

If CCR6 is set to 1 before the SLP instruction places the MPU in STANDBY mode, the value of the CCR3 bit determines the length of the delay before the oscillator restarts and stabilizes when it leaves STANDBY mode due to an external interrupt request. When CCR3 is 0, the Z8S180/Z8L180 waits 2^{17} (131,072) clock cycles. When CCR3 is 1, it waits 64 clock cycles. This state is called QUICK RECOVERY mode. The same delay applies to grant-

ing the bus to an external Master during STANDBY mode, when the BREXT bit in the CPU Control Register (CCR5) is 1.

As described previously for SLEEP and IDLE modes, when the MPU leaves STANDBY mode due to $\overline{NMI}$ Low or an enabled $\overline{INT0}$–$\overline{INT2}$ Low when the IEF, flag is 1 due to an IE instruction, it starts by performing the interrupt with the return address being that of the instruction following the SLP instruction. If the Z8S180/Z8L180 leaves STANDBY mode due to an external interrupt request that's enabled in the INT/TRAP Control Register, but the IEF, bit is 0 due to a DI instruction, the processor restarts by executing the instruction(s) following the SLP instruction. If $\overline{INT0}$, or $\overline{INT1}$ or $\overline{INT2}$ goes inactive before the end of the clock stabilization delay, the Z8S180/Z8L180 stays in STANDBY mode.

Figure 17 indicates the timing for leaving STANDBY mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes either 64 or 2^{17} (131,072) clocks to restart, depending on the CCR3 bit.

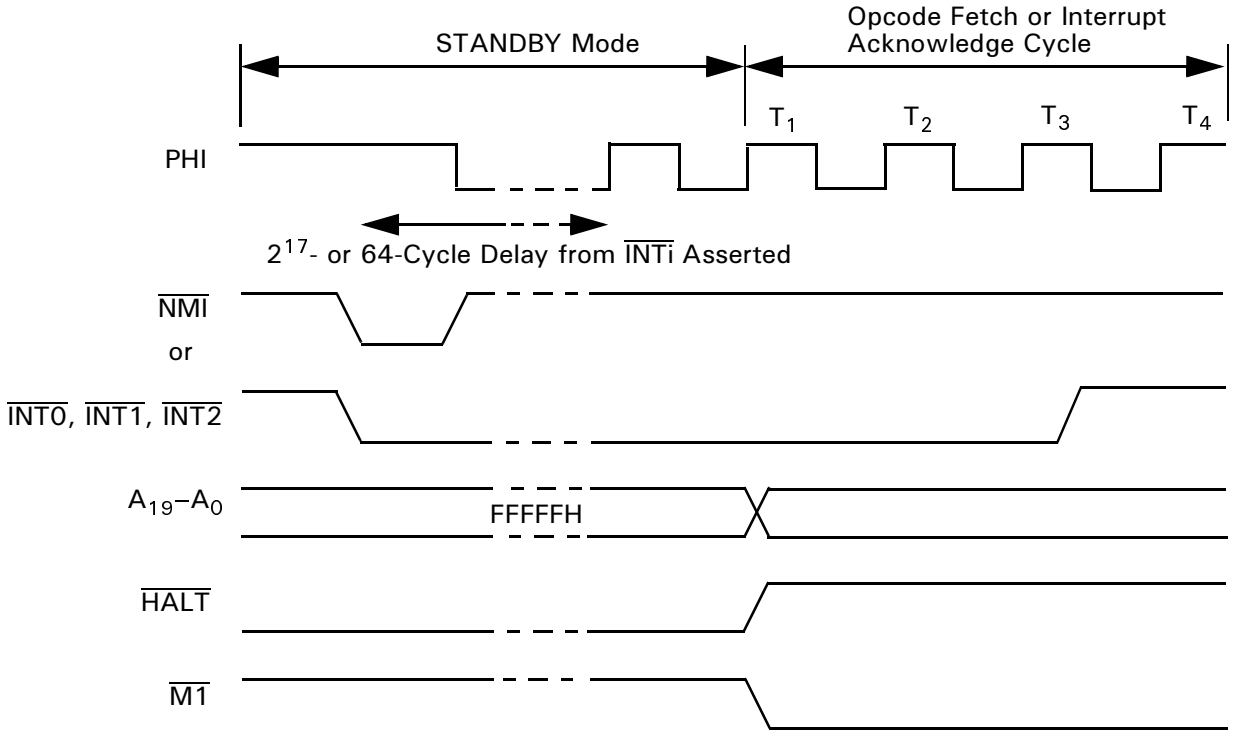


Figure 17. Z8S180/Z8L180 STANDBY Mode Exit Due to External Interrupt

While the Z8S180/Z8L180 is in STANDBY mode, it grants the bus to an external Master if the BREXT bit (CCR5) is 1. Figure 18 indicates the timing of this sequence. The device takes 64 or 2^{17} (131,072) clock cycles to grant the bus depending on the CCR3 bit. The latter (not the QUICK RECOVERY) case may be prohibitive for many demand-driven external Masters. If so, QUICK RECOVERY or IDLE mode can be used.

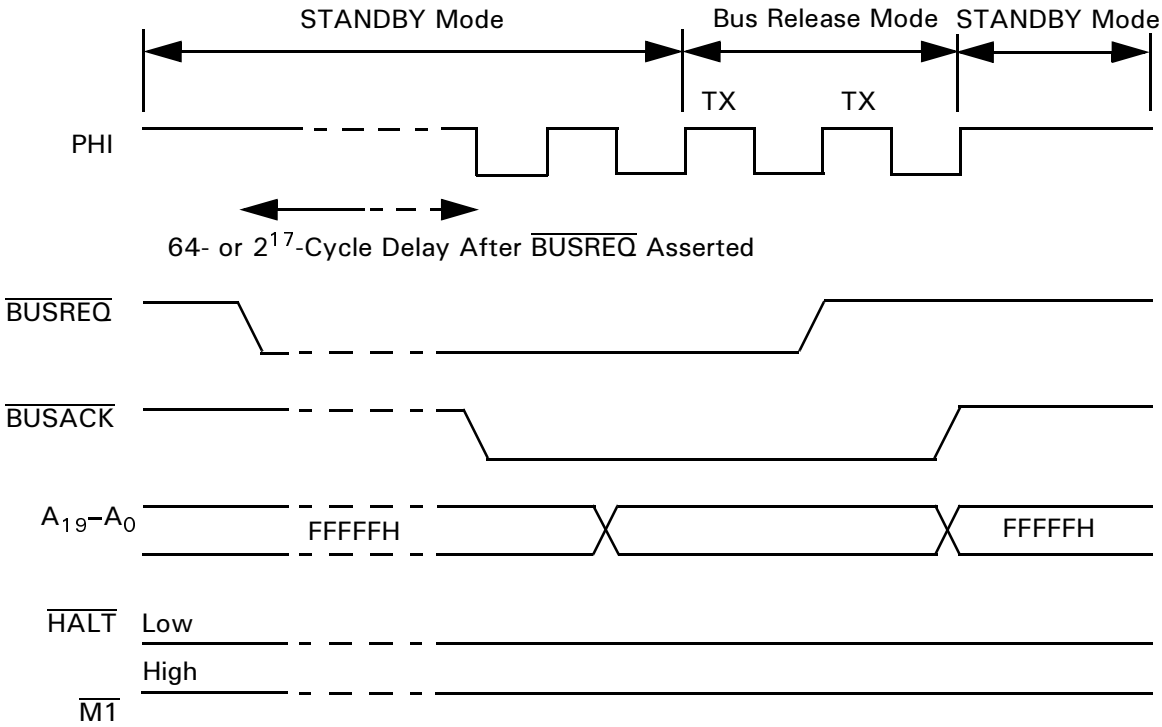


Figure 18. Bus Granting to External Master During STANDBY Mode

DC CHARACTERISTICS—Z8S180

Table 6. Z8S180 DC Characteristics
V_{DD} = 5V ±10%; V_{SS} = 0V

Symbol	Item	Condition	Min	Typ	Max	Unit
V_{IH1}	Input H Voltage $\overline{RESET}$, EXTAL, $\overline{NMI}$		V_{DD} –0.6	—	V_{DD} +0.3	V
V_{IH2}	Input H Voltage Except $\overline{RESET}$, EXTAL, $\overline{NMI}$		2.0	—	V_{DD} +0.3	V
V_{IH3}	Input H Voltage CKS, CKA0, CKA1		2.4	—	V_{DD} +0.3	V
V_{IL1}	Input L Voltage RESET, EXTAL, NMI		–0.3	—	0.6	V
V_{IL2}	Input L Voltage Except RESET, EXTAL, NMI		–0.3	—	0.8	V
V_{OH}	Outputs H Voltage All outputs	I_{OH} = –200 µA	2.4	—	—	V
		I_{OH} = –20 µA	V_{DD} –1.2	—	—	
V_{OL}	Outputs L Voltage All outputs	I_{OL} = 2.2 mA	—	—	0.45	V
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL	V_{IN} = 0.5 ~ V_{DD} –0.5	—	—	1.0	µA
I_{TL}	Three State Leakage Current	V_{IN} = 0.5 ~ V_{DD} –0.5	—	—	1.0	µA
I_{DD}[1]	Power Dissipation (Normal Operation)	F = 10 MHz	—	25	60	mA
		20		30	50	
		33		60	100	
	Power Dissipation (SYSTEM STOP mode)	F = 10 MHz	—	2	5	
		20		3	6	
		33		5	9	
C_P	Pin Capacitance	V_{IN} = 0_V, f = 1 MHz T_A = 25°C	—	—	12	pF

Note:
1. V_{IHmin} = V_{DD}–1.0V, V_{ILmax} = 0.8V (All output terminals are at NO LOAD.) V_{DD} = 5.0V.

Table 7. Z8L180 DC Characteristics
V_{DD} = 3.3V ±10%; V_{SS} = 0V

Symbol	Item	Condition	Min	Typ	Max	Unit
V_{IH1}	Input H Voltage $\overline{RESET}$, EXTAL, $\overline{NMI}$		V_{DD} –0.6		V_{DD} +0.3	V
V_{IH2}	Input H Voltage Except $\overline{RESET}$, EXTAL, $\overline{NMI}$		2.0		V_{DD} +0.3	V
V_{IL1}	Input L Voltage RESET, EXTAL, NMI		–0.3		0.6	V
V_{IL2}	Input L Voltage Except RESET, EXTAL, NMI		–0.3		0.8	V
V_{OH}	Outputs H Voltage All outputs	I_{OH} = –200 µA	2.15			V
		I_{OH} = –20 µA	V_{DD} –0.6			V
V_{OL}	Outputs L Voltage All Outputs	I_{OL} = 4 mA			0.4	V
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL	V_{IN} = 0.5 ~ V_{DD} –0.5			1.0	µA
I_{TL}	Three State Leakage Current	V_{IN} = 0.5 ~ V_{DD} –0.5			1.0	µA
I_{DD1}	Power Dissipation (Normal Operation)	F = 20 MHz		30	60	mA
		4 MHz		4	10	
	Power Dissipation (SYSTEM STOP mode)	F = 20 MHz		5	10	
		4 MHz		2	5	
C_P	Pin Capacitance	V_{IN} = 0V, f = 1 MHz T_A = 25° C			12	pF

Note:
1. V_{IHmin} = V_{DD} –1.0V, V_{ILmax} = 0.6V (All output terminals are at NO LOAD.) V_{DD} = 3.0V.

Table 8. Z8S180 AC Characteristics (Continued)
V_{DD} = 5V ±10% or V_{DD} = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation

			Z8S180—20 MHz		Z8S180—33 MHz		
Number	**Symbol**	**Item**	**Min**	**Max**	**Min**	**Max**	**Unit**
63	t_{REH}	$\overline{RESET}$ Hold Time from PHI Fall	25	—	15	—	ns
64	t_{OSC}	Oscillator Stabilization Time	—	20	—	20	ns
65	t_{EXR}	External Clock Rise Time (EXTAL)	—	5	—	5	ns
66	t_{EXF}	External Clock Fall Time (EXTAL)	—	5	—	5	ns
67	t_{RR}	$\overline{RESET}$ Rise Time	—	50	—	50	ms
68	t_{RF}	$\overline{RESET}$ Fall Time	—	50	—	50	ms
69	t_{IR}	Input Rise Time (except EXTAL, $\overline{RESET}$)	—	50	—	50	ns
70	t_{IF}	Input Fall Time (except EXTAL, $\overline{RESET}$)	—	50	—	50	ns

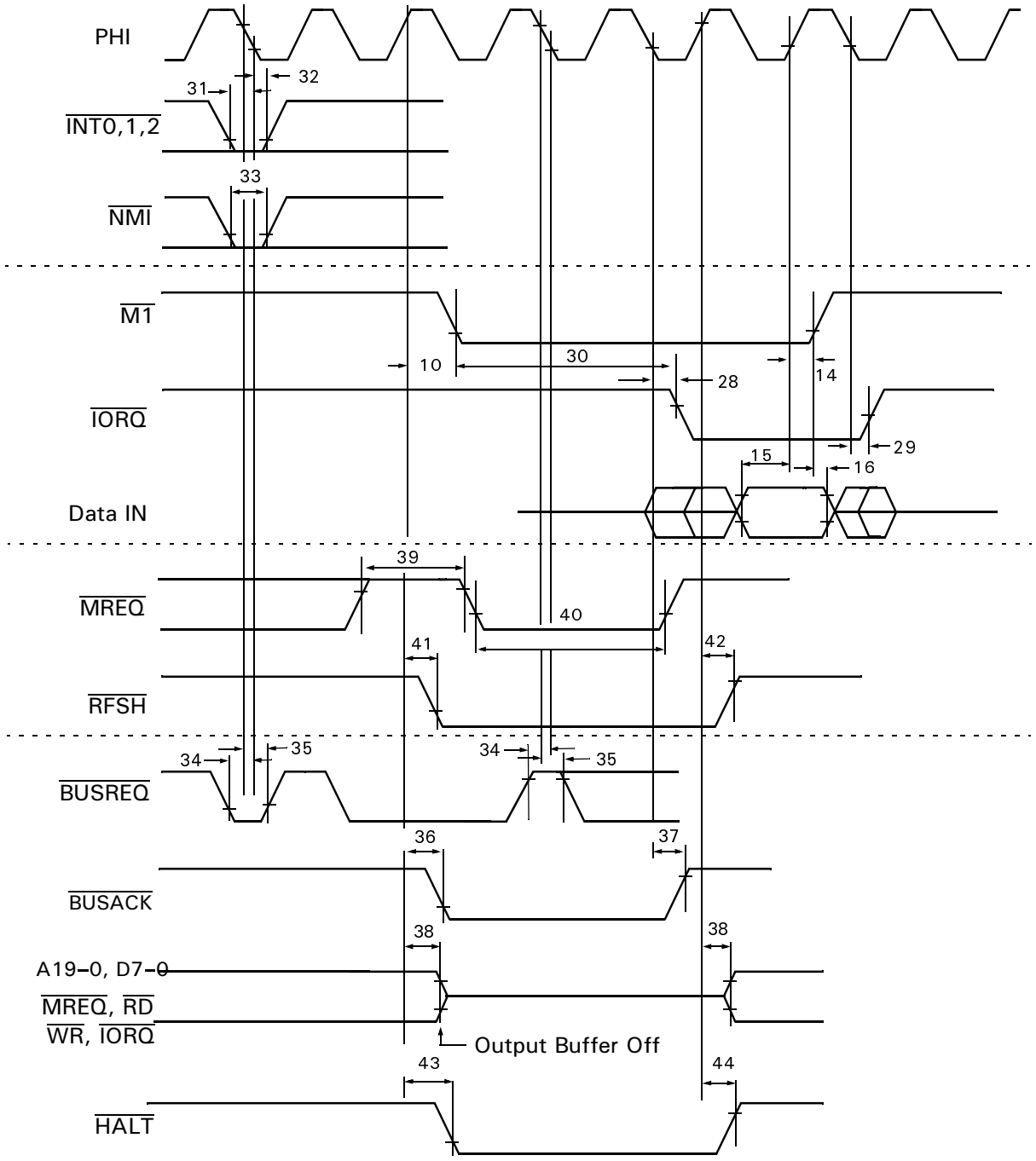


Figure 21. CPU Timing
(INT0 Acknowledge Cycle, Refresh Cycle, BUS RELEASE Mode, HALT Mode, SLEEP Mode, SYSTEM STOP Mode)

Bit 2 LNIO. This bit controls the drive capability of certain external I/O pins of the Z8S180/Z8L180. When this bit is set to 1, the output drive capability of the following pins is reduced to 33 percent of the original drive capability:

$\overline{RTS0}$	TxS
CKA1/$\overline{TEND0}$	CKA0/$\overline{DREQ0}$
TXA0	TXA1
$\overline{TENDi}$	CKS

Bit 1 LNCPUCTL. This bit controls the drive capability of the CPU Control pins. When this bit is set to 1, the output drive capability of the following pins is reduced to 33 percent of the original drive capability:

$\overline{BUSACK}$	$\overline{RD}$
$\overline{WR}$	$\overline{M1}$
$\overline{MREQ}$	$\overline{IORQ}$
$\overline{RFSH}$	$\overline{HALT}$
E	TEST
ST	

Bit 0 LNAD/DATA. This bit controls the drive capability of the Address/Data bus output drivers. If this bit is set to 1, the output drive capability of the Address and Data bus outputs is reduced to 33 percent of its original drive capability.

ASCI RECEIVE REGISTER

Register addresses 08H and 09H hold the ASCI receive data for channel 0 and channel 1, respectively.

ASCI Receive Register Channel 0

Mnemonic RDR0
Address 08H

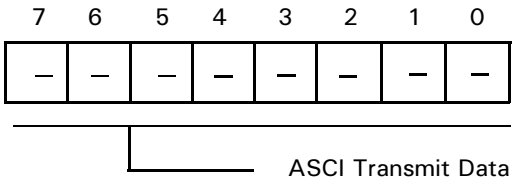


Figure 38. ASCI Receive Register Channel 0

ASCI Receive Register Channel 1

Mnemonic RDR1
Address 09H

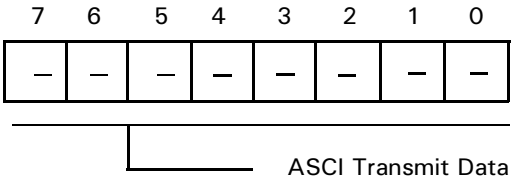


Figure 39. ASCI Receive Register Channel 1

CSI/O CONTROL/STATUS REGISTER

The CSI/O Control/Status Register (CNTR) is used to monitor CSI/O status, enable and disable the CSI/O, enable and disable interrupt generation, and select the data clock speed and source.

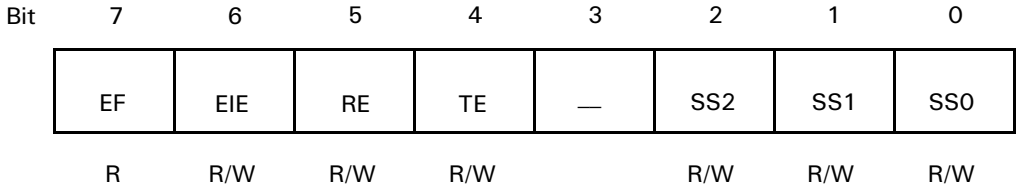


Figure 40. CSI/O Control Register (CNTR: I/O Address = 000AH)

EF: End Flag (Bit 7). EF is set to 1 by the CSI/O to indicate completion of an 8-bit data transmit or receive operation. If End Interrupt Enable (EIE) bit = 1 when EF is set to 1, a CPU interrupt request is generated. Program access of TRDR only occurs if EF = 1. The CSI/O clears EF to 0 when TRDR is read or written. EF is cleared to 0 during RESET and IOSTOP mode.

EIE: End Interrupt Enable (Bit 6). EIE is set to 1 to generate a CPU interrupt request. The interrupt request is inhibited if EIE is reset to 0. EIE is cleared to 0 during RESET.

RE: Receive Enable (Bit 5). A CSI/O receive operation is started by setting RE to 1. When RE is set to 1, the data clock is enabled. In internal clock mode, the data clock is output from the CKS pin. In external clock mode, the clock is input on the CKS pin. In either case, data is shifted in on the RXS pin in synchronization with the (internal or external) data clock. After receiving 8 bits of data, the CSI/O automatically clears RE to 0, EF is set to 1, and an interrupt (if enabled by EIE = 1) is generated. RE and TE are never both set to 1 at the same time. RE is cleared to 0 during RESET and IOSTOP mode.

TE: Transmit Enable (Bit 4). A CSI/O transmit operation is started by setting TE to 1. When TE is set to 1, the data clock is enabled. When in internal clock mode, the data clock is output from the CKS pin. In external clock mode, the clock is input on the CKS pin. In either case, data is shifted out on the TXS pin synchronous with the (internal or external) data clock. After transmitting 8 bits of data, the CSI/O automatically clears TE to 0, sets EF to 1, and requests an interrupt if enabled by EIE = 1. TE and RE are

DMA DESTINATION ADDRESS REGISTER CHANNEL 0

The DMA Destination Address Register Channel 0 specifies the physical destination address for channel 0 transfers. The register contains 20 bits and can specify up to 1024-KB memory addresses or up to 64-KB I/O addresses. Channel 0 destination can be memory, I/O, or memory mapped I/O. For I/O, the MS bits of this register identify the Request Handshake signal for channel 0.

DMA Destination Address Register Channel 0 Low

Mnemonic DAR0L
Address 23H

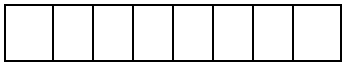


Figure 58. DMA Destination Address Register Channel 0 Low

DMA Destination Address Register Channel 0 High

Mnemonic DAR0H
Address 24H

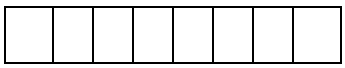


Figure 59. DMA Destination Address Register Channel 0 High

DMA Destination Address Register Channel 0B

Mnemonic DAR0B
Address 25H

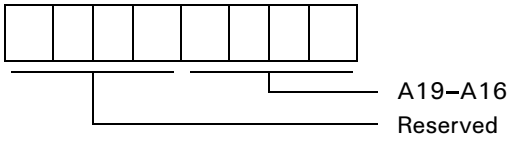


Figure 60. DMA Destination Address Register Channel 0B

If the DMA destination is in I/O space, bits 1–0 of this register select the DMA request signal for DMA0, as follows:

Bit 1 (A17)	Bit 0 (A16)	DMA Transfer Request
0	0	DREQ0 (external)
0	1	TDR0 (ASCI0)
1	0	TDR1 (ASCI1)
1	1	Not Used

DMA STATUS REGISTER

The DMA Status Register (DSTAT) is used to enable and disable DMA transfer and DMA termination interrupts. DSTAT also indicates DMA transfer status, Completed or In Progress.

DMA Status Register

Mnemonic DSTAT
Address 30H

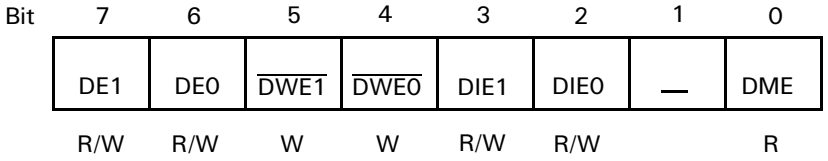


Figure 71. DMA Status Register (DSTAT: I/O Address = 30H)

DE1: DMA Enable Channel 1 (Bit 7). When DE1 = 1 and DME = 1, channel 1 DMA is enabled. When a DMA transfer terminates (BCR1 = 0), DE1 is reset to 0 by the DMAC. When DE1 = 0 and the DMA interrupt is enabled (DIE1 = 1), a DMA interrupt request is made to the CPU.

To perform a software WRITE to DE1, $\overline{\text{DWE1}}$ should be written with a 0 during the same register WRITE access. Writing DE1 to 0 disables channel 1 DMA, but DMA is restartable. Writing DE1 to 1 enables channel 1 DMA and automatically sets DMA Main Enable (DME) to 1. DE1 is cleared to 0 during RESET.

DE0: DMA Enable Channel 0 (Bit 6). When DE0 = 1 and DME = 1, channel 0 DMA is enabled. When a DMA transfer terminates (BCR0 = 0), DE0 is reset to 0 by the DMAC. When DE0 = 0 and the DMA interrupt is enabled (DIE0 = 1), a DMA interrupt request is made to the CPU.

To perform a software WRITE to DE0, $\overline{\text{DWE0}}$ should be written with 0 during the same register WRITE access. Writing DE0 to 0 disables channel 0 DMA. Writing DE0 to 1 enables channel 0 DMA and automatically sets DMA Main Enable (DME) to 1. DE0 is cleared to 0 during RESET.

$\overline{\text{DWE1}}$: DE1 Bit Write Enable (Bit 5). When performing any software WRITE to DE1, this bit should be written with 0 during the same access. $\overline{\text{DWE1}}$ always reads as 1.

$\overline{\text{DWE0}}$: DE0 Bit Write Enable (Bit 4). When performing any software WRITE to DE0, this bit should be written with 0 during the same access. $\overline{\text{DWE0}}$ always reads as 1.

DIE1: DMA Interrupt Enable Channel 1 (Bit 3). When DIE0 is set to 1, the termination channel 1 DMA transfer (indicated when DE1 = 0) causes a CPU interrupt request to be generated. When DIE0 = 0, the channel 0 DMA termination interrupt is disabled. DIE0 is cleared to 0 during RESET.

DIE0: DMA Interrupt Enable Channel 0 (Bit 2). When DIE0 is set to 1, the termination channel 0 of DMA transfer (indicated when DE0 = 0) causes a CPU interrupt request to be generated. When DIE0 = 0, the channel 0 DMA termination interrupt is disabled. DIE0 is cleared to 0 during RESET.

DME: DMA Main Enable (Bit 0). A DMA operation is only enabled when its DE bit (DE0 for channel 0, DE1 for channel 1) and the DME bit is set to 1.

When $\overline{\text{NMI}}$ occurs, DME is reset to 0, thus disabling DMA activity during the $\overline{\text{NMI}}$ interrupt service routine. To restart DMA, DE– and/or DE1 should be written with a 1 (even if the contents are already 1). This condition automatically sets DME to 1, allowing DMA operations to continue.

Note: DME cannot be directly written. The bit is cleared to 0 by $\overline{\text{NMI}}$ or indirectly set to 1 by setting DE0 and/or DE1 to 1. DME is cleared to 0 during RESET.

INTERRUPT VECTOR LOW REGISTER

Bits 7–5 of the Interrupt Vector Low Register (I_L) are used as bits 7–5 of the synthesized interrupt vector during interrupts for the $\overline{INT1}$ and $\overline{INT2}$ pins and for the DMAs, ASCIs, PRTs, and CSI/O. These three bits are cleared to 0 during RESET (Figure 74).

Interrupt Vector Low Register

Mnemonic: IL
Address 33H

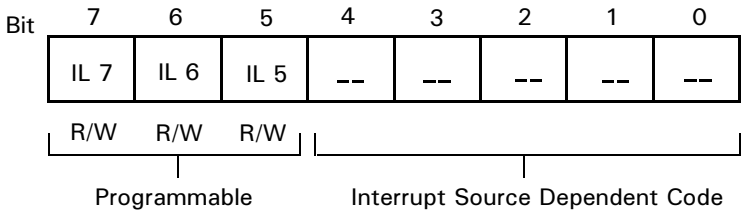


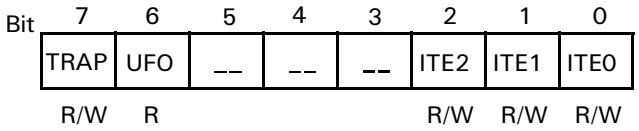
Figure 74. Interrupt Vector Low Register (IL: I/O Address = 33H)

INT/TRAP CONTROL REGISTER

This register is used in handling TRAP interrupts and to enable or disable Maskable Interrupt Level 0 and the $\overline{INT1}$ and $\overline{INT2}$ pins.

INT/TRAP Control Register

Mnemonics ITC
Address 34H



TRAP (Bit 7). This bit is set to 1 when an undefined opcode is fetched. TRAP can be reset under program control by writing it with a 0; however, TRAP cannot be written with 1 under program control. TRAP is reset to 0 during RESET.

UFO: Undefined Fetch Object (Bit 6). When a TRAP interrupt occurs, the contents of UFO allow the starting address of the undefined instruction to be determined. This interrupt is necessary because the TRAP may occur on either the second or third byte of the opcode. UFO allows the stacked PC value to be correctly adjusted. If UFO = 0, the first opcode should be interpreted as the stacked PC-1. If UFO = 1, the first opcode address is stacked PC-2. UFO is Read-Only.

ITE2, 1, 0: Interrupt Enable 2, 1, 0 (Bits 2–0). ITE2 and ITE1 enable and disable the external interrupt inputs $\overline{INT2}$ and $\overline{INT1}$, respectively. ITE0 enables and disables interrupts from:

- ESCC
- Bidirectional Centronics controller
- CTCs
- External interrupt input $\overline{INT0}$

A 1 in a bit enables the corresponding interrupt level while a 0 disables it. A RESET sets ITE0 to 1 and clears ITE1 and ITE2 to 0.

TRAP Interrupt. The Z8S180/Z8L180 generates a TRAP sequence when an undefined opcode fetch occurs. This feature can be used to increase software reliability, implement an *extended* instruction set, or both. TRAP may occur during opcode fetch cycles and also if an undefined opcode is fetched during the interrupt acknowledge cycle for $\overline{INT0}$ when Mode 0 is used.

When a TRAP sequence occurs, the Z8S180/Z8L180:

1. Sets the TRAP bit in the Interrupt TRAP/Control (ITC) register to 1.
2. Saves the current Program Counter (PC) value, reflecting the location of the undefined opcode, on the stack.
3. Resumes execution at logical address 0.

Note: If logical address 0000H is mapped to physical address 00000H, the vector is the same as for RESET. In this case, testing the TRAP bit in ITC reveals whether the restart at physical address 00000H was caused by RESET or TRAP.

All TRAPs occur after fetching an undefined second opcode byte following one of the prefix opcodes (CBH, DDH, EDH, or FDH) or after fetching an undefined third opcode byte following one of the double-prefix opcodes (DDCBH or FDCBH).

The state of the Undefined Fetch Object (UFO) bit in ITC allows TRAP software to correctly *adjust* the stacked PC, depending on whether the second or third byte of the opcode generated the TRAP. If UFO = 0, the starting address of the invalid instruction is the stacked PC–1. If UFO = 1, the starting address of the invalid instruction is equal to the stacked PC–2.

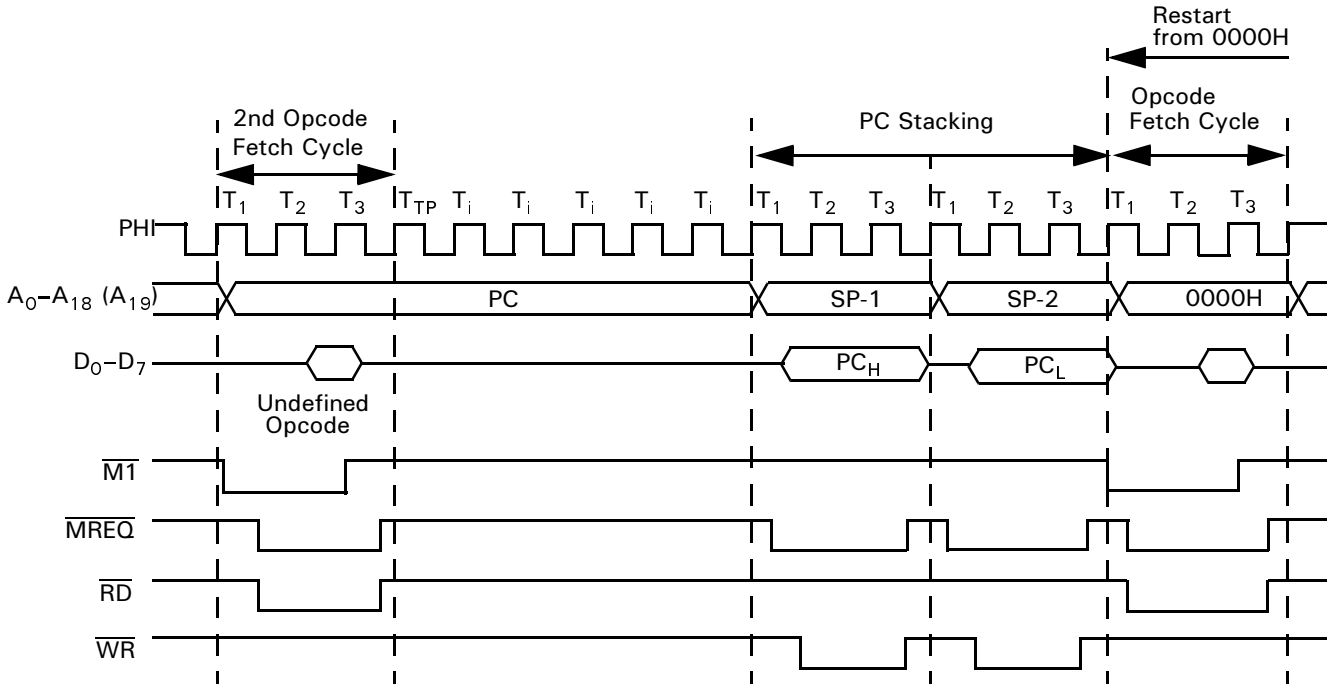


Figure 75. TRAP Timing—2nd Opcode Undefined

REFRESH CONTROL REGISTER

Mnemonic RCR
Address 36H

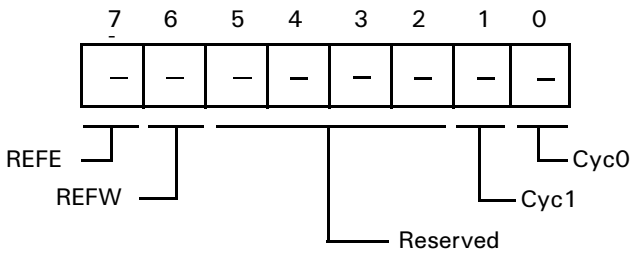


Figure 77. Refresh Control Register (RCR: I/O Address = 36H)

The Refresh Control Register (RCR) specifies the interval and length of refresh cycles, while enabling or disabling the refresh function.

REFE: Refresh Enable (Bit 7). REFE = 0 disables the refresh controller, while REFE = 1 enables refresh cycle insertion. REFE is set to 1 during RESET.

REFW: Refresh Wait (Bit 6). REFW = 0 causes the refresh cycle to be two clocks in duration. REFW = 1 causes the refresh cycle to be three clocks in duration by adding a refresh wait cycle (TRW). REFW is set to 1 during RESET.

CYC1, 0: Cycle Interval (Bit 1,0). CYC1 and CYC0 specify the interval (in clock cycles) between refresh cycles. When dynamic RAM requires 128 refresh cycles every 2 ms (or 256 cycles in every 4 ms), the required refresh interval is less than or equal to 15.625 µs. Thus, the underlined values indicate the best refresh interval depending on CPU clock frequency. CYC0 and CYC1 are cleared to 0 during RESET (see Table 18).

Table 18. DRAM Refresh Intervals

			Time Interval				
CYC1	**CYC0**	**Insertion Interval**	**PHI: 10 MHz**	**8 MHz**	**6 MHz**	**4 MHz**	**2.5 MHz**
0	0	10 states	(1.0 µs)*	(1.25 µs)*	1.66 µs	2.5 µs	4.0 µs
0	1	20 states	(2.0 µs)*	(2.5 µs)*	3.3 µs	5.0 µs	8.0 µs
1	0	40 states	(4.0 µs)*	(5.0 µs)*	6.6 µs	10.0 µs	16.0 µs
1	1	80 states	(8.0 µs)*	(10.0 µs)*	13.3 µs	20.0 µs	32.0 µs

Note: *calculated interval.

Refresh Control and Reset. After RESET, based on the initialized value of RCR, refresh cycles occur with an interval of 10 clock cycles and be 3 clock cycles in duration.

Dynamic RAM Refresh Operation

1. Refresh Cycle insertion is stopped when the CPU is in the following states:
   a. During RESET
   b. When the bus is released in response to $\overline{\text{BUSREQ}}$
   c. During SLEEP mode
   d. During $\overline{\text{WAIT}}$ states
2. Refresh cycles are suppressed when the bus is released in response to $\overline{\text{BUSREQ}}$. However, the refresh timer continues to operate. The time at which the first refresh cycle occurs after the Z8S180/Z8L180 reacquires the bus depends on the refresh timer. This cycle offers no timing relationship with the bus exchange.
3. Refresh cycles are suppressed during SLEEP mode. If a refresh cycle is requested during SLEEP mode, the refresh cycle request is internally latched (until replaced with the next refresh request). The latched refresh cycle is inserted at the end of the first machine cycle after SLEEP mode is exited. After this initial cycle, the time at which the next refresh cycle occurs depends on the refresh time and offers no relationship with the exit from SLEEP mode.
4. The refresh address is incremented by one for each successful refresh cycle, not for each refresh. Thus, independent of the number of missed refresh requests, each refresh bus cycle uses a refresh address incremented by one from that of the previous refresh bus cycles.

I/O CONTROL REGISTER

The I/O Control Register (ICR) allows relocation of the internal I/O addresses. ICR also controls the enabling and disabling of IOSTOP mode (Figure 83).

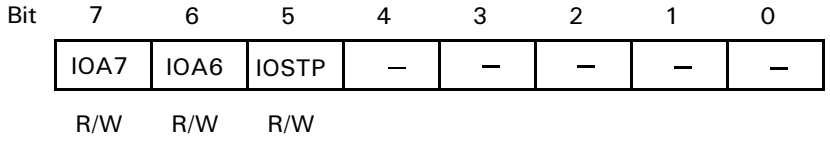


Figure 83. I/O Control Register (ICR: I/O Address = 3FH)

IOA7, 6: I/O Address Relocation (Bits 7,6). IOA7 and IOA6 relocate internal I/O as indicated in Figure 84.

Note: The high-order 8 bits of 16-bit internal I/O address are always 0. IOA7 and IOA6 are cleared to 0 during RESET.

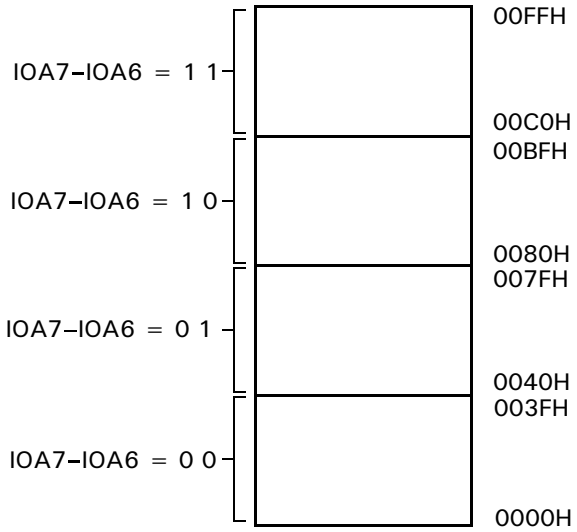
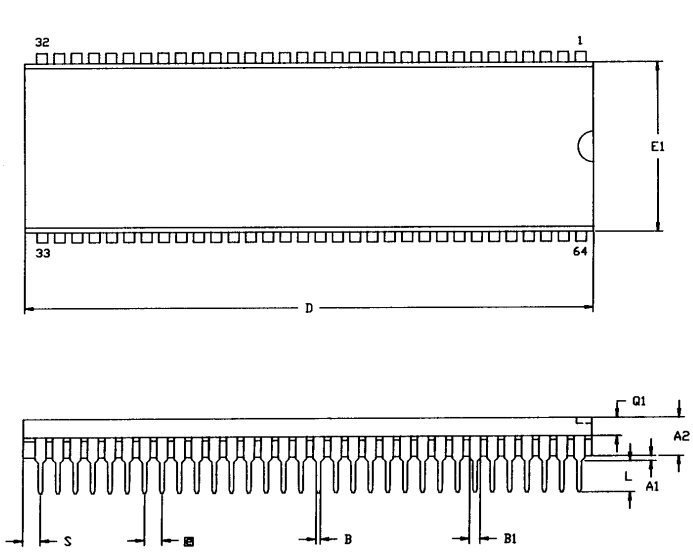


Figure 84. I/O Address Relocation

IOSTP: IOSTOP Mode (Bit 5). IOSTOP mode is enabled when IOSTP is set to 1. Normal I/O operation resumes when IOSTP is reprogrammed or RESET to 0.

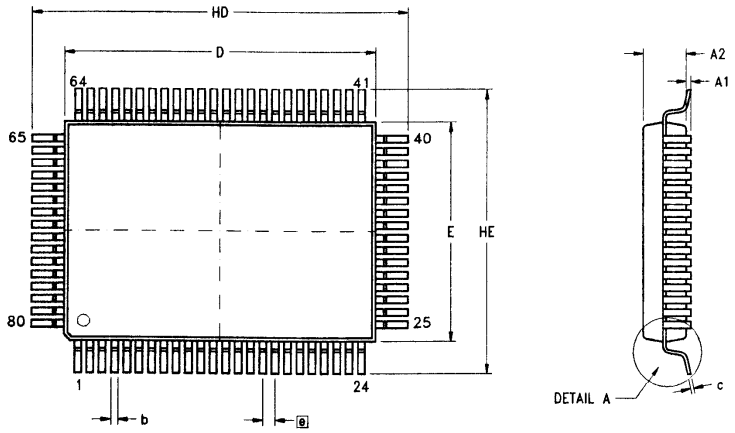
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	1.07	.015	.042
A2	3.68	3.94	.145	.155
B	0.38	0.53	.015	.021
B1	0.94	1.09	.037	.043
C	0.23	0.38	.009	.015
D	57.40	58.17	2.260	2.290
E	18.80	19.30	.740	.760
E1	16.76	17.27	.660	.680
e	1.78 TYP		.070 TYP	
eA	19.30	20.32	.760	.800
L	3.18	3.81	.125	.150
Q1	1.65	1.91	.065	.075
S	1.02	1.78	.040	.070

CONTROLLING DIMENSIONS : INCH

Figure 85. 64-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.10	0.30	.004	.012
A2	2.60	2.80	.102	.110
b	0.30	0.45	.012	.018
c	0.13	0.20	.005	.008
HD	23.70	24.15	.933	.951
D	19.90	20.10	.783	.791
HE	17.70	18.15	.697	.715
E	13.90	14.10	.547	.555
e	0.80 TYP		.0315 TYP	
L	0.70	1.10	.028	.043

NOTES:
1. CONTROLLING DIMENSIONS: MILLIMETER
2. MAX COPLANARITY: .10 / .004

Figure 86. 80-Pin QFP Package Diagram