Understanding **Embedded - Microprocessors**

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

|	
Product Status	Obsolete
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	20MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	80-BQFP
Supplier Device Package	80-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8s18020fsc1960

PIN IDENTIFICATION
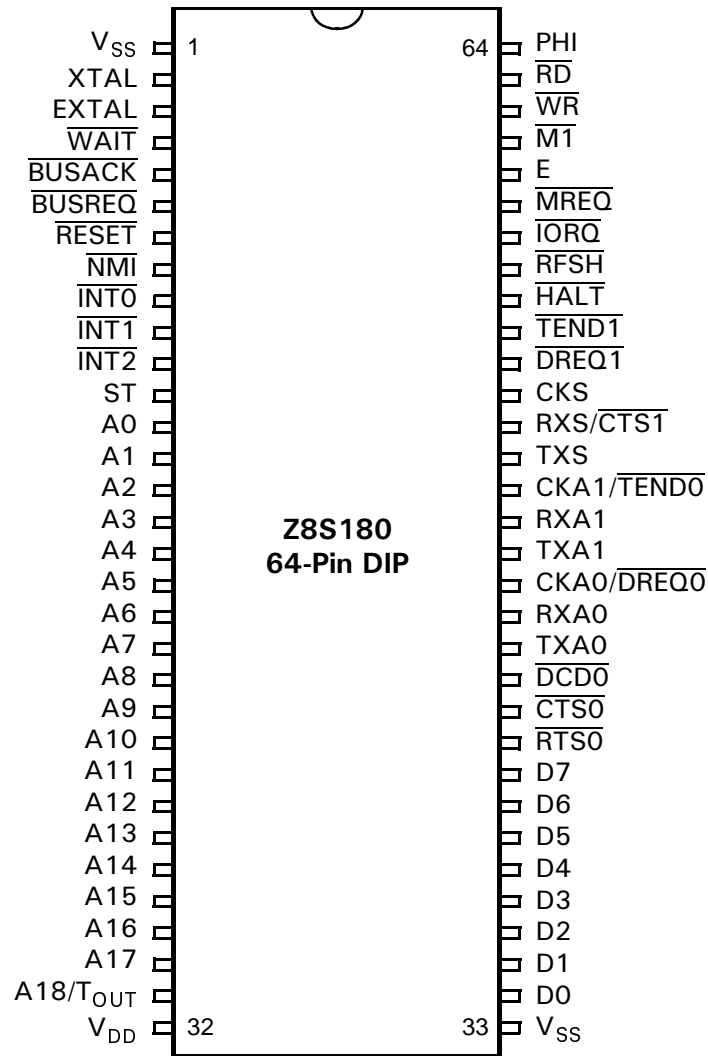
Figure 2. Z8S180 64-Pin DIP Pin Configuration

PIN IDENTIFICATION (Continued)

Table 1. Z8S180/Z8L180 Pin Identification (Continued)

Pin Number and Package Type			Default	Secondary	
QFP	PLCC	DIP	Function	Function	Control
13	19	17	A4		
14			NC		
15	20	18	A5		
16	21	19	A6		
17	22	20	A7		
18	23	21	A8		
19	24	22	A9		
20	25	23	A10		
21	26	24	A11		
22			NC		
23			NC		
24	27	25	A12		
25	28	26	A13		
26	29	27	A14		
27	30	28	A15		
28	31	29	A16		
29	32	30	A17		
30			NC		
31	33	31	A18	T_{OUT}	Bit 2 or Bit 3 of TCR
32	34	32	V_{DD}		
33	35		A19		
34	36	33	V_{SS}		
35	37	34	D0		
36	38	35	D1		
37	39	36	D2		
38	40	37	D3		
39	41	38	D4		
40	42	39	D5		
41	43	40	D6		
42			NC		
43			NC		
44	44	41	D7		
45	45	42	$\overline{RTS0}$		
46	46	43	$\overline{CTS0}$		
47	47	44	$\overline{DCD0}$		
48	48	45	TXA0		
49	49	46	RXA0		
50	50	47	CKA0	$\overline{DREQ0}$	Bit 3 or Bit 5 of DMODE
51			NC		
52	51	48	TXA1		

PIN IDENTIFICATION (Continued)

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
1	9	8	$\overline{\text{NMI}}$		IN	IN	IN
2			NC				
3			NC				
4	10	9	$\overline{\text{INT0}}$		IN	IN	IN
5	11	10	$\overline{\text{INT1}}$		IN	IN	IN
6	12	11	$\overline{\text{INT2}}$		IN	IN	IN
7	13	12	ST		High	High	High
8	14	13	A0		3T	3T	High
9	15	14	A1		3T	3T	High
10	16	15	A2		3T	3T	High
11	17	16	A3		3T	3T	High
12	18		V_{SS}		V_{SS}	V_{SS}	V_{SS}
13	19	17	A4		3T	3T	High
14			NC				
15	20	18	A5		3T	3T	High
16	21	19	A6		3T	3T	High
17	22	20	A7		3T	3T	High
18	23	21	A8		3T	3T	High
19	24	22	A9		3T	3T	High
20	25	23	A10		3T	3T	High
21	26	24	A11		3T	3T	High
22			NC				
23			NC				
24	27	25	A12		3T	3T	High
25	28	26	A13		3T	3T	High
26	29	27	A14		3T	3T	High
27	30	28	A15		3T	3T	High
28	31	29	A16		3T	3T	High
29	32	30	A17		3T	3T	High
30			NC				
31	33	31	A18		3T	3T	High
				T_{OUT}	N/A	OUT	OUT
32	34	32	V_{DD}		V_{DD}	V_{DD}	V_{DD}
33	35		A19		3T	3T	High
34	36	33	V_{SS}		V_{SS}	V_{SS}	V_{SS}
35	37	34	D0		3T	3T	3T
36	38	35	D1		3T	3T	3T
37	39	36	D2		3T	3T	3T
38	40	37	D3		3T	3T	3T

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
39	41	38	D4		3T	3T	3T
40	42	39	D5		3T	3T	3T
41	43	40	D6		3T	3T	3T
42			NC				
43			NC				
44	44	41	D7		3T	3T	3T
45	45	42	$\overline{RTS0}$		High	OUT	High
46	46	43	$\overline{CTS0}$		IN	OUT	IN
47	47	44	$\overline{DCD0}$		IN	IN	IN
48	48	45	TXA0		High	OUT	OUT
49	49	46	RXA0		IN	IN	IN
50	50	47	CKA0		3T	I/O	I/O
			$\overline{DREQ0}$		N/A	IN	IN
51			NC				
52	51	48	TXA1		High	OUT	OUT
53	52		TEST				
54	53	49	RXA1		IN	IN	IN
55	54	50	CKA1		3T	I/O	I/O
			$\overline{TEND0}$		N/A	High	High
56	55	51	TXS		High	OUT	OUT
57	56	52	RXS		IN	IN	IN
			$\overline{CTS1}$		N/A	IN	IN
58	57	53	CKS		3T	I/O	I/O
59	58	54	$\overline{DREQ1}$		IN	3T	IN
60	59	55	$\overline{TEND1}$		High	OUT	High
61	60	56	$\overline{HALT}$		High	High	Low
62			NC				
63			NC				
64	61	57	$\overline{RFSH}$		High	OUT	High
65	62	58	$\overline{IORQ}$		High	3T	High
66	63	59	$\overline{MREQ}$		High	3T	High
67	64	60	E		Low	OUT	OUT
68	65	61	$\overline{M1}$		High	High	High
69	66	62	$\overline{WR}$		High	3T	High
70	67	63	$\overline{RD}$		High	3T	High
71	68	64	PHI		OUT	OUT	OUT
72	1	1	V_{SS}		GND	GND	GND
73	2		V_{SS}		GND	GND	GND
74	3	2	XTAL		OUT	OUT	OUT
75			NC				

PIN DESCRIPTIONS

A0–A19. Address Bus (Output, 3-state). A0–A19 form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 1 MB) and I/O data bus exchanges (up to 64 KB). The address bus enters a high–impedance state during reset and external bus acknowledge cycles. Address line A18 is multiplexed with the output of PRT channel 1 (T_{OUT}, selected as address output on reset), and address line A19 is not available in DIP versions of the Z8S180.

$\overline{BUSACK}$. Bus Acknowledge (Output, active Low). $\overline{BUSACK}$ indicates that the requesting device, the MPU address and data bus, and some control signals enter their high-impedance state.

$\overline{BUSREQ}$. Bus Request (Input, active Low). This input is used by external devices (such as DMA controllers) to request access to the system bus. This request demands a higher priority than $\overline{NMI}$ and is always recognized at the end of the current machine cycle. This signal stops the CPU from executing further instructions, places addresses, data buses, and other control signals into the high-impedance state.

CKA0, CKA1. Asynchronous Clock 0 and 1 (bidirectional). When in output mode, these pins are the transmit and receive clock outputs from the ASCI baud rate generators. When in input mode, these pins serve as the external clock inputs for the ASCI baud rate generators. CKA0 is multiplexed with $\overline{DREQ0}$, and CKA1 is multiplexed with $\overline{TEND0}$.

CKS. Serial Clock (bidirectional). This line is the clock for the CSI/O channel.

$\overline{CTS0}$–$\overline{CTS1}$. Clear to send 0 and 1 (Inputs, active Low). These lines are modem control signals for the ASCI channels. $\overline{CTS1}$ is multiplexed with RXS.

D0–D7. Data Bus = (bidirectional, 3-state). D0–D7 constitute an 8-bit bidirectional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high-impedance state during reset and external bus acknowledge cycles.

$\overline{DCD0}$. Data Carrier Detect 0 (Input, active Low); a programmable modem control signal for ASCI channel 0.

$\overline{DREQ0}$, $\overline{DREQ1}$. DMA Request 0 and 1 (Input, active Low). $\overline{DREQ}$ is used to request a DMA transfer from one of the on-chip DMA channels. The DMA channels monitor these inputs to determine when an external device is ready for a READ or WRITE operation. These inputs can be programmed to be either level or edge sensed. $\overline{DREQ0}$ is multiplexed with CKA0.

E. Enable Clock (Output). This pin functions as a synchronous, machine-cycle clock output during bus transactions.

EXTAL. External Clock Crystal (Input). Crystal oscillator connections. An external clock can be input to the Z8S180/Z8L180 on this pin when a crystal is not used. This input is Schmitt triggered.

$\overline{HALT}$. HALT/SLEEP (Output, active Low). This output is asserted after the CPU executes either the HALT or SLEEP instruction and is waiting for either a nonmaskable or a maskable interrupt before operation can resume. It is also used with the $\overline{M1}$ and ST signals to decode the status of the CPU machine cycle.

$\overline{INT0}$. Maskable Interrupt Request 0 (Input, active Low). This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the $\overline{NMI}$ and $\overline{BUSREQ}$ signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the $\overline{M1}$ and $\overline{IORQ}$ signals become active.

$\overline{INT1}$, $\overline{INT2}$. Maskable Interrupt Request 1 and 2 (Inputs, active Low). This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the $\overline{NMI}$, $\overline{BUSREQ}$, and $\overline{INT0}$ signals are inactive. The CPU acknowledges these requests with an interrupt acknowledge cycle. Unlike the acknowledgment for $\overline{INT0}$, neither the $\overline{M1}$ or $\overline{IORQ}$ signals become active during this cycle.

$\overline{IORQ}$. I/O Request (Output, active Low, 3-state). $\overline{IORQ}$ indicates that the address bus contains a valid I/O address for an I/O READ or I/O WRITE operation. $\overline{IORQ}$ is also generated, along with $\overline{M1}$, during the acknowledgment of the $\overline{INT0}$ input signal to indicate that an interrupt response vector can be place onto the data bus. This signal is analogous to the $\overline{IOE}$ signal of the Z64180.

$\overline{M1}$. Machine Cycle 1 (Output, active Low). Together with $\overline{MREQ}$, $\overline{M1}$ indicates that the current cycle is the opcode-fetch cycle of instruction execution. Together with $\overline{IORQ}$, $\overline{M1}$ indicates that the current cycle is for interrupt acknowledgment. It is also used with the $\overline{HALT}$ and ST signal to decode the status of the CPU machine cycle. This signal is analogous to the $\overline{LIR}$ signal of the Z64180.

$\overline{MREQ}$. Memory Request (Output, active Low, 3-state). $\overline{MREQ}$ indicates that the address bus holds a valid address for a memory READ or memory WRITE operation. This signal is analogous to the $\overline{ME}$ signal of Z64180.

$\overline{NMI}$. Nonmaskable Interrupt (Input, negative edge triggered). $\overline{NMI}$ demands a higher priority than $\overline{INT}$ and is al-

PIN DESCRIPTIONS (Continued)

ways recognized at the end of an instruction, regardless of the state of the interrupt-enable flip-flops. This signal forces CPU execution to continue at location 0066H.

PHI. System Clock (Output). The output is used as a reference clock for the MPU and the external system. The frequency of this output may be one-half, equal to, or twice the crystal or input clock frequency.

RD. Read (Output, active Low, 3-state). $\overline{RD}$ indicates that the CPU wants to read data from either memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus.

RFSH. Refresh (Output, active Low). Together with $\overline{MREQ}$, $\overline{RFSH}$ indicates that the current CPU machine cycle and the contents of the address bus should be used for refresh of dynamic memories. The low-order 8 bits of the address bus (A7–A0) contain the refresh address. *This signal is analogous to the $\overline{REF}$ signal of the Z64180.*

RTS0. Request to Send 0 (Output, active Low); a programmable MODEM control signal for ASCI channel 0.

RXA0, RXA1. Receive Data 0 and 1 (Input). These signals are the receive data for the ASCI channels.

RXS. Clocked Serial Receive Data (Input). This line is the receive data for the CSI/O channel. RXS is multiplexed with the $\overline{CTS1}$ signal for ASCI channel 1.

ST. Status (Output). This signal is used with the $\overline{M1}$ and $\overline{HALT}$ output to decode the status of the CPU machine cycle. See Table 3.

Table 3. Status Summary

ST	$\overline{HALT}$	$\overline{M1}$	Operation
0	1	0	CPU Operation (1st Opcode Fetch)
1	1	0	CPU Operation (2nd Opcode and 3rd Opcode Fetch)
1	1	1	CPU Operation (MC Except Opcode Fetch)
0	X	1	DMA Operation
0	0	0	HALT Mode
1	0	1	SLEEP Mode (Including SYSTEM STOP Mode)

Notes:
X = Do not care.
MC = Machine Cycle.

TEND0, TEND1. Transfer End 0 and 1 (Outputs, active Low). This output is asserted active during the most recent WRITE cycle of a DMA operation. It is used to indicate the end of the block transfer. $\overline{TEND0}$ is multiplexed with CKA1.

TEST. Test (Output, not in DIP version). This pin is for test and should be left open.

T$_{OUT}$. Timer Out (Output). T$_{OUT}$ is the output from PRT channel 1. This line is multiplexed with A18 of the address bus.

TXA0, TXA1. Transmit Data 0 and 1 (Outputs). These signals are the transmitted data from the ASCI channels. Transmitted data changes are with respect to the falling edge of the transmit clock.

TXS. Clocked Serial Transmit Data (Output). This line is the transmitted data from the CSI/O channel.

WAIT. Wait (Input, active Low). $\overline{WAIT}$ indicates to the MPU that the addressed memory or I/O devices are not ready for data transfer. This input is sampled on the falling edge of T2 (and subsequent WAIT states). If the input is sampled Low, then the additional WAIT states are inserted until the $\overline{WAIT}$ input is sampled High, at which time execution continues.

WR. WRITE (Output, active Low, 3-state). $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

XTAL. Crystal Oscillator Connection (Input). This pin should be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (see DC Characteristics).

Several pins are used for different conditions, depending on the circumstance.

OPERATION MODES (Continued)

The Z8S180/Z8L180 leaves HALT mode in response to:

- Low on $\overline{RESET}$

- Interrupt from an enabled on-chip source

- External request on $\overline{NMI}$

- Enabled external request on $\overline{INT0}$, $\overline{INT1}$, or $\overline{INT2}$

In case of an interrupt, the return address is the instruction following the HALT instruction. The program can either branch back to the HALT instruction to wait for another interrupt or can examine the new state of the system/application and respond appropriately.
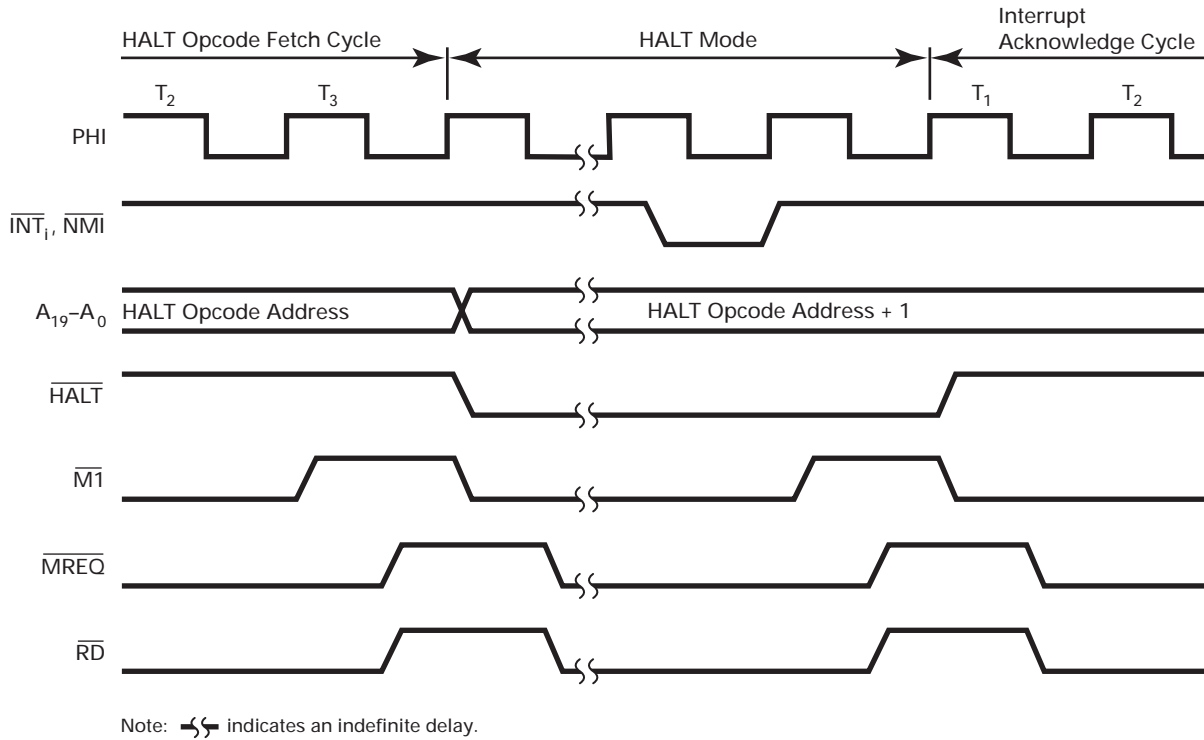
Figure 13. HALT Timing

SLEEP Mode. This mode is entered by keeping the IOSTOP bit (ICR5) and bits 3 and 6 of the CPU Control Register (CCR3, CCR6) all zero and executing the SLP instruction. The oscillator and PHI output continue operating, but are blocked from the CPU core and DMA channels to reduce power consumption. DRAM refresh stops, but interrupts and granting to an external Master can occur. Except when the bus is granted to an external Master, A19–0 and all control signals except $\overline{HALT}$ are maintained High. $\overline{HALT}$ is Low. I/O operations continue as before the SLP instruction, except for the DMA channels.

The Z8S180/Z8L180 leaves SLEEP mode in response to a Low on $\overline{RESET}$, an interrupt request from an on-chip source,

an external request on $\overline{NMI}$, or an external request on $\overline{INT0}$, $\overline{INT1}$, or $\overline{INT2}$.

If an interrupt source is individually disabled, it cannot bring the Z8S180/Z8L180 out of SLEEP mode. If an interrupt source is individually enabled, and the IEF bit is 1 so that interrupts are globally enabled (by an EI instruction), the highest priority active interrupt occurs with the return address being the instruction after the SLP instruction. If an interrupt source is individually enabled, but the IEF bit is 0 so that interrupts are globally disabled (by a DI instruction), the Z8S180/Z8L180 leaves SLEEP mode by simply executing the following instruction(s).

This condition provides a technique for synchronization with high-speed external events without incurring the latency imposed by an interrupt-response sequence. Figure 14 depicts the timing for exiting SLEEP mode due to an interrupt request.

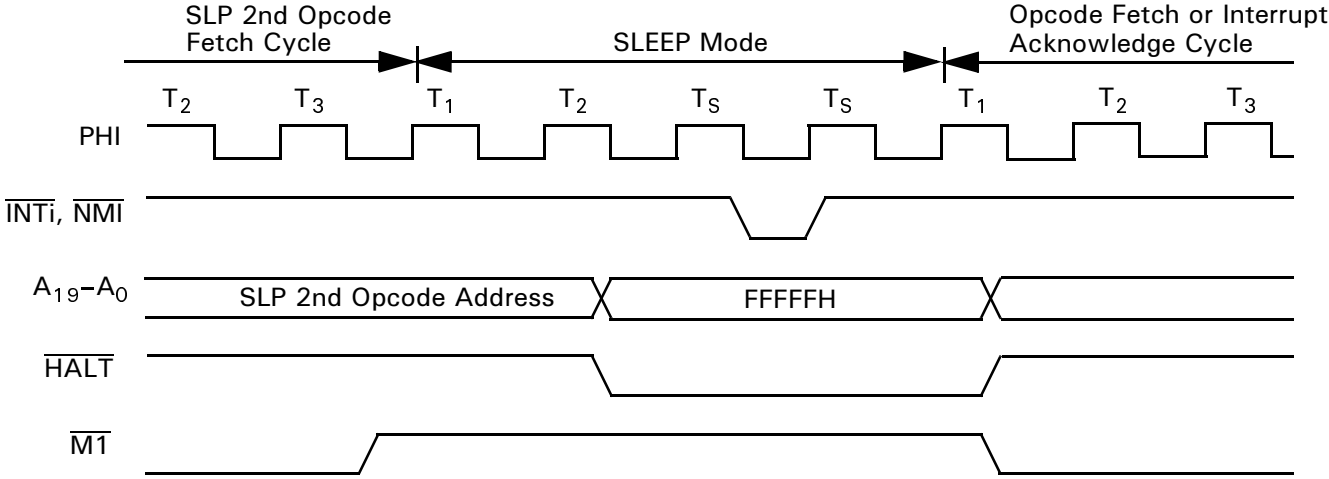**Note:** The Z8S180/Z8L180 takes about 1.5 clock ticks to restart.

Figure 14. SLEEP Timing

IOSTOP Mode. IOSTOP mode is entered by setting the IOSTOP bit of the I/O Control Register (ICR) to 1. In this case, on-chip I/O (ASCI, CSI/O, PRT) stops operating. However, the CPU continues to operate. Recovery from IOSTOP mode is performed by resetting the IOSTOP bit in ICR to 0.

SYSTEM STOP Mode. SYSTEM STOP mode is the combination of SLEEP and IOSTOP modes. SYSTEM STOP mode is entered by setting the IOSTOP bit in ICR to 1 followed by execution of the SLP instruction. In this mode, on-chip I/O and CPU stop operating, reducing power consumption, but the PHI output continues to operate. Recovery from SYSTEM STOP mode is the same as recovery from SLEEP mode except that internal I/O sources (disabled by IOSTOP) cannot generate a recovery interrupt.

IDLE Mode. Software puts the Z8S180/Z8L180 into this mode by performing the following actions:

• Set the IOSTOP bit (ICR5) to 1

• Set CCR6 to 0

• Set CCR3 to 1

• Execute the SLP instruction

The oscillator keeps operating but its output is blocked to all circuitry including the PHI pin. DRAM refresh and all internal devices stop, but external interrupts can occur. Bus granting to external Masters can occur if the BREST bit in the CPU control Register (CCR5) was set to 1 before IDLE mode was entered.

The Z8S180/Z8L180 leaves IDLE mode in response to a Low on $\overline{RESET}$, an external interrupt request on $\overline{NMI}$, or an external interrupt request on $\overline{INT0}$, $\overline{INT1}$ or $\overline{INT2}$ that is enabled in the INT/TRAP Control Register. As previously described for SLEEP mode, when the Z8S180/Z8L180 leaves IDLE mode due to an $\overline{NMI}$, or due to an enabled external interrupt request when the $\overline{IEF}$ flag is 1 due to an EI instruction, the device starts by performing the interrupt with the return address of the instruction after the SLP instruction.

If an external interrupt enables the INT/TRAP control register while the IEF1 bit is 0, Z8S180/Z8L180 leaves IDLE mode; specifically, the processor restarts by executing the instructions following the SLP instruction.

Figure 15 indicates the timing for exiting IDLE mode due to an interrupt request.

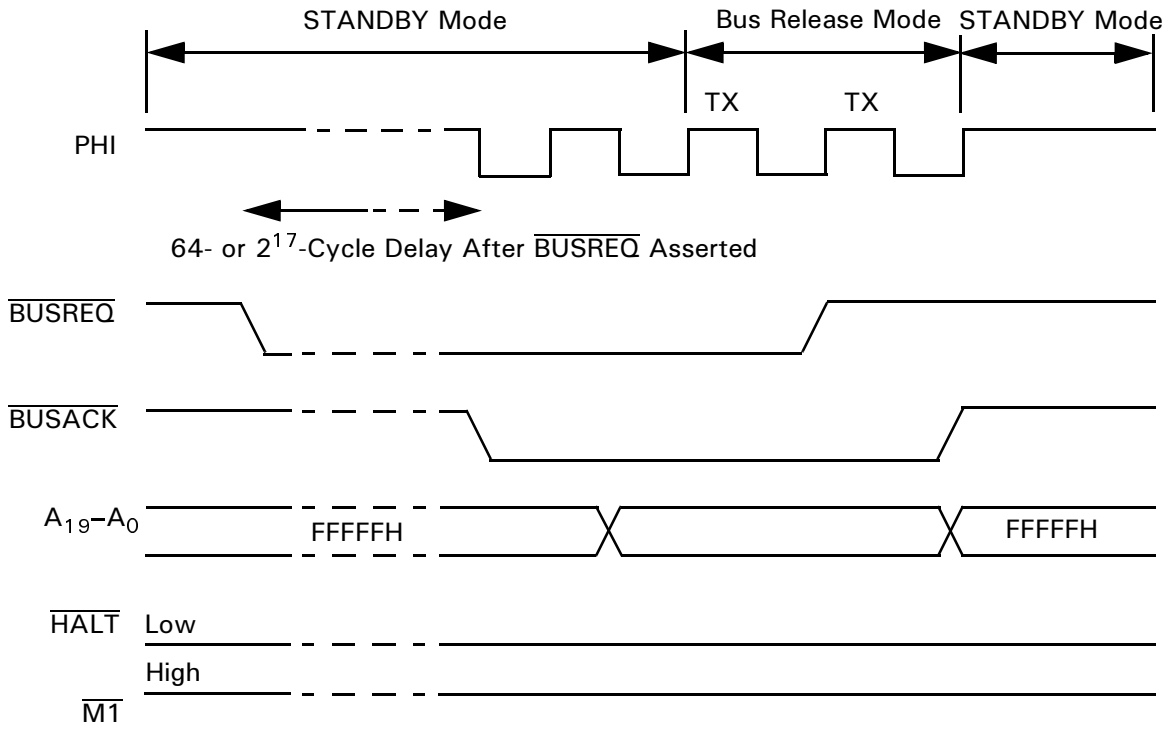**Note:** The Z8S180/Z8L180 takes about 9.5 clocks to restart.

Figure 18. Bus Granting to External Master During STANDBY Mode

AC CHARACTERISTICS—Z8S180

Table 8. Z8S180 AC Characteristics
V_{DD} = 5V ± 10% or V_{DD} = 3.3V ± 10%; 33-MHz Characteristics Apply Only to 5V Operation

Number	Symbol	Item	Z8S180—20 MHz Min	Max	Z8S180—33 MHz Min	Max	Unit
1	t_{CYC}	Clock Cycle Time	50	DC	30	DC	ns
2	t_{CHW}	Clock "H" Pulse Width	15	—	10	—	ns
3	t_{CLW}	Clock "L" Pulse Width	15	—	10	—	ns
4	t_{CF}	Clock Fall Time	—	10	—	5	ns
5	t_{CR}	Clock Rise Time	—	10	—	5	ns
6	t_{AD}	PHI Rise to Address Valid Delay	—	30	—	15	ns
7	t_{AS}	Address Valid to $\overline{MREQ}$ Fall or $\overline{IORQ}$ Fall)	5	—	5	—	ns
8	t_{MED1}	PHI Fall to $\overline{MREQ}$ Fall Delay	—	25	—	15	ns
9	t_{RDD1}	PHI Fall to $\overline{RD}$ Fall Delay $\overline{IOC}$ = 1	—	25	—	15	ns
		PHI Rise to $\overline{RD}$ Rise Delay $\overline{IOC}$ = 0	—	25	—	15	
10	t_{M1D1}	PHI Rise to $\overline{M1}$ Fall Delay	—	35	—	15	ns
11	t_{AH}	Address Hold Time from $\overline{MREQ}$, $\overline{IOREQ}$, $\overline{RD}$, $\overline{WR}$ High	5	—	5	—	ns
12	t_{MED2}	PHI Fall to $\overline{MREQ}$ Rise Delay	—	25	—	15	ns
13	t_{RDD2}	PHI Fall to $\overline{RD}$ Rise Delay	—	25	—	15	ns
14	t_{M1D2}	PHI Rise to $\overline{M1}$ Rise Delay	—	40	—	15	ns
15	t_{DRS}	Data Read Set-up Time	10	—	5	—	ns
16	t_{DRH}	Data Read Hold Time	0	—	0	—	ns
17	t_{STD1}	PHI Fall to ST Fall Delay	—	30	—	15	ns
18	t_{STD2}	PHI Fall to ST Rise Delay	—	30	—	15	ns
19	t_{WS}	$\overline{WAIT}$ Set-up Time to PHI Fall	15	—	10	—	ns
20	t_{WH}	$\overline{WAIT}$ Hold Time from PHI Fall	10	—	5	—	ns
21	t_{WDZ}	PHI Rise to Data Float Delay	—	35	—	20	ns
22	t_{WRD1}	PHI Rise to $\overline{WR}$ Fall Delay	—	25	—	15	ns
23	t_{WDD}	PHI Fall to Write Data Delay Time	—	25	—	15	ns
24	t_{WDS}	Write Data Set-up Time to $\overline{WR}$ Fall	10	—	10	—	ns
25	t_{WRD2}	PHI Fall to $\overline{WR}$ Rise Delay	—	25	—	15	ns
26	t_{WRP}	$\overline{WR}$ Pulse Width (Memory Write Cycle)	80	—	45	—	ns
26a		$\overline{WR}$ Pulse Width (I/O Write Cycle)	150	—	70	—	ns
27	t_{WDH}	Write Data Hold Time from $\overline{WR}$ Rise	10	—	5	—	ns
28	t_{IOD1}	PHI Fall to $\overline{IORQ}$ Fall Delay $\overline{IOC}$ = 1	—	25	—	15	ns
		PHI Rise to $\overline{IORQ}$ Fall Delay $\overline{IOC}$ = 0	—	25	—	15	
29	t_{IOD2}	PHI Fall to $\overline{IORQ}$ Rise Delay	—	25	—	15	ns
30	t_{IOD3}	$\overline{M1}$ Fall to $\overline{IORQ}$ Fall Delay	125	—	80	—	ns
31	t_{INTS}	$\overline{INT}$ Set-up Time to PHI Fall	20	—	15	—	ns

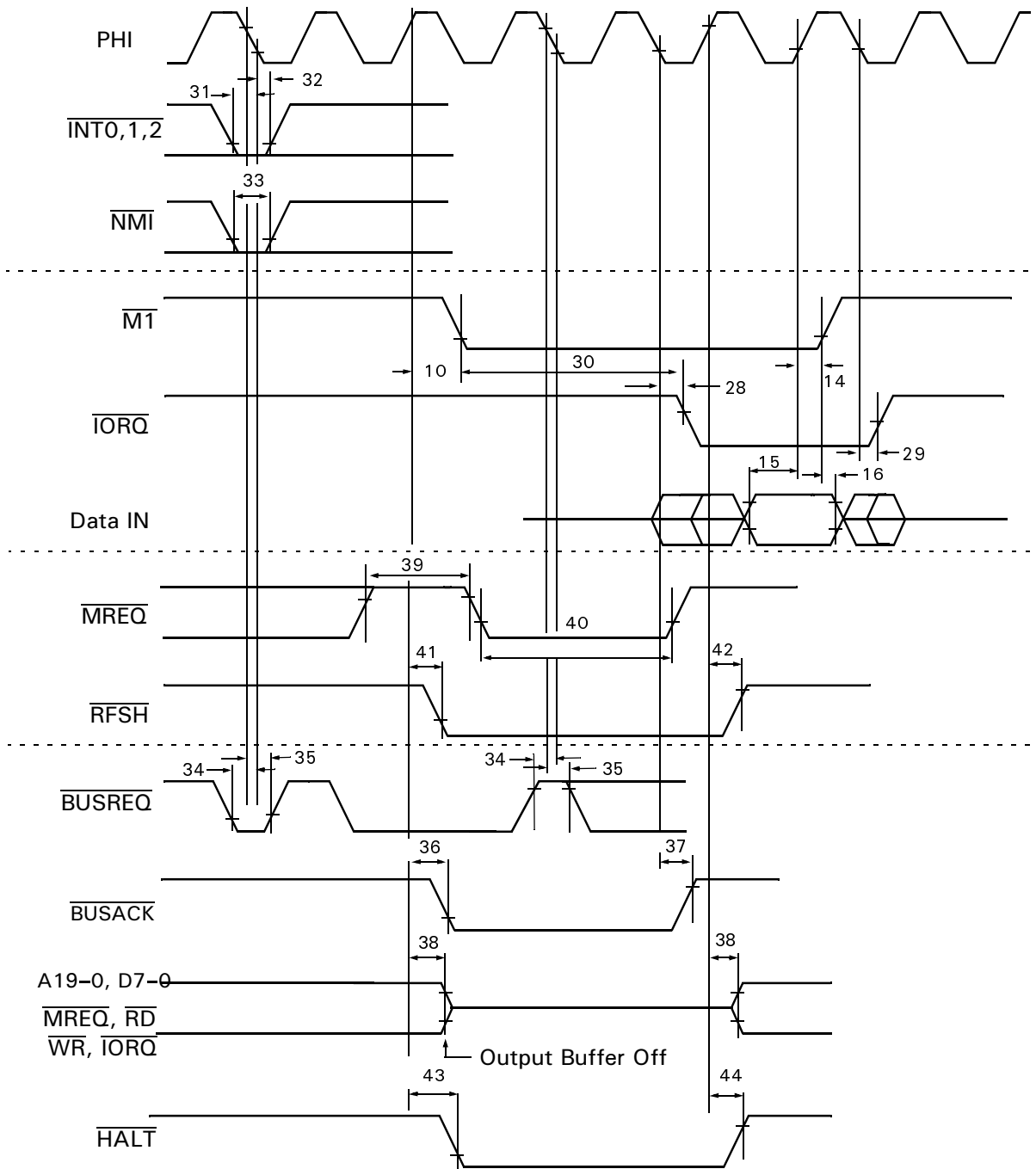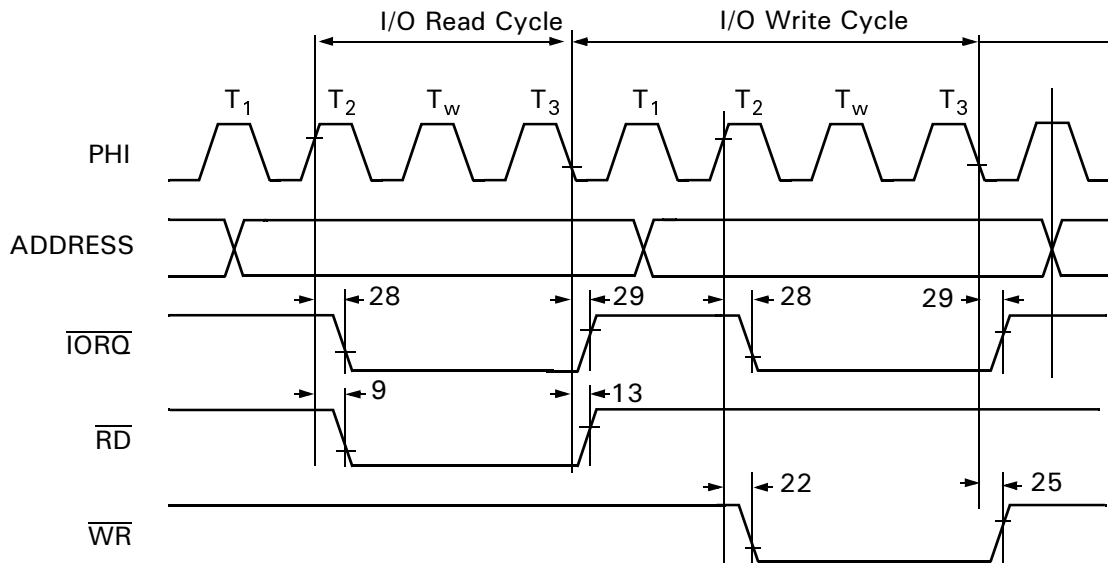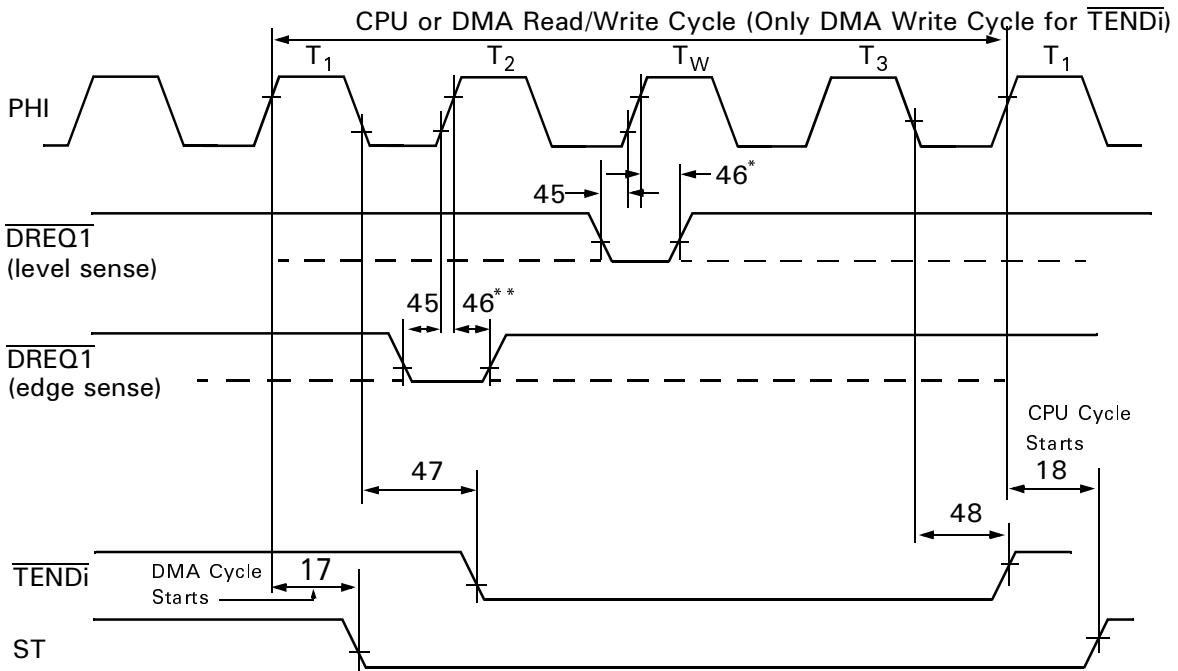**Figure 21. CPU Timing**
(INT0 Acknowledge Cycle, Refresh Cycle, BUS RELEASE Mode,
HALT Mode, SLEEP Mode, SYSTEM STOP Mode)
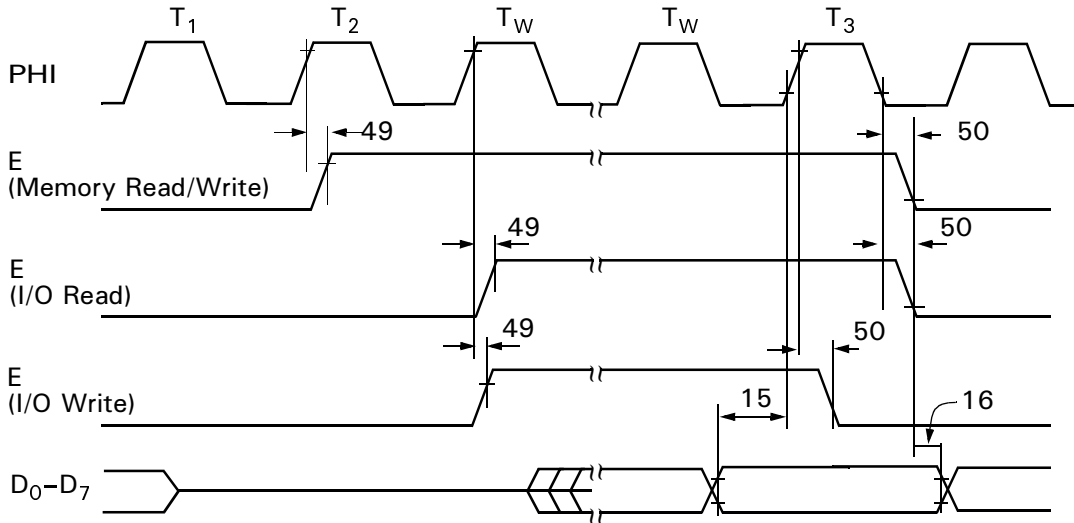
TIMING DIAGRAMS (Continued)

Figure 22. CPU Timing ($\overline{\text{IOC}}$ = 0)
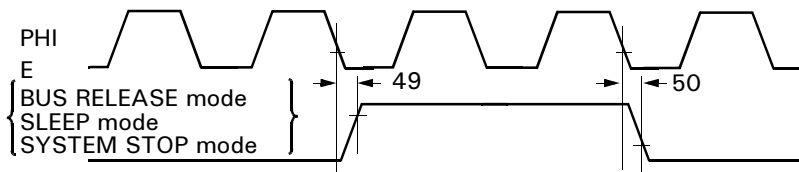**(I/O Read Cycle, I/O Write Cycle)**

Notes:
   *T_{DRQS} and T_{DRQH} are specified for the rising edge of the clock followed by T_3.
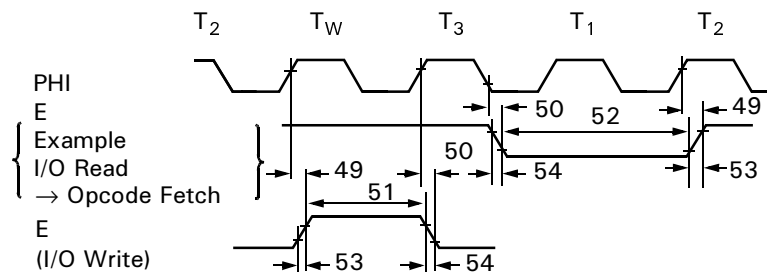   **T_{DRQS} and T_{DRQH} are specified for the rising edge of the clock.

Figure 23. DMA Control Signals

P R E L I M I N A R Y

Figure 24. E Clock Timing
(Memory Read/Write Cycle, I/O Read/Write Cycle)

Figure 25. E Clock Timing
(BUS RELEASE Mode, SLEEP Mode, SYSTEM STOP Mode)

Figure 26. E Clock Timing
(Minimum Timing Example of P_{WEL} and P_{WEH})

ASCI CHANNEL CONTROL REGISTER B

ASCI Control Register B 0 (CNTLB0: I/O Address = 02H)
ASCI Control Register B 1 (CNTLB1: I/O Address = 03H)

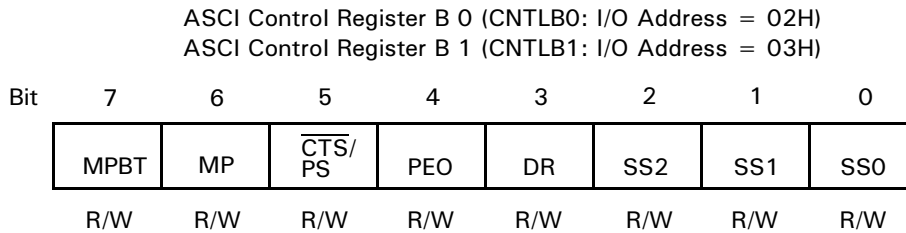| Bit	7	6	5	4	3	2	1	0
	MPBT	MP	$\overline{\text{CTS}}$/PS	PEO	DR	SS2	SS1	SS0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 34. ASCI Channel Control Register B

MPBT: Multiprocessor Bit Transmit (Bit 7). When multi-processor communication format is selected (MP bit = 1), MPBT is used to specify the MPB data bit for transmission. If MPBT = 1, then MPB = 1 is transmitted. If MPBT = 0, then MPB = 0 is transmitted. The MPBT state is undefined during and after RESET.

MP: Multiprocessor Mode (Bit 6). When MP is set to 1, the data format is configured for multiprocessor mode based on MOD2 (number of data bits) and MOD0 (number of stop bits) in CNTLA. The format is as follows:

Start bit + 7 or 8 data bits + MPB bit + 1 or 2 stop bits

Multiprocessor (MP = 1) format offers no provision for parity. If MP = 0, the data format is based on MOD0, MOD1, MOD2, and may include parity. The MP bit is cleared to 0 during RESET.

$\overline{\text{CTS}}$/PS: Clear to Send/Prescale (Bit 5). When read, $\overline{\text{CTS}}$/PS reflects the state of the external $\overline{\text{CTS}}$ input. If the $\overline{\text{CTS}}$ input pin is High, $\overline{\text{CTS}}$/PS is read as 1.

Note: When the $\overline{\text{CTS}}$ input pin is High, the TDRE bit is inhibited (that is, held at 0).

For channel 1, the $\overline{\text{CTS}}$ input is multiplexed with RXS pin (Clocked Serial Receive Data). Thus, $\overline{\text{CTS}}$/PS is only valid when read if the channel 1 CTS1E bit = 1 and the $\overline{\text{CTS}}$ input pin function is selected. The READ data of $\overline{\text{CTS}}$/PS is not affected by $\overline{\text{RESET}}$.

If the SS2–0 bits in this register are not 111, and the BRG mode bit in the ASEXT register is 0, then writing to this bit sets the prescale (PS) control. Under those circumstances, a 0 indicates a divide-by-10 prescale function while a 1 indicates divide-by-30. The bit resets to 0.

PEO: Parity Even Odd (Bit 4). PEO selects oven or odd parity. PEO does not affect the enabling/disabling of parity (MOD1 bit of CNTLA). If PEO is cleared to 0, even parity is selected. If PEO is set to 1, odd parity is selected. PEO is cleared to 0 during RESET.

DR: Divide Ratio (Bit 3). If the X1 bit in the ASEXT register is 0, this bit specifies the divider used to obtain baud rate from the data sampling clock. If DR is reset to 0, divide-by-16 is used, while if DR is set to 1, divide-by-64 is used. DR is cleared to 0 during RESET.

SS2,1,0: Source/Speed Select 2,1,0 (Bits 2–0). First, if these bits are 111, as they are after a RESET, the CKA pin is used as a clock input, and is divided by 1, 16, or 64 depending on the DR bit and the X1 bit in the ASEXT register.

If these bits are not 111 and the BRG mode bit is ASEXT is 0, then these bits specify a power-of-two divider for the PHI clock as indicated in Table 10.

Setting or leaving these bits as 111 makes sense for a channel only when its CKA pin is selected for the CKA function. CKAO/CKS offers the CKAO function when bit 4 of the System Configuration Register is 0. $\overline{\text{DCD0}}$/CKA1 offers the CKA1 function when bit 0 of the Interrupt Edge register is 1.

Table 10. Divide Ratio

SS2	SS1	SS0	Divide Ratio
0	0	0	÷1
0	0	1	÷2
0	1	0	÷4
0	1	1	÷8
1	0	0	÷16
1	0	1	÷32
1	1	0	÷64
1	1	1	External Clock

CLOCK MULTIPLIER REGISTER

(Z180 MPU Address 1EH)

7	6	5	4	3	2	1	0
0	0	1	1	1	1	1	1

RESERVED

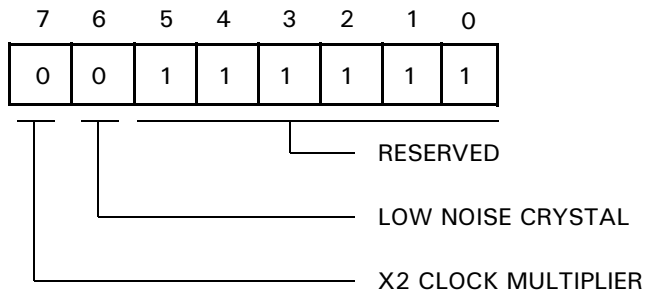LOW NOISE CRYSTAL

X2 CLOCK MULTIPLIER

Figure 54. Clock Multiplier Register

Bit 7. X2 Clock Multiplier Mode. When this bit is set to 1, the programmer can double the internal clock speed from the speed of the external clock. This feature only operates effectively with frequencies of 10–16 MHz (20–32 MHz internal). When this bit is set to 0, the Z8S180/Z8L180 device operates in normal mode. At power-up, this feature is disabled.

Bit 6. Low Noise Crystal Option. Setting this bit to 1 enables the low-noise option for the EXTAL and XTAL pins. This option reduces the gain in addition to reducing the output drive capability to 30% of its original drive capability. The Low Noise Crystal Option is recommended in the use of crystals for PCMCIA applications, where the crystal may be driven too hard by the oscillator. Setting this bit to 0 is selected for normal operation of the EXTAL and XTAL pins. The default for this bit is 0.

Note: Operating restrictions for device operation are listed below. If a low-noise option is required, and normal device operation is required, use the clock multiplier feature.

Table 13. Low Noise Option

Low Noise ADDR 1E, bit 6 = 1	Normal ADDR 1E, bit 6 = 0
20 MHz @ 4.5V, 100°C	33 MHz @ 4.5V, 100°C
10 MHz @ 3.0V, 100°C	20 MHz @ 3.0V, 100°C

DMA STATUS REGISTER

The DMA Status Register (DSTAT) is used to enable and disable DMA transfer and DMA termination interrupts.

DSTAT also indicates DMA transfer status, Completed or In Progress.

DMA Status Register

Mnemonic DSTAT
Address 30H

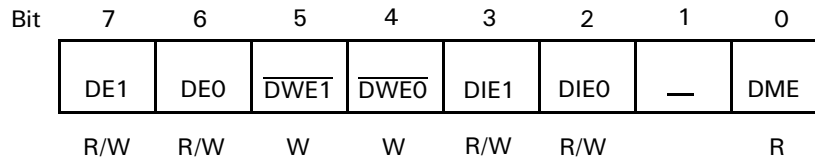| Bit	7	6	5	4	3	2	1	0
	DE1	DE0	$\overline{DWE1}$	$\overline{DWE0}$	DIE1	DIE0	—	DME
	R/W	R/W	W	W	R/W	R/W		R

Figure 71. DMA Status Register (DSTAT: I/O Address = 30H)

DE1: DMA Enable Channel 1 (Bit 7). When DE1 = 1 and DME = 1, channel 1 DMA is enabled. When a DMA transfer terminates (BCR1 = 0), DE1 is reset to 0 by the DMAC. When DE1 = 0 and the DMA interrupt is enabled (DIE1 = 1), a DMA interrupt request is made to the CPU.

To perform a software WRITE to DE1, $\overline{DWE1}$ should be written with a 0 during the same register WRITE access. Writing DE1 to 0 disables channel 1 DMA, but DMA is restartable. Writing DE1 to 1 enables channel 1 DMA and automatically sets DMA Main Enable (DME) to 1. DE1 is cleared to 0 during RESET.

DE0: DMA Enable Channel 0 (Bit 6). When DE0 = 1 and DME = 1, channel 0 DMA is enabled. When a DMA transfer terminates (BCR0 = 0), DE0 is reset to 0 by the DMAC. When DE0 = 0 and the DMA interrupt is enabled (DIE0 = 1), a DMA interrupt request is made to the CPU.

To perform a software WRITE to DE0, $\overline{DWE0}$ should be written with 0 during the same register WRITE access. Writing DE0 to 0 disables channel 0 DMA. Writing DE0 to 1 enables channel 0 DMA and automatically sets DMA Main Enable (DME) to 1. DE0 is cleared to 0 during RESET.

$\overline{DWE1}$: DE1 Bit Write Enable (Bit 5). When performing any software WRITE to DE1, this bit should be written with 0 during the same access. $\overline{DWE1}$ always reads as 1.

$\overline{DWE0}$: DE0 Bit Write Enable (Bit 4). When performing any software WRITE to DE0, this bit should be written with 0 during the same access. $\overline{DWE0}$ always reads as 1.

DIE1: DMA Interrupt Enable Channel 1 (Bit 3). When DIE0 is set to 1, the termination channel 1 DMA transfer (indicated when DE1 = 0) causes a CPU interrupt request to be generated. When DIE0 = 0, the channel 0 DMA termination interrupt is disabled. DIE0 is cleared to 0 during RESET.

DIE0: DMA Interrupt Enable Channel 0 (Bit 2). When DIE0 is set to 1, the termination channel 0 of DMA transfer (indicated when DE0 = 0) causes a CPU interrupt request to be generated. When DIE0 = 0, the channel 0 DMA termination interrupt is disabled. DIE0 is cleared to 0 during RESET.

DME: DMA Main Enable (Bit 0). A DMA operation is only enabled when its DE bit (DE0 for channel 0, DE1 for channel 1) and the DME bit is set to 1.

When $\overline{NMI}$ occurs, DME is reset to 0, thus disabling DMA activity during the $\overline{NMI}$ interrupt service routine. To restart DMA, DE– and/or DE1 should be written with a 1 (even if the contents are already 1). This condition automatically sets DME to 1, allowing DMA operations to continue.

Note: DME cannot be directly written. The bit is cleared to 0 by $\overline{NMI}$ or indirectly set to 1 by setting DE0 and/or DE1 to 1. DME is cleared to 0 during RESET.

DMA MODE REGISTER

The DMA Mode Register (DMODE) is used to set the addressing and transfer mode for channel 0.

DMA Mode Register

Mnemonic DMODE
Address 31H

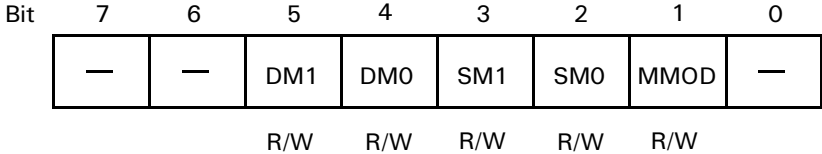| Bit	7	6	5	4	3	2	1	0
	—	—	DM1	DM0	SM1	SM0	MMOD	—
			R/W	R/W	R/W	R/W	R/W	

Figure 72. DMA Mode Register (DMODE: I/O Address = 31H)

DM1, DM0: Destination Mode Channel 0 (Bits 5,4). This mode specifies whether the destination for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred. DM1 and DM0 are cleared to 0 during RESET.

Table 14. Channel 0 Destination

DM1	DM0	Memory I/O	Memory Increment/Decrement
0	0	Memory	+ 1
0	1	Memory	−1
1	0	Memory	fixed
1	1	I/O	fixed

SM1, SM0: Source Mode Channel 0 (Bits 3, 2). This mode specifies whether the source for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred.

Table 15. Channel 0 Source

SM1	SM0	Memory I/O	Memory Increment/Decrement
0	0	Memory	+ 1
0	1	Memory	−1
1	0	Memory	fixed
1	1	I/O	fixed

Table 16 indicates all DMA transfer mode combinations of DM0, DM1, SM0, and SM1. Because I/O to/from I/O transfers are not implemented, 12 combinations are available.

Table 16. Transfer Mode Combinations

DM1	DM0	SM1	SM0	Transfer Mode	Address Increment/Decrement
0	0	0	0	Memory→Memory	SAR0 + 1, DAR0 + 1
0	0	0	1	Memory→Memory	SAR0−1, DAR0 + 1
0	0	1	0	Memory*→Memory	SAR0 fixed, DAR0 + 1
0	0	1	1	I/O→Memory	SAR0 fixed, DAR0 + 1
0	1	0	0	Memory→Memory	SAR0 + 1, DAR0−1
0	1	0	1	Memory→Memory	SAR0−1, DAR0−1
0	1	1	0	Memory*→Memory	SAR0 fixed, DAR0−1
0	1	1	1	I/O→Memory	SAR0 fixed, DAR0−1
1	0	0	0	Memory→Memory*	SAR0 + 1, DAR0 fixed
1	0	0	1	Memory→Memory*	SAR0−1, DAR0 fixed
1	0	1	0	Reserved	
1	0	1	1	Reserved	
1	1	0	0	Memory→I/O	SAR0 + 1, DAR0 fixed
1	1	0	1	Memory→I/O	SAR0−1, DAR0 fixed
1	1	1	0	Reserved	
1	1	1	1	Reserved	
Note: * Includes memory mapped I/O.					

MMOD: Memory Mode Channel 0 (Bit 1). When channel 0 is configured for memory to/from memory transfers there is no Request Handshake signal to control the transfer timing. Instead, two automatic transfer timing modes are selectable: burst (MMOD = 1) and cycle steal (MMOD = 0). For burst memory to/from memory transfers, the DMAC takes control of the bus continuously until the DMA transfer completes (as indicated by the byte count register = 0). In cycle steal mode, the CPU is provided a cycle for each DMA byte transfer cycle until the transfer is completed.

For channel 0 DMA with I/O source or destination, the selected Request signal times the transfer ignoring MMOD. MMOD is cleared to 0 during RESET.

DMA/WAIT CONTROL REGISTER

The DMA/WAIT Control Register (DCNTL) controls the insertion of wait states into DMAC (and CPU) accesses of memory or I/O. Also, the register defines the Request signal for each channel as level or edge sense. DCNTL also sets the DMA transfer mode for channel 1, which is limited to memory to/from I/O transfers.
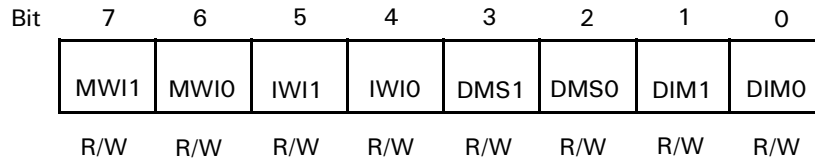
Bit	7	6	5	4	3	2	1	0
	MWI1	MWI0	IWI1	IWI0	DMS1	DMS0	DIM1	DIM0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 73. DMA/WAIT Control Register (DCNTL: I/O Address = 32H)

MWI1, MWI0: Memory Wait Insertion (Bits 7–6). This bit specifies the number of wait states introduced into CPU or DMAC memory access cycles. MWI1 and MWI0 are set to 1 during RESET.

MWI1	MWI0	Wait State
0	0	0
0	1	1
1	0	2
1	1	3

IWI1, IWI0: I/O Wait Insertion (Bits 5–4). This bit specifies the number of wait states introduced into CPU or DMAC I/O access cycles. IWI1 and IWI0 are set to 1 during RESET.

IWI1	IWI0	Wait State
0	0	1
0	1	2
1	0	3
1	1	4

Note: These wait states are added to the 3-clock I/O cycle that is used to access the on-chip I/O registers. It is equally valid to regard these as 0 to 3 wait states added to a 4-clock external I/O cycle.

DMS1, DMS0: DMA Request Sense (Bits 3–2). DMS1 and DMS0 specify the DMA request sense for channel 0 and channel 1 respectively. When reset to 0, the input is level sense. When set to 1, the input is edge sense. DMS1 and DMS0 are cleared to 0 during RESET.

DMSi	Sense
1	Edge Sense
0	Level Sense

Typically, for an input/source device, the associated DMS bit should be programmed as 0 for level sense. The device takes a relatively long time to update its Request signal after the DMA channel reads data (in the first of the two machine cycles involved in transferring a byte).

An output/destination device takes much less time to update its Request signal after the DMA channel starts a WRITE operation to it (the second machine cycle of the two cycles involved in transferring a byte). With zero-wait state I/O cycles, a device cannot update its request signal in the required time, so edge sensing must be used.

A one-wait-state I/O cycle also does not provide sufficient time for updating, so edge sensing is again required.

DIM1, DIM0: DMA Channel 1 I/O and Memory Mode (Bits 1–0). Specifies the source/destination and address modifier for channel 1 memory to/from I/O transfer modes. DIM1 and DIM0 are cleared to 0 during RESET.

Table 17. Channel 1 Transfer Mode

DIM1	DMI0	Transfer Mode	Address Increment/Decrement
0	0	Memory→I/O	MAR1 +1, IAR1 fixed
0	1	Memory→I/O	MAR1 −1, IAR1 fixed
1	0	I/O→Memory	IAR1 fixed, MAR1 +1
1	1	I/O→Memory	IAR1 fixed, MAR1 −1

CA3–CA0:CA (Bits 7–4). CA specifies the start (Low) address (on 4-KB boundaries) for Common Area 1. This condition also determines the most recent address of the Bank Area. All bits of CA are set to 1 during RESET.

BA3–BA0 (Bits 3–0). BA specifies the start (Low) address (on 4-KB boundaries) for the Bank Area. This condition also determines the most recent address of Common Area 0. All bits of BA are set to 1 during RESET.

OPERATION MODE CONTROL REGISTER

The Z8S180/Z8L180 is descended from two different ancestor processors, ZiLOG's original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR) can be programmed to select between certain differences between the Z80 and the 64180.
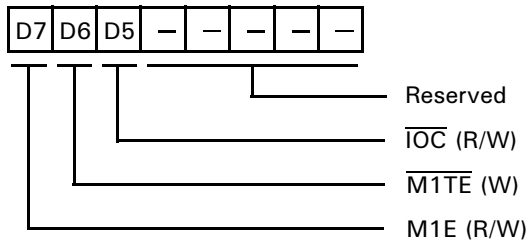
Operation Mode Control Register

Mnemonic OMCR
Address 3EH

Figure 81. Operating Control Register
(OMCR: I/O Address = 3EH)

M1E ($\overline{M1}$ Enable). This bit controls the $\overline{M1}$ output and is set to a 1 during reset.

When M1E = 1, the $\overline{M1}$ output is asserted Low during the opcode fetch cycle, the $\overline{INT0}$ acknowledge cycle, and the first machine cycle of the $\overline{NMI}$ acknowledge.

On the Z8S180/Z8L180, this choice makes the processor fetch one RETI instruction. When fetching a RETI from zero-wait-state memory, the processor uses three clock machine cycles that are not fully Z80-timing-compatible.

When M1E = 0, the processor does not drive $\overline{M1}$ Low during instruction fetch cycles. After fetching one RETI instruction with normal timing, the processor returns and refetches the instruction using Z80-compatible cycles that drive $\overline{M1}$ Low. This timing compatibility may be required by external Z80 peripherals to properly decode the RETI instruction.
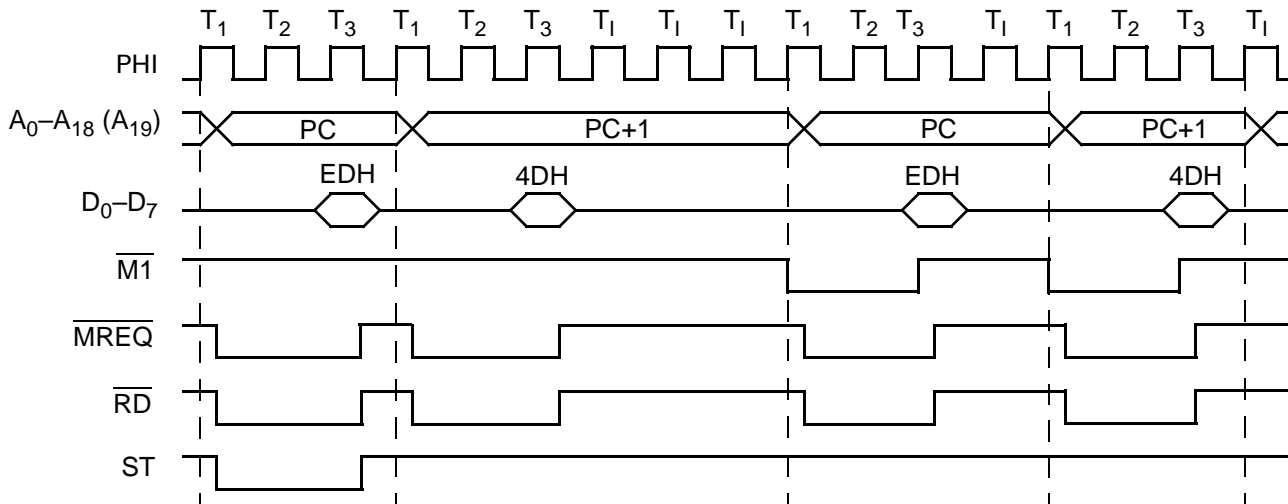

Figure 82. RETI Instruction Sequence with M1E = 0