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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z8S180 |
| Number of Cores/Bus Width | 1 Core, 8-Bit |
| Speed | 20MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 5.0V |
| Operating Temperature | -40°C ~ 100°C (TA) |
| Security Features | - |
| Package / Case | 68-LCC (J-Lead) |
| Supplier Device Package | 68-PLCC |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8s18020vec |

## PIN IDENTIFICATION (Continued)

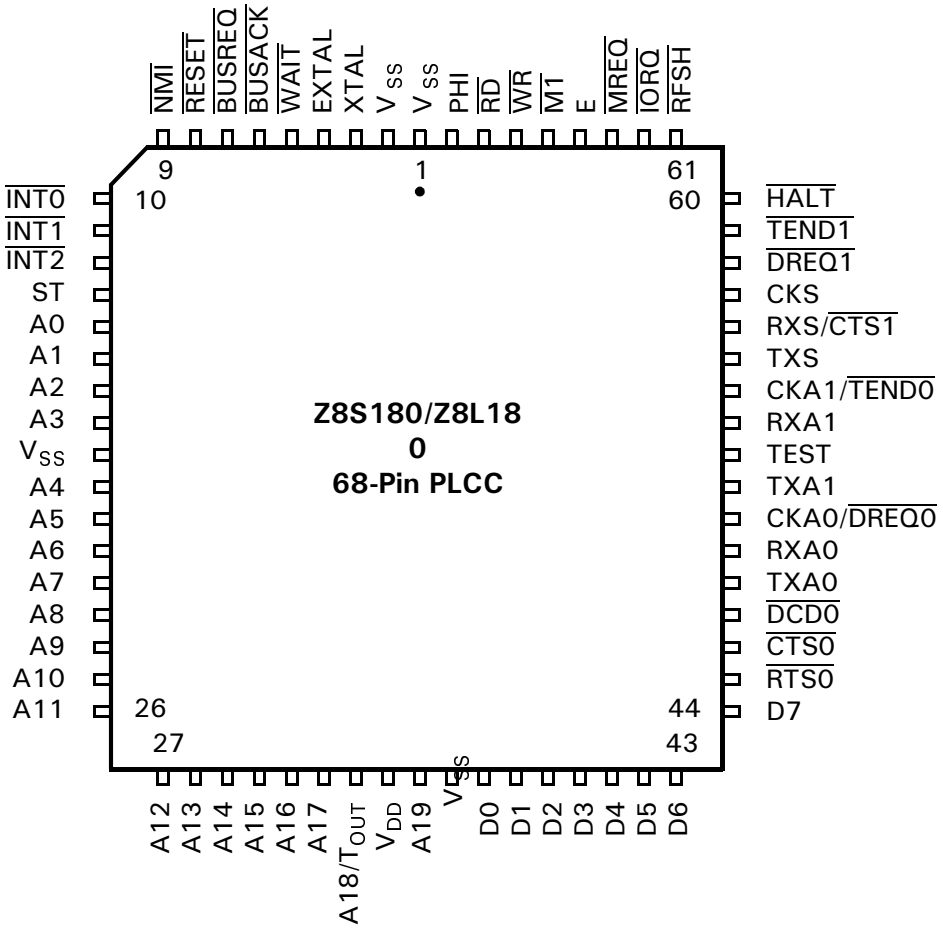


**Figure 3. Z8S180/Z8L180 68-Pin PLCC Pin Configuration**

**Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)**

| Pin Number and Package Type | | | | | Pin Status | | |
|---|---|---|---|---|---|---|---|
| QFP | PLCC | DIP | Default Function | Secondary Function | RESET | BUSACK | SLEEP |
| 39 | 41 | 38 | D4 | | 3T | 3T | 3T |
| 40 | 42 | 39 | D5 | | 3T | 3T | 3T |
| 41 | 43 | 40 | D6 | | 3T | 3T | 3T |
| 42 | | | NC | | | | |
| 43 | | | NC | | | | |
| 44 | 44 | 41 | D7 | | 3T | 3T | 3T |
| 45 | 45 | 42 | $\overline{RTS0}$ | | High | OUT | High |
| 46 | 46 | 43 | $\overline{CTS0}$ | | IN | OUT | IN |
| 47 | 47 | 44 | $\overline{DCD0}$ | | IN | IN | IN |
| 48 | 48 | 45 | TXA0 | | High | OUT | OUT |
| 49 | 49 | 46 | RXA0 | | IN | IN | IN |
| 50 | 50 | 47 | CKA0 | | 3T | I/O | I/O |
| | | | $\overline{DREQ0}$ | | N/A | IN | IN |
| 51 | | | NC | | | | |
| 52 | 51 | 48 | TXA1 | | High | OUT | OUT |
| 53 | 52 | | TEST | | | | |
| 54 | 53 | 49 | RXA1 | | IN | IN | IN |
| 55 | 54 | 50 | CKA1 | | 3T | I/O | I/O |
| | | | $\overline{TEND0}$ | | N/A | High | High |
| 56 | 55 | 51 | TXS | | High | OUT | OUT |
| 57 | 56 | 52 | RXS | | IN | IN | IN |
| | | | $\overline{CTS1}$ | | N/A | IN | IN |
| 58 | 57 | 53 | CKS | | 3T | I/O | I/O |
| 59 | 58 | 54 | $\overline{DREQ1}$ | | IN | 3T | IN |
| 60 | 59 | 55 | $\overline{TEND1}$ | | High | OUT | High |
| 61 | 60 | 56 | $\overline{HALT}$ | | High | High | Low |
| 62 | | | NC | | | | |
| 63 | | | NC | | | | |
| 64 | 61 | 57 | $\overline{RFSH}$ | | High | OUT | High |
| 65 | 62 | 58 | $\overline{IORQ}$ | | High | 3T | High |
| 66 | 63 | 59 | $\overline{MREQ}$ | | High | 3T | High |
| 67 | 64 | 60 | E | | Low | OUT | OUT |
| 68 | 65 | 61 | $\overline{M1}$ | | High | High | High |
| 69 | 66 | 62 | $\overline{WR}$ | | High | 3T | High |
| 70 | 67 | 63 | $\overline{RD}$ | | High | 3T | High |
| 71 | 68 | 64 | PHI | | OUT | OUT | OUT |
| 72 | 1 | 1 | $V_{SS}$ | | GND | GND | GND |
| 73 | 2 | | $V_{SS}$ | | GND | GND | GND |
| 74 | 3 | 2 | XTAL | | OUT | OUT | OUT |
| 75 | | | NC | | | | |

## PIN IDENTIFICATION (Continued)

**Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)**

| Pin Number and Package Type | | | | | Pin Status | | |
|---|---|---|---|---|---|---|---|
| QFP | PLCC | DIP | Default Function | Secondary Function | RESET | BUSACK | SLEEP |
| 76 | 4 | 3 | EXTAL | | IN | IN | IN |
| 77 | 5 | 4 | $\overline{\text{WAIT}}$ | | IN | IN | IN |
| 78 | 6 | 5 | $\overline{\text{BUSACK}}$ | | High | OUT | OUT |
| 79 | 7 | 6 | $\overline{\text{BUSREQ}}$ | | IN | IN | IN |
| 80 | 8 | 7 | $\overline{\text{RESET}}$ | | IN | IN | IN |

## PIN DESCRIPTIONS

**A0–A19**. Address Bus (Output, 3-state). A0–A19 form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 1 MB) and I/O data bus exchanges (up to 64 KB). The address bus enters a high–impedance state during reset and external bus acknowledge cycles. Address line A18 is multiplexed with the output of PRT channel 1 ($T_{OUT}$, selected as address output on reset), and address line A19 is not available in DIP versions of the Z8S180.

**$\overline{\text{BUSACK}}$**. Bus Acknowledge (Output, active Low). $\overline{\text{BUSACK}}$ indicates that the requesting device, the MPU address and data bus, and some control signals enter their high-impedance state.

**BUSREQ**. Bus Request (Input, active Low). This input is used by external devices (such as DMA controllers) to request access to the system bus. This request demands a higher priority than $\overline{\text{NMI}}$ and is always recognized at the end of the current machine cycle. This signal stops the CPU from executing further instructions, places addresses, data buses, and other control signals into the high-impedance state.

**CKA0, CKA1.** Asynchronous Clock 0 and 1 (bidirectional). When in output mode, these pins are the transmit and receive clock outputs from the ASCI baud rate generators. When in input mode, these pins serve as the external clock inputs for the ASCI baud rate generators. CKA0 is multiplexed with $\overline{\text{DREQ0}}$, and CKA1 is multiplexed with $\overline{\text{TEND0}}$.

**CKS.** Serial Clock (bidirectional). This line is the clock for the CSI/O channel.

**$\overline{\text{CTS0}}$–$\overline{\text{CTS1}}$.** Clear to send 0 and 1 (Inputs, active Low). These lines are modem control signals for the ASCI channels. $\overline{\text{CTS1}}$ is multiplexed with RXS.

**D0–D7.** Data Bus = (bidirectional, 3-state). D0–D7 constitute an 8-bit bidirectional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high-impedance state during reset and external bus acknowledge cycles.

**$\overline{\text{DCD0}}$.** Data Carrier Detect 0 (Input, active Low); a programmable modem control signal for ASCI channel 0.

**$\overline{\text{DREQ0}}$, $\overline{\text{DREQ1}}$**. DMA Request 0 and 1 (Input, active Low). $\overline{\text{DREQ}}$ is used to request a DMA transfer from one of the on-chip DMA channels. The DMA channels monitor these inputs to determine when an external device is ready for a READ or WRITE operation. These inputs can be programmed to be either level or edge sensed. $\overline{\text{DREQ0}}$ is multiplexed with CKA0.

**E.** Enable Clock (Output). This pin functions as a synchronous, machine-cycle clock output during bus transactions.

**EXTAL.** External Clock Crystal (Input). Crystal oscillator connections. An external clock can be input to the Z8S180/Z8L180 on this pin when a crystal is not used. This input is Schmitt triggered.

**$\overline{\text{HALT}}$.** HALT/SLEEP (Output, active Low). This output is asserted after the CPU executes either the HALT or SLEEP instruction and is waiting for either a nonmaskable or a maskable interrupt before operation can resume. It is also used with the $\overline{\text{M1}}$ and ST signals to decode the status of the CPU machine cycle.

**$\overline{\text{INT0}}$.** Maskable Interrupt Request 0 (Input, active Low). This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the $\overline{\text{NMI}}$ and $\overline{\text{BUSREQ}}$ signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$ signals become active.

**$\overline{\text{INT1}}$, $\overline{\text{INT2}}$.** Maskable Interrupt Request 1 and 2 (Inputs, active Low). This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the $\overline{\text{NMI}}$, $\overline{\text{BUSREQ}}$, and $\overline{\text{INT0}}$ signals are inactive. The CPU acknowledges these requests with an interrupt acknowledge cycle. Unlike the acknowledgment for $\overline{\text{INT0}}$, neither the $\overline{\text{M1}}$ or $\overline{\text{IORQ}}$ signals become active during this cycle.

**$\overline{\text{IORQ}}$.** I/O Request (Output, active Low, 3-state). $\overline{\text{IORQ}}$ indicates that the address bus contains a valid I/O address for an I/O READ or I/O WRITE operation. $\overline{\text{IORQ}}$ is also generated, along with $\overline{\text{M1}}$, during the acknowledgment of the $\overline{\text{INT0}}$ input signal to indicate that an interrupt response vector can be place onto the data bus. This signal is analogous to the $\overline{\text{IOE}}$ signal of the Z64180.

**$\overline{\text{M1}}$.** Machine Cycle 1 (Output, active Low). Together with $\overline{\text{MREQ}}$, $\overline{\text{M1}}$ indicates that the current cycle is the opcode-fetch cycle of instruction execution. Together with $\overline{\text{IORQ}}$, $\overline{\text{M1}}$ indicates that the current cycle is for interrupt acknowledgment. It is also used with the $\overline{\text{HALT}}$ and ST signal to decode the status of the CPU machine cycle. This signal is analogous to the $\overline{\text{LIR}}$ signal of the Z64180.

**$\overline{\text{MREQ}}$.** Memory Request (Output, active Low, 3-state). $\overline{\text{MREQ}}$ indicates that the address bus holds a valid address for a memory READ or memory WRITE operation. This signal is analogous to the $\overline{\text{ME}}$ signal of Z64180.

**$\overline{\text{NMI}}$.** Nonmaskable Interrupt (Input, negative edge triggered). $\overline{\text{NMI}}$ demands a higher priority than $\overline{\text{INT}}$ and is al-

**Table 4. Multiplexed Pin Descriptions**

| | |
|---|---|
| A18/TOUT | During RESET, this pin is initialized as A18. If either the TOC1 or the TOC0 bit of the Timer Control register (TCR) is set to 1, the $T_{OUT}$ function is selected. If TOC1 and TOC0 are cleared to 0, the A18 function is selected. |
| CKA0/$\overline{\text{DREQ0}}$ | During RESET, this pin is initialized as CKA0. If either DM1 or SM1 in the DMA Mode register (DMODE) is set to 1, the $\overline{\text{DREQ0}}$ function is selected. |
| CKA1/$\overline{\text{TEND0}}$ | During RESET, this pin is initialized as CKA1. If the CKA1D bit in ASCI control register ch1 (CNTLA1) is set to 1, the $\overline{\text{TEND0}}$ function is selected. If the CKA1D bit is set to 0, the CKA1 function is selected. |
| RXS/$\overline{\text{CTS1}}$ | During RESET, this pin is initialized as RXS. If the CTS1E bit in the ASCI status register ch1 (STAT1) is set to 1, the $\overline{\text{CTS1}}$ function is selected. If the CTS1E bit is set to 0, the RXS function is selected. |

## ARCHITECTURE

The Z180 combines a high-performance CPU core with a variety of system and I/O resources useful in a broad range of applications. The CPU core consists of five functional blocks: clock generator, bus state controller, Interrupt controller, memory management unit (MMU), and the central processing unit (CPU). The integrated I/O resources make up the remaining four functional blocks: direct memory access (DMA) control (2 channels), asynchronous serial communication interface (ASCI, 2 channels) programmable reload timers (PRT, 2 channels), and a clock serial I/O (CSI/O) channel.

**Clock Generator.** This logic generates a system clock from an external crystal or clock input. The external clock is divided by 2 or 1 and provides the timing for both internal and external devices.

**Bus State Controller.** This logic performs all of the status and bus-control activity associated with the CPU and some on-chip peripherals. Also includes wait-state timing, reset cycles, DRAM refresh, and DMA bus exchanges.

**Interrupt Controller.** This logic monitors and prioritizes the variety of internal and external interrupts and traps to provide the correct responses from the CPU. To maintain compatibility with the Z80 CPU, three different interrupts modes are supported.

**Memory Management Unit.** The MMU allows the user to map the memory used by the CPU (logically only 64KB) into the 1-MB addressing range supported by the Z8S180/Z8L180. The organization of the MMU object code maintains compatibility with the Z80 CPU, while offering access to an extended memory space. Accomplished by using an effective common-area/banked-area scheme.

**Central Processing Unit.** The CPU is microcoded to provide a core that is object-code compatible with the Z80 CPU. It also provides a superset of the Z80 instruction set, including 8-bit multiplication. The core is modified to allow many of the instructions to execute in fewer clock cycles.

**DMA Controller.** The DMA controller provides high-speed transfers between memory and I/O devices. Transfer operations supported are memory-to-memory, memory to/from I/O, and I/O-to-I/O. Transfer modes supported are request, burst, and cycle steal. DMA transfers can access the full 1-MB address range with a block length up to 64 KB, and can cross over 64K boundaries.

**Asynchronous Serial Communication Interface (ASCI).**

The ASCI logic provides two individual full-duplex UARTs. Each channel includes a programmable baud rate generator and modem control signals. The ASCI channels can also support a multiprocessor communication format as well as break detection and generation

**Programmable Reload Timers (PRT).** This logic consists of two separate channels, each containing a 16-bit counter (timer) and count reload register. The time base for the counters is derived from the system clock (divided by 20) before reaching the counter. PRT channel 1 provides an optional output to allow for waveform generation.

**ARCHITECTURE** (Continued)

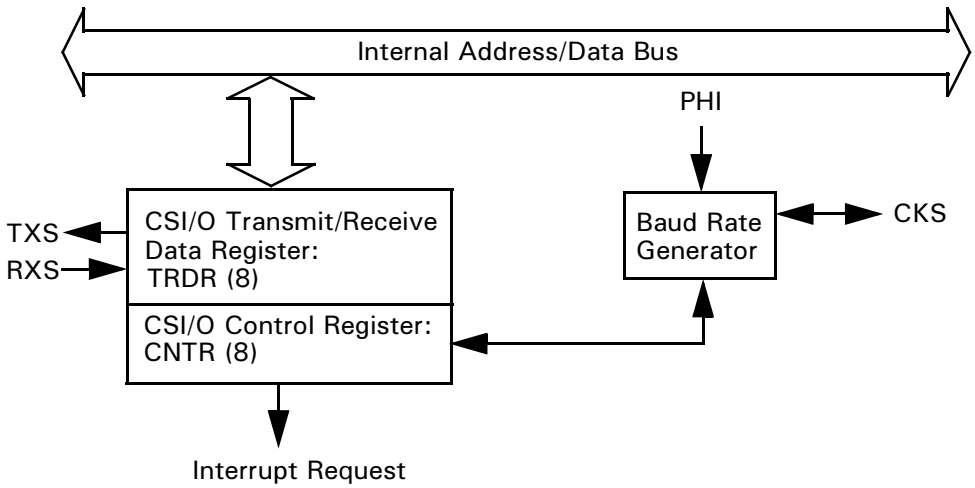


**Figure 7. CSI/O Block Diagram**

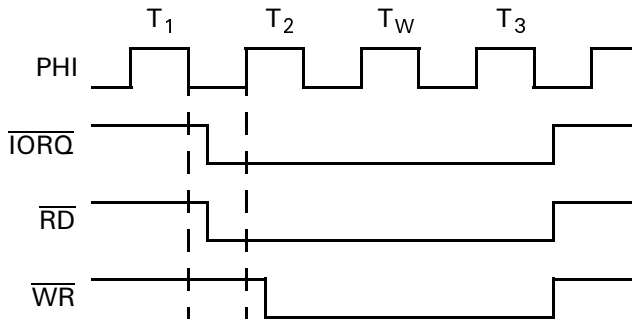


**Figure 11. I/O Read and Write Cycles with $\overline{IOC}$ = 1**

When $\overline{IOC}$ = 0, the timing of the $\overline{IORQ}$ and $\overline{RD}$ signals match the timing of the Z80. The $\overline{IORQ}$ and $\overline{RD}$ signals go active as a result of the rising edge of T2. (Figure 12.)

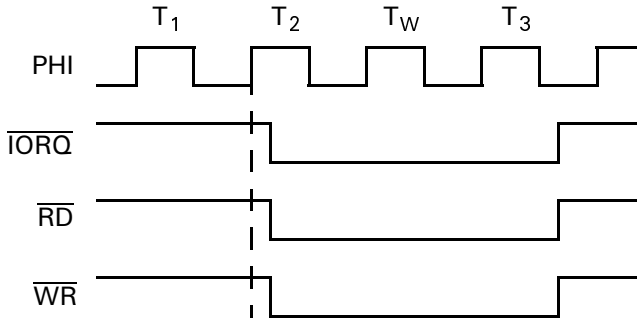


**Figure 12. I/O Read and Write Cycles with $\overline{IOC}$ = 0**

**HALT and Low-Power Operating Modes.** The Z8S180/Z8L180 can operate in seven modes with respect to activity and power consumption:

- Normal Operation
- HALT Mode
- IOSTOP Mode
- SLEEP Mode
- SYSTEM STOP Mode
- IDLE Mode
- STANDBY Mode (with or without QUICK RECOVERY)

**Normal Operation.** In this state, the Z8S180/Z8L180 processor is fetching and running a program. All enabled functions and portions of the device are active, and the $\overline{HALT}$ pin is High.

**HALT Mode.** This mode is entered by the HALT instruction. Thereafter, the Z8S180/Z8L180 processor continually fetches the following opcode but does not execute it and drives the $\overline{HALT}$, ST and $\overline{M1}$ pins all Low. The oscillator and PHI pin remain Active. Interrupts and bus granting to external Masters, and DRAM refresh can occur, and all on-chip I/O devices continue to operate including the DMA channels.

This condition provides a technique for synchronization with high-speed external events without incurring the latency imposed by an interrupt-response sequence. Figure 14 depicts the timing for exiting SLEEP mode due to an interrupt request.

**Note:** The Z8S180/Z8L180 takes about 1.5 clock ticks to restart.

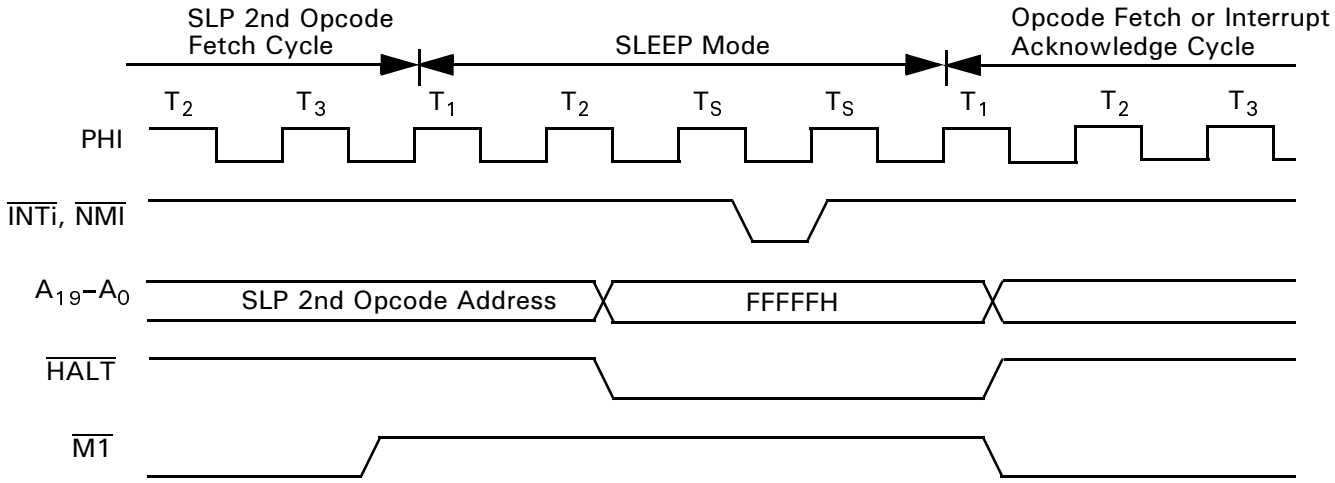


**Figure 14. SLEEP Timing**

**IOSTOP Mode.** IOSTOP mode is entered by setting the IOSTOP bit of the I/O Control Register (ICR) to 1. In this case, on-chip I/O (ASCI, CSI/O, PRT) stops operating. However, the CPU continues to operate. Recovery from IOSTOP mode is performed by resetting the IOSTOP bit in ICR to 0.

**SYSTEM STOP Mode.** SYSTEM STOP mode is the combination of SLEEP and IOSTOP modes. SYSTEM STOP mode is entered by setting the IOSTOP bit in ICR to 1 followed by execution of the SLP instruction. In this mode, on-chip I/O and CPU stop operating, reducing power consumption, but the PHI output continues to operate. Recovery from SYSTEM STOP mode is the same as recovery from SLEEP mode except that internal I/O sources (disabled by IOSTOP) cannot generate a recovery interrupt.

**IDLE Mode.** Software puts the Z8S180/Z8L180 into this mode by performing the following actions:

- Set the IOSTOP bit (ICR5) to 1
- Set CCR6 to 0
- Set CCR3 to 1
- Execute the SLP instruction

The oscillator keeps operating but its output is blocked to all circuitry including the PHI pin. DRAM refresh and all internal devices stop, but external interrupts can occur. Bus granting to external Masters can occur if the BREST bit in the CPU control Register (CCR5) was set to 1 before IDLE mode was entered.

The Z8S180/Z8L180 leaves IDLE mode in response to a Low on $\overline{\text{RESET}}$, an external interrupt request on $\overline{\text{NMI}}$, or an external interrupt request on $\overline{\text{INT0}}$, $\overline{\text{INT1}}$ or $\overline{\text{INT2}}$ that is enabled in the INT/TRAP Control Register. As previously described for SLEEP mode, when the Z8S180/Z8L180 leaves IDLE mode due to an $\overline{\text{NMI}}$, or due to an enabled external interrupt request when the $\overline{\text{IEF}}$ flag is 1 due to an EI instruction, the device starts by performing the interrupt with the return address of the instruction after the SLP instruction.

If an external interrupt enables the INT/TRAP control register while the IEF1 bit is 0, Z8S180/Z8L180 leaves IDLE mode; specifically, the processor restarts by executing the instructions following the SLP instruction.

Figure 15 indicates the timing for exiting IDLE mode due to an interrupt request.

**Note:** The Z8S180/Z8L180 takes about 9.5 clocks to restart.

ing the bus to an external Master during STANDBY mode, when the BREXT bit in the CPU Control Register (CCR5) is 1.

As described previously for SLEEP and IDLE modes, when the MPU leaves STANDBY mode due to $\overline{NMI}$ Low or an enabled $\overline{INT0}$–$\overline{INT2}$ Low when the IEF, flag is 1 due to an IE instruction, it starts by performing the interrupt with the return address being that of the instruction following the SLP instruction. If the Z8S180/Z8L180 leaves STANDBY mode due to an external interrupt request that's enabled in the INT/TRAP Control Register, but the IEF, bit is 0 due to a DI instruction, the processor restarts by executing the instruction(s) following the SLP instruction. If $\overline{INT0}$, or $\overline{INT1}$ or $\overline{INT2}$ goes inactive before the end of the clock stabilization delay, the Z8S180/Z8L180 stays in STANDBY mode.

Figure 17 indicates the timing for leaving STANDBY mode due to an interrupt request.

**Note:** The Z8S180/Z8L180 takes either 64 or $2^{17}$ (131,072) clocks to restart, depending on the CCR3 bit.

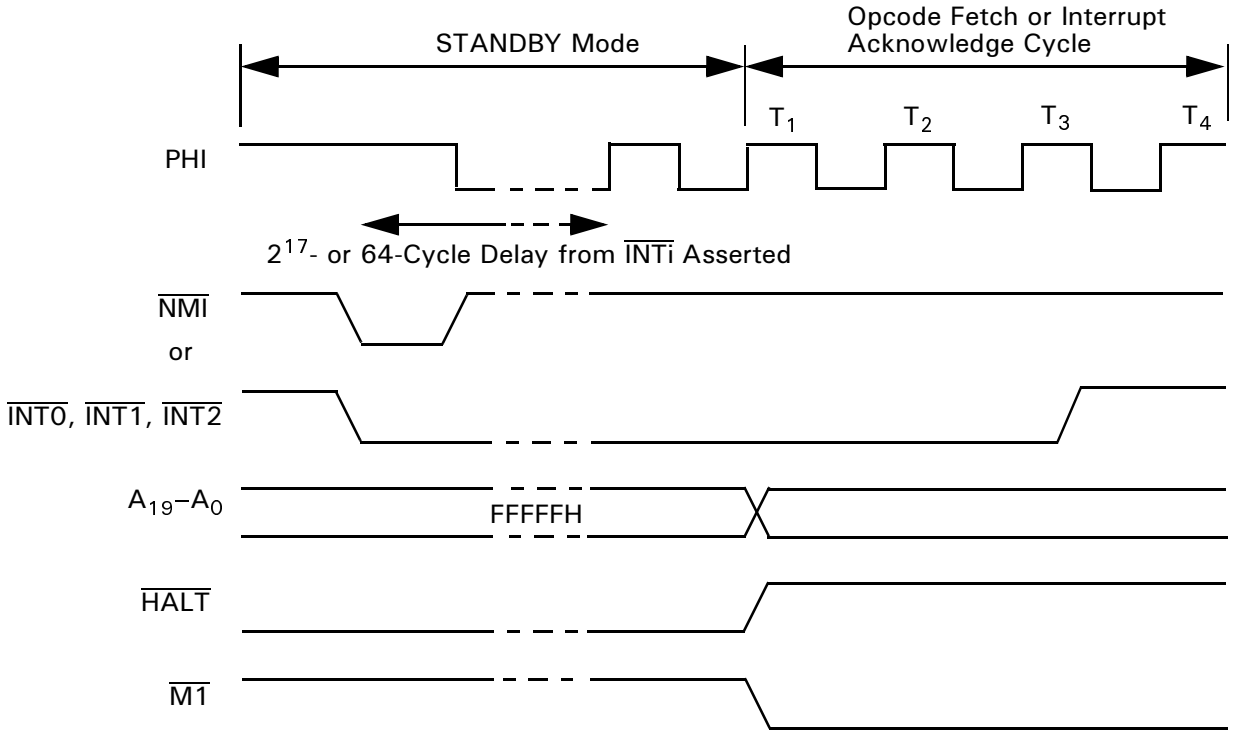


**Figure 17. Z8S180/Z8L180 STANDBY Mode Exit Due to External Interrupt**

While the Z8S180/Z8L180 is in STANDBY mode, it grants the bus to an external Master if the BREXT bit (CCR5) is 1. Figure 18 indicates the timing of this sequence. The device takes 64 or $2^{17}$ (131,072) clock cycles to grant the bus depending on the CCR3 bit. The latter (not the QUICK RECOVERY) case may be prohibitive for many demand-driven external Masters. If so, QUICK RECOVERY or IDLE mode can be used.

## STANDARD TEST CONDITIONS

The following standard test conditions apply to DC Characteristics, unless otherwise noted. All voltages are referenced to $V_{SS}$ (0V). Positive current flows into the referenced pin.

All AC parameters assume a load capacitance of 100 pF. Add a 10-ns delay for each 50-pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to $V_{OL}$ MAX or $V_{OL}$ MIN as indicated in Figures 20 through 30 (except for CLOCK, which is referenced to the 10% and 90% points). Ordering Information lists temperature ranges and product numbers. Find package drawings in Package Information.

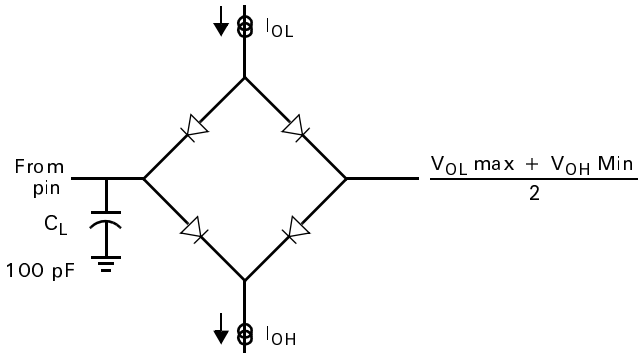


**Figure 19. AC Parameter Test Circuit**

## ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | –0.3 ~ +7.0 | V |
| Input Voltage | $V_{IN}$ | –0.3 ~ $V_{cc}$ +0.3 | V |
| Operating Temperature | $T_{OPR}$ | 0 ~ 70 | °C |
| Extended Temperature | $T_{EXT}$ | –40 ~ 85 | °C |
| Storage Temperature | $T_{STG}$ | –55 ~ +150 | °C |

**Note:** Permanent damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability.

**Table 8. Z8S180 AC Characteristics (Continued)**
**$V_{DD}$ = 5V ±10% or $V_{DD}$ = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation**

| | | | Z8S180—20 MHz | | Z8S180—33 MHz | | |
|---|---|---|---|---|---|---|---|
| **Number** | **Symbol** | **Item** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| 63 | $t_{REH}$ | $\overline{RESET}$ Hold Time from PHI Fall | 25 | — | 15 | — | ns |
| 64 | $t_{OSC}$ | Oscillator Stabilization Time | — | 20 | — | 20 | ns |
| 65 | $t_{EXR}$ | External Clock Rise Time (EXTAL) | — | 5 | — | 5 | ns |
| 66 | $t_{EXF}$ | External Clock Fall Time (EXTAL) | — | 5 | — | 5 | ns |
| 67 | $t_{RR}$ | $\overline{RESET}$ Rise Time | — | 50 | — | 50 | ms |
| 68 | $t_{RF}$ | $\overline{RESET}$ Fall Time | — | 50 | — | 50 | ms |
| 69 | $t_{IR}$ | Input Rise Time (except EXTAL, $\overline{RESET}$) | — | 50 | — | 50 | ns |
| 70 | $t_{IF}$ | Input Fall Time (except EXTAL, $\overline{RESET}$) | — | 50 | — | 50 | ns |

ASCI0 requests an interrupt when $\overline{DCD0}$ goes High. RIE is cleared to 0 by RESET.

**$\overline{DCD0}$: Data Carrier Detect (Bit 2 STAT0).** This bit is set to 1 when the pin is High. It is cleared to 0 on the first READ of STAT0 following the pin's transition from High to Low and during RESET. When bit 6 of the ASEXT0 register is 0 to select auto-enabling, and the pin is negated (High), the receiver is reset and its operation is inhibited.

**$\overline{CTS1E}$: Clear To Send (Bit 2 STAT1).** Channel 1 features an external $\overline{CTS1}$ input, which is multiplexed with the receive data pin RSX for the CSI/O. Setting this bit to 1 selects the CTS1 function; clearing the bit to 0 selects the RXS function.

**TDRE: Transmit Data Register Empty (Bit 1).** TDRE = 1 indicates that the TDR is empty and the next transmit data byte is written to TDR. After the byte is written to TDR, TDRE is cleared to 0 until the ASCI transfers the byte from TDR to the TSR and then TDRE is again set to 1. TDRE is set to 1 in IOSTOP mode and during RESET. On ASCI0, if the $\overline{CTS0}$ pin is auto-enabled in the ASEXT0 register and the pin is High, TDRE is reset to 0.

**TIE: Transmit Interrupt Enable (Bit 0).** TIE should be set to 1 to enable ASCI transmit interrupt requests. If TIE = 1, an interrupt is requested when TDRE = 1. TIE is cleared to 0 during RESET.

## ASCI TRANSMIT DATA REGISTERS

Register addresses 06H and 07H hold the ASCI transmit data for channel 0 and channel 1, respectively.

### ASCI Transmit Data Registers Channel 0

**Mnemonic TDR0**
**Address 06H**

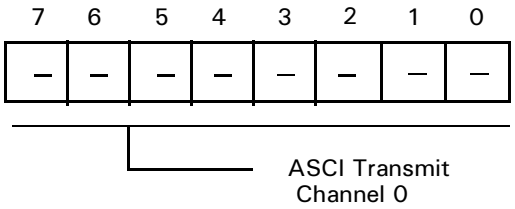


**Figure 36. ASCI Register**

### ASCI Transmit Data Registers Channel 1

**Mnemonic TDR1**
**Address 07H**

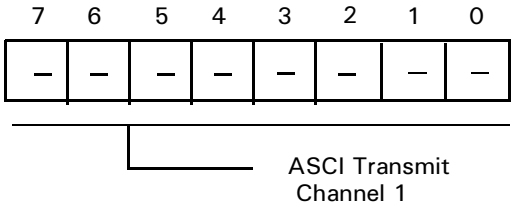


**Figure 37. ASCI Register**

never both set to 1 at the same time. TE is cleared to 0 during RESET and IOSTOP mode.

**SS2, 1, 0: Speed Select 2, 1, 0 (Bits 2–0).** SS2, SS1 and SS0 select the CSI/O transmit/receive clock source and speed. SS2, SS1 and SS0 are all set to 1 during $\overline{\text{RESET}}$. Table 11 indicates CSI/O Baud Rate Selection.

**Table 11. CSI/O Baud Rate Selection**

| SS2 | SS1 | SS0 | Divide Ratio |
|---|---|---|---|
| 0 | 0 | 0 | ÷20 |
| 0 | 0 | 1 | ÷40 |
| 0 | 1 | 0 | ÷80 |
| 0 | 1 | 1 | ÷160 |
| 1 | 0 | 0 | ÷320 |
| 1 | 0 | 1 | ÷640 |
| 1 | 1 | 0 | ÷1280 |
| 1 | 1 | 1 | External Clock Input (Less Than ÷20) |

After $\overline{\text{RESET}}$, the CKS pin is configured as an external clock input (SS2, SS1, SS0 = 1). Changing these values causes CKS to become an output pin and the selected clock is output when transmit or receive operations are enabled.

## CSI/O Transmit/Receive Data Register

**Mnemonic TRDR**
**Address 0BH**

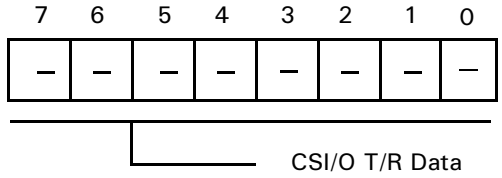


**Figure 41. CSI/O Transmit/Receive Data Register**

## Timer Data Register Channel 0 Low

**Mnemonic TMDR0L**
**Address 0CH**

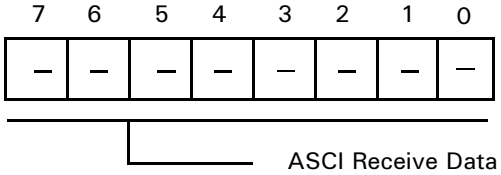


**Figure 42. Timer Register Channel 0 Low**

## Timer Data Register Channel 0H

**Mnemonic TMDR0H**
**Address 0DH**

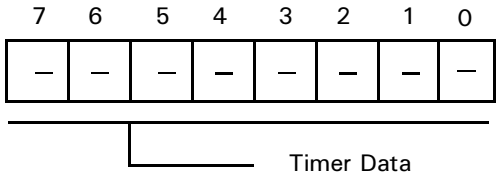


**Figure 43. Timer Data Register Channel 0 High**

## Timer Reload Register Channel 0 Low

**Mnemonic RLDR0L**
**Address 0EH**

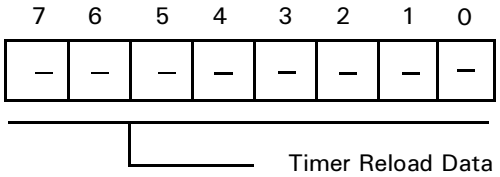


**Figure 44. Timer Reload Register Low**

## Timer Reload Register Channel 0 High

**Mnemonic RLDR0H**
**Address 0FH**

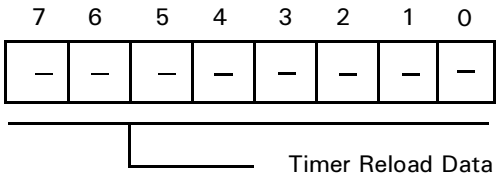


**Figure 45. Timer Reload Register Channel 0 High**

## TIMER CONTROL REGISTER

The Timer Control Register (TCR) monitors both channels (PRT0, PRT1) TMDR status. It also controls the enabling and disabling of down-counting and interrupts, and controls the output pin A18/$T_{OUT}$ for PRT1.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | TIF1 | TIF0 | TIE1 | TIE0 | TOC1 | TOC0 | TDE1 | TDE0 |
| | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

**Figure 46. Timer Control Register (TCR: I/O Address = 10H)**

**TIF1: Timer Interrupt Flag 1 (Bit 7) .** When TMDR1 decrements to 0, TIF1 is set to 1. This condition generates an interrupt request if enabled by TIE1 = 1. TIF1 is reset to 0 when TCR is read and the higher or lower byte of TMDR1 is read. During RESET, TIF1 is cleared to 0.

**TIF0: Timer Interrupt Flag 0 (Bit 6).** When TMDR0 decrements to 0, TIF0 is set to 1. This condition generates an interrupt request if enabled by TIE0 = 1. TIF0 is reset to 0 when TCR is read and the higher or lower byte of TMDR0 is read. During RESET, TIF0 is cleared to 0.

**TIE1: Timer Interrupt Enable 1 (Bit 5).** When TIE0 is set to 1, TIF1 = 1 generates a CPU interrupt request. When TIE0 is reset to 0, the interrupt request is inhibited. During RESET, TIE0 is cleared to 0.

**TOC1, 0: Timer Output Control (Bits 3, 2).** TOC1 and TOC0 control the output of PRT1 using the multiplexed A18/$T_{OUT}$ pin as indicated in Table 12. During RESET, TOC1 and TOC0 are cleared to 0. If bit 3 of the IAR1B register is 1, the $T_{OUT}$ function is selected. By programming TOC1 and TOC0, the A18/$T_{OUT}$ pin can be forced High, Low, or toggled when TMDR1 decrements to 0.

**Table 12. Timer Output Control**

| TOC1 | TOC0 | Output | |
|---|---|---|---|
| 0 | 0 | Inhibited | The A18/$T_{OUT}$ pin is not affected by the PRT |
| 0 | 1 | Toggled | If bit 3 of IAR1B is 1, the A18/$T_{OUT}$ pin is toggled or set Low or High as indicated |
| 1 | 0 | 0 | |
| 1 | 1 | 1 | |

**TDE1, 0: Timer Down Count Enable (Bits 1, 0).** TDE1 and TDE0 enable and disable down-counting for TMDR1 and TMDR0, respectively. When TDEn (n = 0,1) is set to 1, down-counting is stopped and TMDRn is freely read or written. TDE1 and TDE0 are cleared to 0 during RESET and TMDRn does not decrement until TDEn is set to 1.

## DMA STATUS REGISTER

The DMA Status Register (DSTAT) is used to enable and disable DMA transfer and DMA termination interrupts. DSTAT also indicates DMA transfer status, Completed or In Progress.

### DMA Status Register

**Mnemonic DSTAT**
**Address 30H**

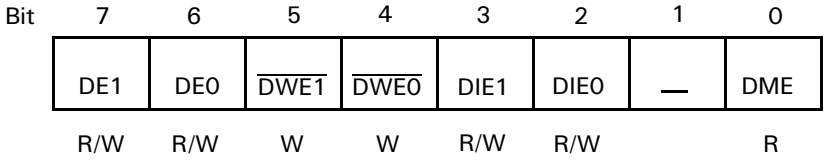


**Figure 71. DMA Status Register (DSTAT: I/O Address = 30H)**

**DE1: DMA Enable Channel 1 (Bit 7).** When DE1 = 1 and DME = 1, channel 1 DMA is enabled. When a DMA transfer terminates (BCR1 = 0), DE1 is reset to 0 by the DMAC. When DE1 = 0 and the DMA interrupt is enabled (DIE1 = 1), a DMA interrupt request is made to the CPU.

To perform a software WRITE to DE1, $\overline{\text{DWE1}}$ should be written with a 0 during the same register WRITE access. Writing DE1 to 0 disables channel 1 DMA, but DMA is restartable. Writing DE1 to 1 enables channel 1 DMA and automatically sets DMA Main Enable (DME) to 1. DE1 is cleared to 0 during RESET.

**DE0: DMA Enable Channel 0 (Bit 6).** When DE0 = 1 and DME = 1, channel 0 DMA is enabled. When a DMA transfer terminates (BCR0 = 0), DE0 is reset to 0 by the DMAC. When DE0 = 0 and the DMA interrupt is enabled (DIE0 = 1), a DMA interrupt request is made to the CPU.

To perform a software WRITE to DE0, $\overline{\text{DWE0}}$ should be written with 0 during the same register WRITE access. Writing DE0 to 0 disables channel 0 DMA. Writing DE0 to 1 enables channel 0 DMA and automatically sets DMA Main Enable (DME) to 1. DE0 is cleared to 0 during RESET.

**$\overline{\text{DWE1}}$: DE1 Bit Write Enable (Bit 5).** When performing any software WRITE to DE1, this bit should be written with 0 during the same access. $\overline{\text{DWE1}}$ always reads as 1.

**$\overline{\text{DWE0}}$: DE0 Bit Write Enable (Bit 4).** When performing any software WRITE to DE0, this bit should be written with 0 during the same access. $\overline{\text{DWE0}}$ always reads as 1.

**DIE1: DMA Interrupt Enable Channel 1 (Bit 3).** When DIE0 is set to 1, the termination channel 1 DMA transfer (indicated when DE1 = 0) causes a CPU interrupt request to be generated. When DIE0 = 0, the channel 0 DMA termination interrupt is disabled. DIE0 is cleared to 0 during RESET.

**DIE0: DMA Interrupt Enable Channel 0 (Bit 2).** When DIE0 is set to 1, the termination channel 0 of DMA transfer (indicated when DE0 = 0) causes a CPU interrupt request to be generated. When DIE0 = 0, the channel 0 DMA termination interrupt is disabled. DIE0 is cleared to 0 during RESET.

**DME: DMA Main Enable (Bit 0).** A DMA operation is only enabled when its DE bit (DE0 for channel 0, DE1 for channel 1) and the DME bit is set to 1.

When $\overline{\text{NMI}}$ occurs, DME is reset to 0, thus disabling DMA activity during the $\overline{\text{NMI}}$ interrupt service routine. To restart DMA, DE– and/or DE1 should be written with a 1 (even if the contents are already 1). This condition automatically sets DME to 1, allowing DMA operations to continue.

**Note:** DME cannot be directly written. The bit is cleared to 0 by $\overline{\text{NMI}}$ or indirectly set to 1 by setting DE0 and/or DE1 to 1. DME is cleared to 0 during RESET.

Table 16 indicates all DMA transfer mode combinations of DM0, DM1, SM0, and SM1. Because I/O to/from I/O transfers are not implemented, 12 combinations are available.

**Table 16. Transfer Mode Combinations**

| DM1 | DM0 | SM1 | SM0 | Transfer Mode | Address Increment/Decrement |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Memory→Memory | SAR0 + 1, DAR0 + 1 |
| 0 | 0 | 0 | 1 | Memory→Memory | SAR0–1, DAR0 + 1 |
| 0 | 0 | 1 | 0 | Memory*→Memory | SAR0 fixed, DAR0 + 1 |
| 0 | 0 | 1 | 1 | I/O→Memory | SAR0 fixed, DAR0 + 1 |
| 0 | 1 | 0 | 0 | Memory→Memory | SAR0 + 1, DAR0–1 |
| 0 | 1 | 0 | 1 | Memory→Memory | SAR0–1, DAR0–1 |
| 0 | 1 | 1 | 0 | Memory*→Memory | SAR0 fixed, DAR0–1 |
| 0 | 1 | 1 | 1 | I/O→Memory | SAR0 fixed, DAR0–1 |
| 1 | 0 | 0 | 0 | Memory→Memory* | SAR0 + 1, DAR0 fixed |
| 1 | 0 | 0 | 1 | Memory→Memory* | SAR0–1, DAR0 fixed |
| 1 | 0 | 1 | 0 | Reserved | |
| 1 | 0 | 1 | 1 | Reserved | |
| 1 | 1 | 0 | 0 | Memory→I/O | SAR0 + 1, DAR0 fixed |
| 1 | 1 | 0 | 1 | Memory→I/O | SAR0–1, DAR0 fixed |
| 1 | 1 | 1 | 0 | Reserved | |
| 1 | 1 | 1 | 1 | Reserved | |

**Note:** * Includes memory mapped I/O.

**MMOD: Memory Mode Channel 0 (Bit 1).** When channel 0 is configured for memory to/from memory transfers there is no Request Handshake signal to control the transfer timing. Instead, two automatic transfer timing modes are selectable: burst (MMOD = 1) and cycle steal (MMOD = 0). For burst memory to/from memory transfers, the DMAC takes control of the bus continuously until the DMA transfer completes (as indicated by the byte count register = 0). In cycle steal mode, the CPU is provided a cycle for each DMA byte transfer cycle until the transfer is completed.

For channel 0 DMA with I/O source or destination, the selected Request signal times the transfer ignoring MMOD. MMOD is cleared to 0 during RESET.

All TRAPs occur after fetching an undefined second opcode byte following one of the prefix opcodes (CBH, DDH, EDH, or FDH) or after fetching an undefined third opcode byte following one of the double-prefix opcodes (DDCBH or FDCBH).

The state of the Undefined Fetch Object (UFO) bit in ITC allows TRAP software to correctly *adjust* the stacked PC, depending on whether the second or third byte of the opcode generated the TRAP. If UFO = 0, the starting address of the invalid instruction is the stacked PC–1. If UFO = 1, the starting address of the invalid instruction is equal to the stacked PC–2.

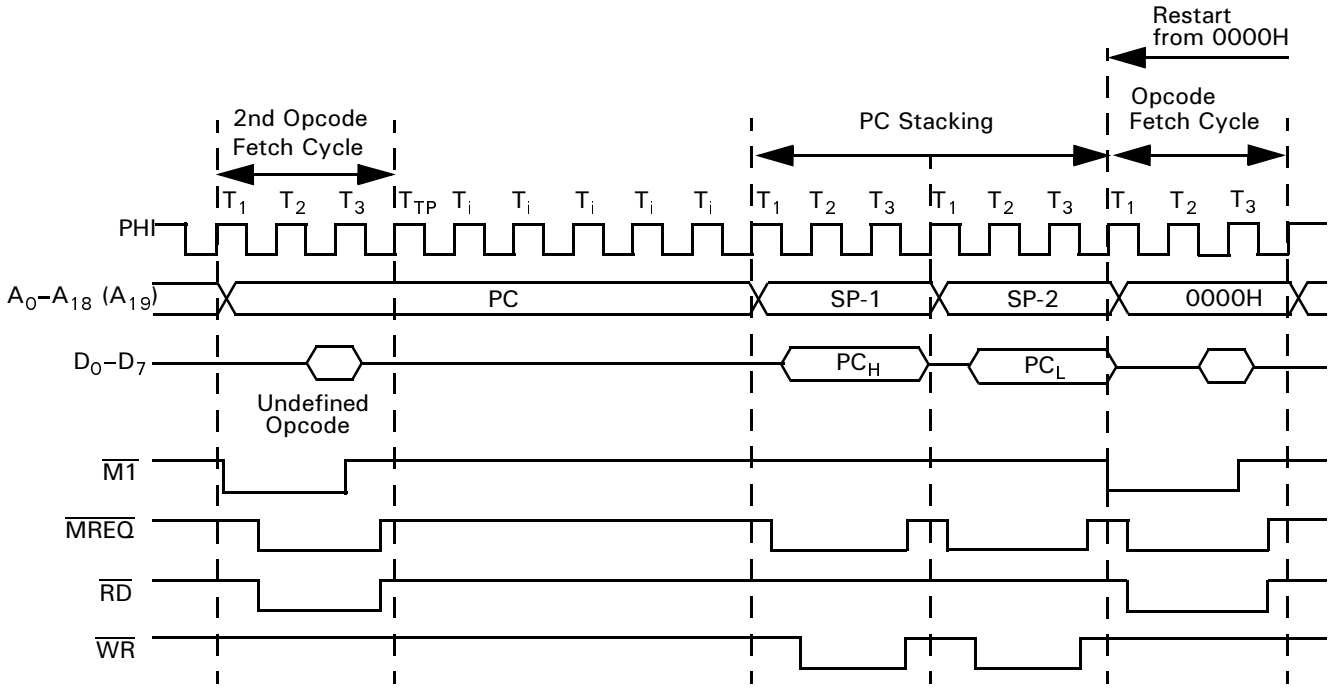


**Figure 75. TRAP Timing—2nd Opcode Undefined**

## REFRESH CONTROL REGISTER

**Mnemonic RCR**
**Address 36H**

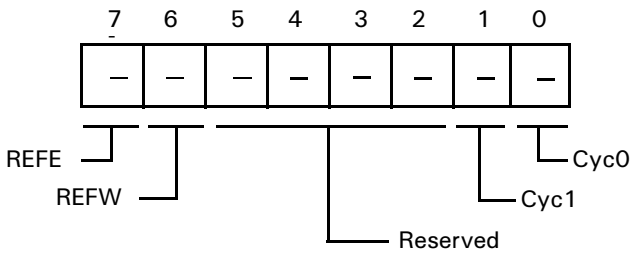


**Figure 77. Refresh Control Register (RCR: I/O Address = 36H)**

The Refresh Control Register (RCR) specifies the interval and length of refresh cycles, while enabling or disabling the refresh function.

**REFE: Refresh Enable (Bit 7).** REFE = 0 disables the refresh controller, while REFE = 1 enables refresh cycle insertion. REFE is set to 1 during RESET.

**REFW: Refresh Wait (Bit 6).** REFW = 0 causes the refresh cycle to be two clocks in duration. REFW = 1 causes the refresh cycle to be three clocks in duration by adding a refresh wait cycle (TRW). REFW is set to 1 during RESET.

**CYC1, 0: Cycle Interval (Bit 1,0).** CYC1 and CYC0 specify the interval (in clock cycles) between refresh cycles. When dynamic RAM requires 128 refresh cycles every 2 ms (or 256 cycles in every 4 ms), the required refresh interval is less than or equal to 15.625 µs. Thus, the underlined values indicate the best refresh interval depending on CPU clock frequency. CYC0 and CYC1 are cleared to 0 during RESET (see Table 18).

**Table 18. DRAM Refresh Intervals**

| | | | Time Interval | | | | |
|---|---|---|---|---|---|---|---|
| **CYC1** | **CYC0** | **Insertion Interval** | **PHI: 10 MHz** | **8 MHz** | **6 MHz** | **4 MHz** | **2.5 MHz** |
| 0 | 0 | 10 states | (1.0 µs)* | (1.25 µs)* | 1.66 µs | 2.5 µs | 4.0 µs |
| 0 | 1 | 20 states | (2.0 µs)* | (2.5 µs)* | 3.3 µs | 5.0 µs | 8.0 µs |
| 1 | 0 | 40 states | (4.0 µs)* | (5.0 µs)* | 6.6 µs | 10.0 µs | 16.0 µs |
| 1 | 1 | 80 states | (8.0 µs)* | (10.0 µs)* | 13.3 µs | 20.0 µs | 32.0 µs |

**Note:** *calculated interval.

**Refresh Control and Reset.** After RESET, based on the initialized value of RCR, refresh cycles occur with an interval of 10 clock cycles and be 3 clock cycles in duration.

### Dynamic RAM Refresh Operation

1. Refresh Cycle insertion is stopped when the CPU is in the following states:
   a. During RESET
   b. When the bus is released in response to $\overline{\text{BUSREQ}}$
   c. During SLEEP mode
   d. During $\overline{\text{WAIT}}$ states
2. Refresh cycles are suppressed when the bus is released in response to $\overline{\text{BUSREQ}}$. However, the refresh timer continues to operate. The time at which the first refresh cycle occurs after the Z8S180/Z8L180 reacquires the bus depends on the refresh timer. This cycle offers no timing relationship with the bus exchange.
3. Refresh cycles are suppressed during SLEEP mode. If a refresh cycle is requested during SLEEP mode, the refresh cycle request is internally latched (until replaced with the next refresh request). The latched refresh cycle is inserted at the end of the first machine cycle after SLEEP mode is exited. After this initial cycle, the time at which the next refresh cycle occurs depends on the refresh time and offers no relationship with the exit from SLEEP mode.
4. The refresh address is incremented by one for each successful refresh cycle, not for each refresh. Thus, independent of the number of missed refresh requests, each refresh bus cycle uses a refresh address incremented by one from that of the previous refresh bus cycles.

## MMU COMMON BASE REGISTER

The Common Base Register (CBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical address for Common Area 1 accesses. All bits of CBR are reset to 0 during RESET.

### MMU Common Base Register

**Mnemonic CBR**
**Address 38H**

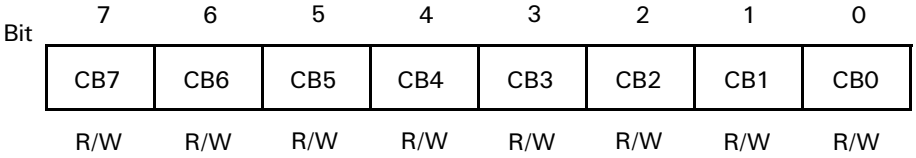


**Figure 78. MMU Common Base Register (CBR: I/O Address = 38H)**

## MMU BANK BASE REGISTER

The Bank Base Register (BBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical address for Bank Area accesses. All bits of BBR are reset to 0 during RESET.

### MMU Bank Base Register

**Mnemonic BBR**
**Address 39H**

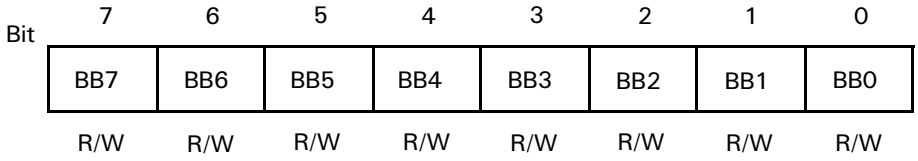


**Figure 79. MMU Bank Base Register (BBR: I/O Address = 39H)**

## MMU COMMON/BANK AREA REGISTER

The Common/Bank Area Register (CBAR) specifies boundaries within the Z8S180/Z8L180 64-KB logical address space for up to three areas; Common Area), Bank Area and Common Area 1.

### MMU Common/Bank Area Register

**Mnemonic CBAR**
**Address 3AH**

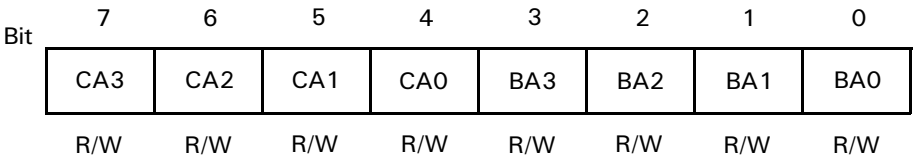


**Figure 80. MMU Common/Bank Area Register (CBAR: I/O Address = 3AH)**