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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	20MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8s18020veg1960

GENERAL DESCRIPTION (Continued)

Power connections follow the conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

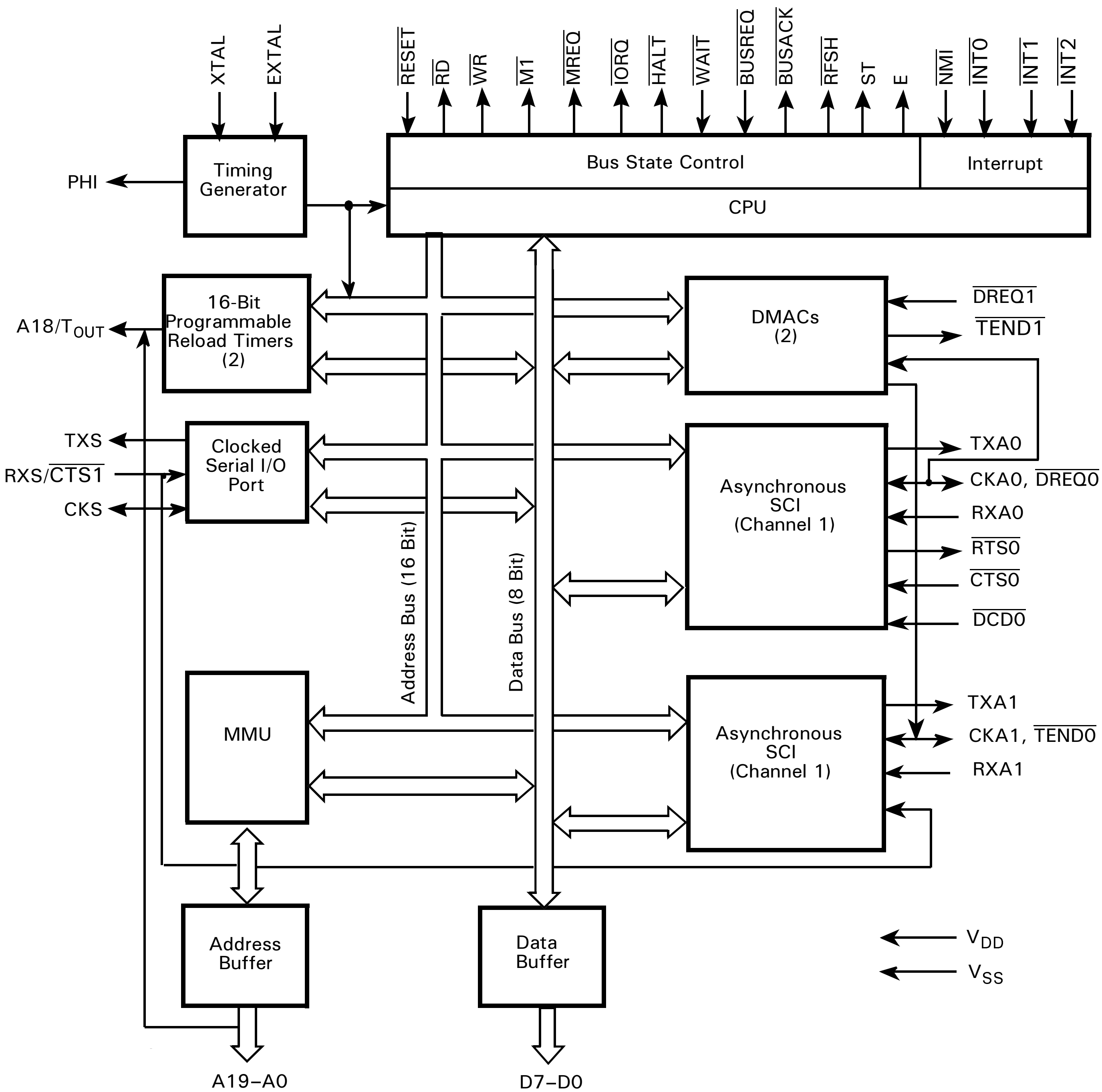

Figure 1. Z8S180/Z8L180 Functional Block Diagram

PIN IDENTIFICATION

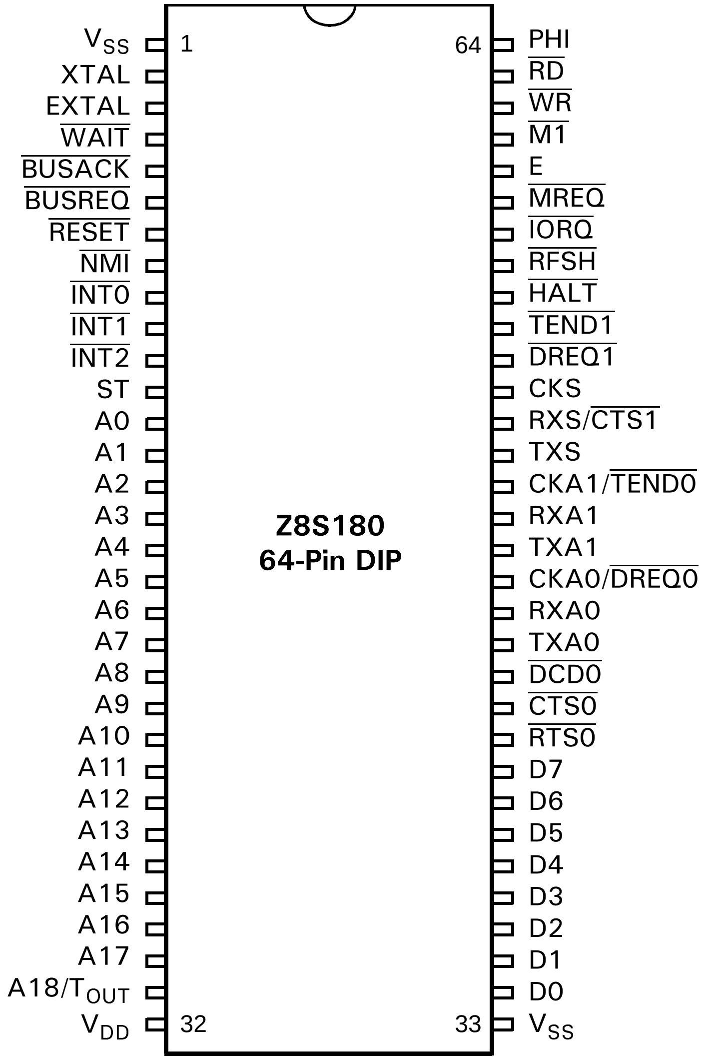

Figure 2. Z8S180 64-Pin DIP Pin Configuration

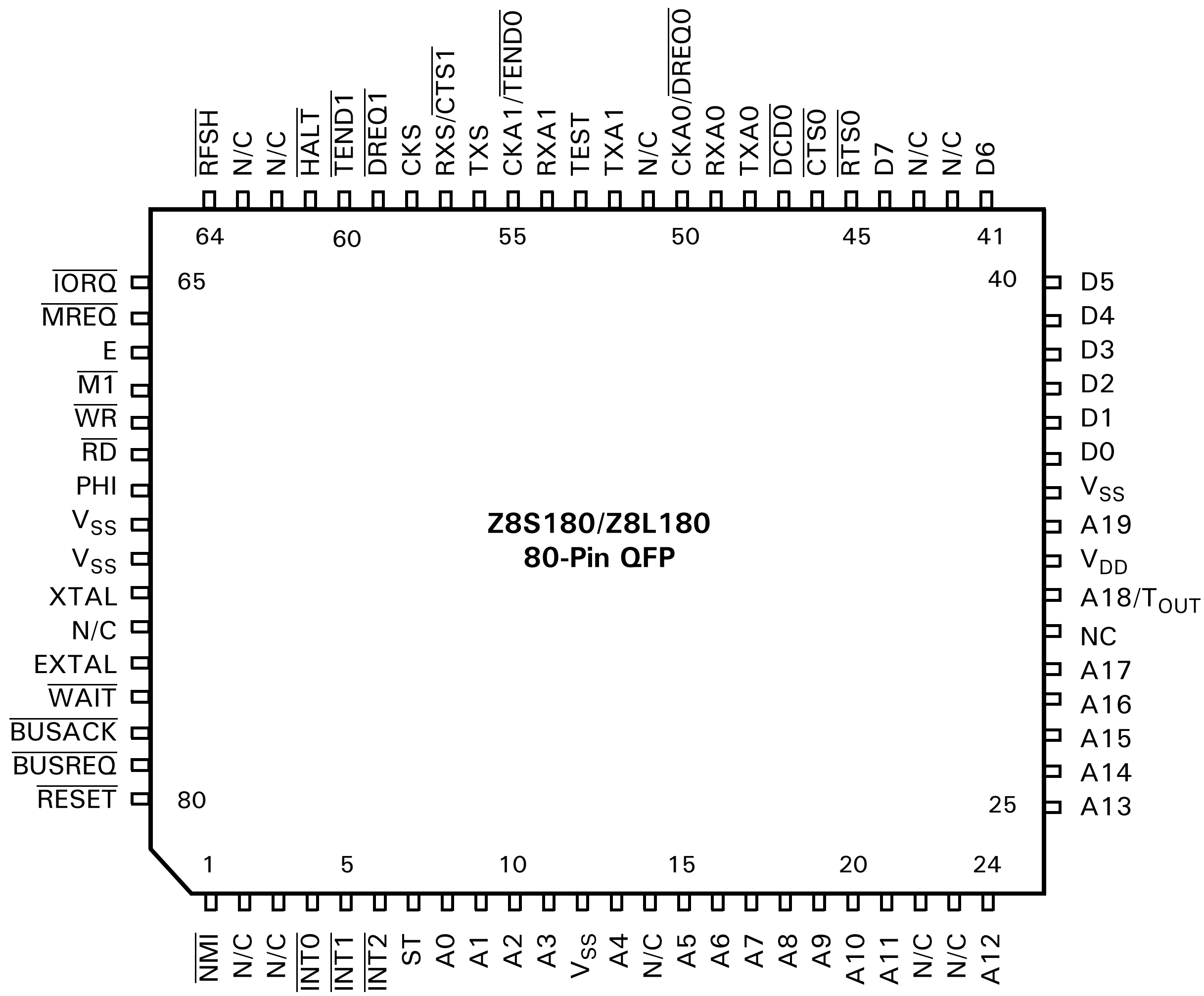

Figure 4. Z8S180/Z8L180 80-Pin QFP Pin Configuration

Table 1. Z8S180/Z8L180 Pin Identification

Pin Number and Package Type					
QFP	**PLCC**	**DIP**	**Default Function**	**Secondary Function**	**Control**
1	9	8	$\overline{NMI}$		
2			NC		
3			NC		
4	10	9	$\overline{INT0}$		
5	11	10	$\overline{INT1}$		
6	12	11	$\overline{INT2}$		
7	13	12	ST		
8	14	13	A0		
9	15	14	A1		
10	16	15	A2		
11	17	16	A3		
12	18		V_{SS}		

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
39	41	38	D4		3T	3T	3T
40	42	39	D5		3T	3T	3T
41	43	40	D6		3T	3T	3T
42			NC				
43			NC				
44	44	41	D7		3T	3T	3T
45	45	42	$\overline{RTS0}$		High	OUT	High
46	46	43	$\overline{CTS0}$		IN	OUT	IN
47	47	44	$\overline{DCD0}$		IN	IN	IN
48	48	45	TXA0		High	OUT	OUT
49	49	46	RXA0		IN	IN	IN
50	50	47	CKA0		3T	I/O	I/O
			$\overline{DREQ0}$		N/A	IN	IN
51			NC				
52	51	48	TXA1		High	OUT	OUT
53	52		TEST				
54	53	49	RXA1		IN	IN	IN
55	54	50	CKA1		3T	I/O	I/O
			$\overline{TEND0}$		N/A	High	High
56	55	51	TXS		High	OUT	OUT
57	56	52	RXS		IN	IN	IN
			$\overline{CTS1}$		N/A	IN	IN
58	57	53	CKS		3T	I/O	I/O
59	58	54	$\overline{DREQ1}$		IN	3T	IN
60	59	55	$\overline{TEND1}$		High	OUT	High
61	60	56	$\overline{HALT}$		High	High	Low
62			NC				
63			NC				
64	61	57	$\overline{RFSH}$		High	OUT	High
65	62	58	$\overline{IORQ}$		High	3T	High
66	63	59	$\overline{MREQ}$		High	3T	High
67	64	60	E		Low	OUT	OUT
68	65	61	$\overline{M1}$		High	High	High
69	66	62	$\overline{WR}$		High	3T	High
70	67	63	$\overline{RD}$		High	3T	High
71	68	64	PHI		OUT	OUT	OUT
72	1	1	V_{SS}		GND	GND	GND
73	2		V_{SS}		GND	GND	GND
74	3	2	XTAL		OUT	OUT	OUT
75			NC				

Table 4. Multiplexed Pin Descriptions

A18/TOUT	During RESET, this pin is initialized as A18. If either the TOC1 or the TOC0 bit of the Timer Control register (TCR) is set to `1`, the T_{OUT} function is selected. If TOC1 and TOC0 are cleared to `0`, the A18 function is selected.
CKA0/$\overline{DREQ0}$	During RESET, this pin is initialized as CKA0. If either DM1 or SM1 in the DMA Mode register (DMODE) is set to `1`, the $\overline{DREQ0}$ function is selected.
CKA1/$\overline{TEND0}$	During RESET, this pin is initialized as CKA1. If the CKA1D bit in ASCI control register ch1 (CNTLA1) is set to `1`, the $\overline{TEND0}$ function is selected. If the CKA1D bit is set to `0`, the CKA1 function is selected.
RXS/$\overline{CTS1}$	During RESET, this pin is initialized as RXS. If the CTS1E bit in the ASCI status register ch1 (STAT1) is set to `1`, the $\overline{CTS1}$ function is selected. If the CTS1E bit is set to `0`, the RXS function is selected.

This condition provides a technique for synchronization with high-speed external events without incurring the latency imposed by an interrupt-response sequence. Figure 14 depicts the timing for exiting SLEEP mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes about 1.5 clock ticks to restart.

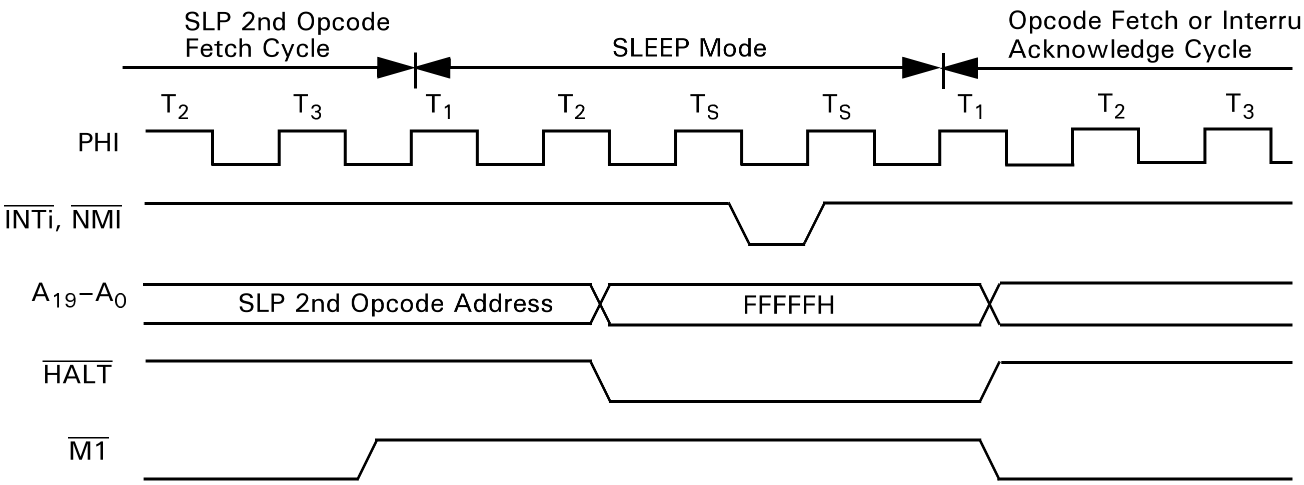

Figure 14. SLEEP Timing

IOSTOP Mode. IOSTOP mode is entered by setting the IOSTOP bit of the I/O Control Register (ICR) to 1. In this case, on-chip I/O (ASCI, CSI/O, PRT) stops operating. However, the CPU continues to operate. Recovery from IOSTOP mode is performed by resetting the IOSTOP bit in ICR to 0.

SYSTEM STOP Mode. SYSTEM STOP mode is the combination of SLEEP and IOSTOP modes. SYSTEM STOP mode is entered by setting the IOSTOP bit in ICR to 1 followed by execution of the SLP instruction. In this mode, on-chip I/O and CPU stop operating, reducing power consumption, but the PHI output continues to operate. Recovery from SYSTEM STOP mode is the same as recovery from SLEEP mode except that internal I/O sources (disabled by IOSTOP) cannot generate a recovery interrupt.

IDLE Mode. Software puts the Z8S180/Z8L180 into this mode by performing the following actions:

- Set the IOSTOP bit (ICR5) to 1
- Set CCR6 to 0
- Set CCR3 to 1
- Execute the SLP instruction

The oscillator keeps operating but its output is blocked to all circuitry including the PHI pin. DRAM refresh and all internal devices stop, but external interrupts can occur. Bus granting to external Masters can occur if the BREST bit in the CPU control Register (CCR5) was set to 1 before IDLE mode was entered.

The Z8S180/Z8L180 leaves IDLE mode in response to a Low on $\overline{RESET}$, an external interrupt request on $\overline{NMI}$, or an external interrupt request on $\overline{INT0}$, $\overline{INT1}$ or $\overline{INT2}$ that is enabled in the INT/TRAP Control Register. As previously described for SLEEP mode, when the Z8S180/Z8L180 leaves IDLE mode due to an $\overline{NMI}$, or due to an enabled external interrupt request when the $\overline{IEF}$ flag is 1 due to an EI instruction, the device starts by performing the interrupt with the return address of the instruction after the SLP instruction.

If an external interrupt enables the INT/TRAP control register while the IEF1 bit is 0, Z8S180/Z8L180 leaves IDLE mode; specifically, the processor restarts by executing the instructions following the SLP instruction.

Figure 15 indicates the timing for exiting IDLE mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes about 9.5 clocks to restart.

ing the bus to an external Master during STANDBY mode, when the BREXT bit in the CPU Control Register (CCR5) is 1.

As described previously for SLEEP and IDLE modes, when the MPU leaves STANDBY mode due to $\overline{\text{NMI}}$ Low or an enabled $\overline{\text{INT0}}$–$\overline{\text{INT2}}$ Low when the IEF, flag is 1 due to an IE instruction, it starts by performing the interrupt with the return address being that of the instruction following the SLP instruction. If the Z8S180/Z8L180 leaves STANDBY mode due to an external interrupt request that's enabled in the INT/TRAP Control Register, but the IEF, bit is 0 due to a DI instruction, the processor restarts by executing the instruction(s) following the SLP instruction. If $\overline{\text{INT0}}$, or $\overline{\text{INT1}}$ or $\overline{\text{INT2}}$ goes inactive before the end of the clock stabilization delay, the Z8S180/Z8L180 stays in STANDBY mode.

Figure 17 indicates the timing for leaving STANDBY mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes either 64 or 2^{17} (131,072) clocks to restart, depending on the CCR3 bit.

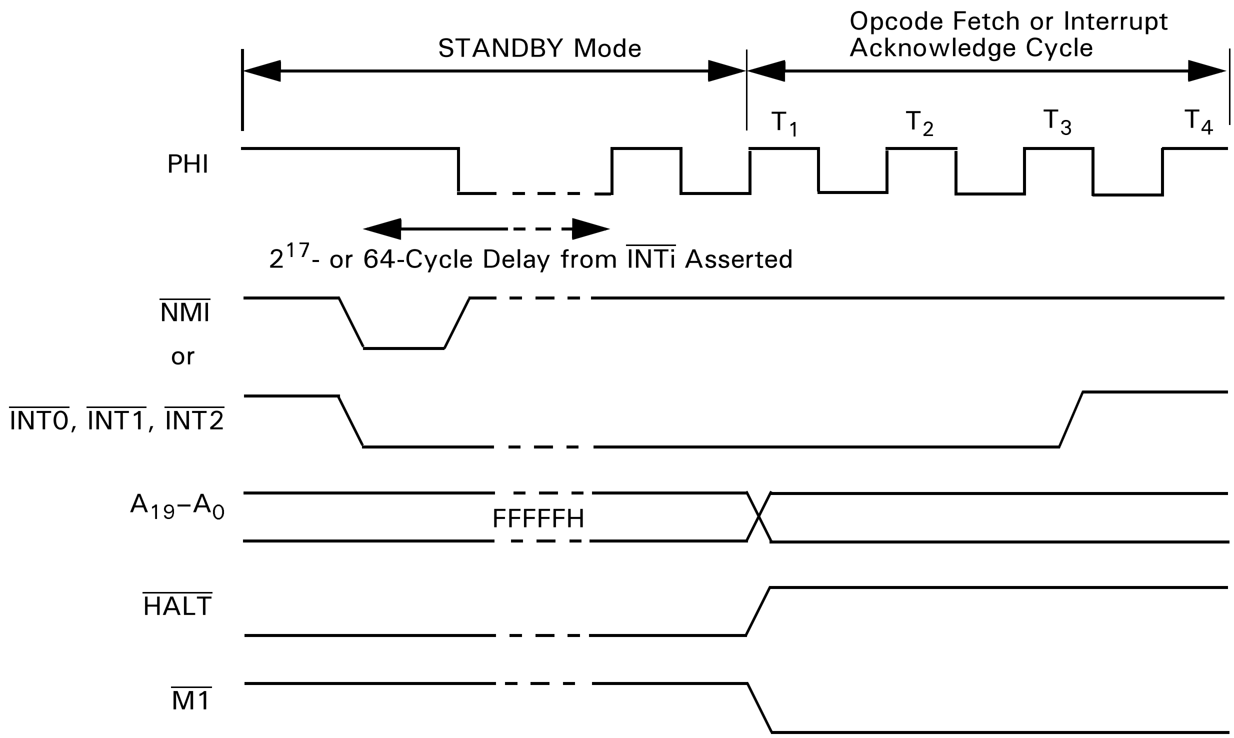

Figure 17. Z8S180/Z8L180 STANDBY Mode Exit Due to External Interrupt

While the Z8S180/Z8L180 is in STANDBY mode, it grants the bus to an external Master if the BREXT bit (CCR5) is 1. Figure 18 indicates the timing of this sequence. The device takes 64 or 2^{17} (131,072) clock cycles to grant the bus depending on the CCR3 bit. The latter (not the QUICK RECOVERY) case may be prohibitive for many demand-driven external Masters. If so, QUICK RECOVERY or IDLE mode can be used.

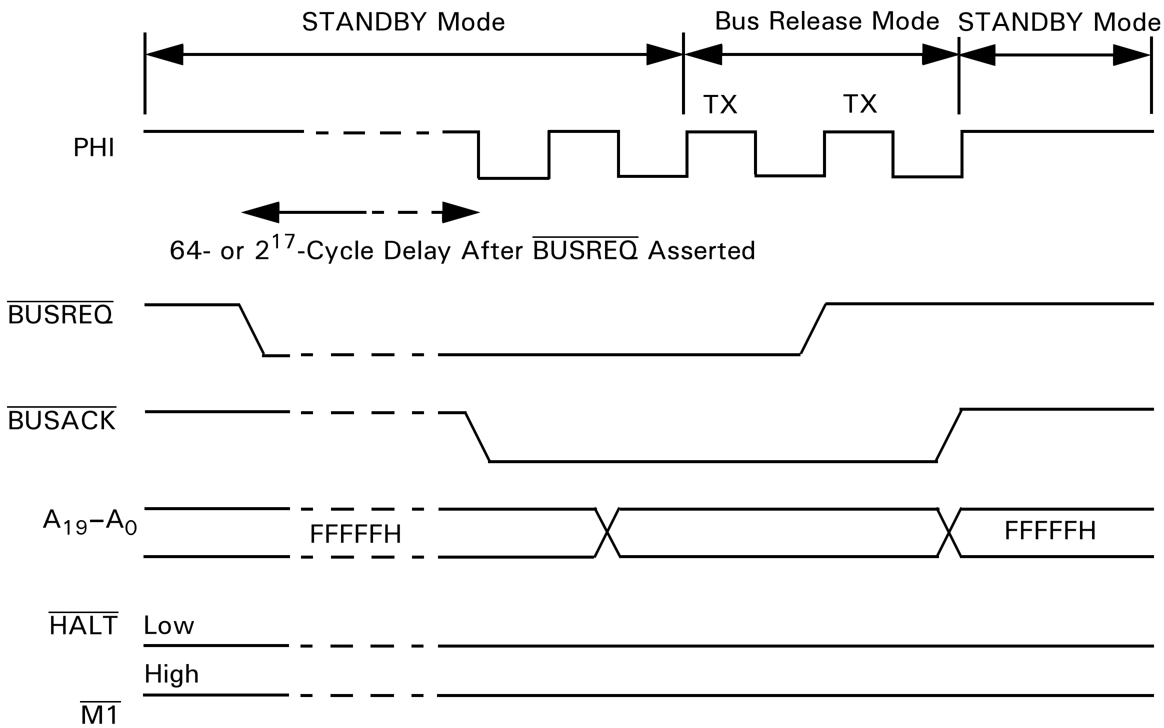

Figure 18. Bus Granting to External Master During STANDBY Mode

Table 7. Z8L180 DC Characteristics
V_{DD} = 3.3V ±10%; V_{SS} = 0V

Symbol	Item	Condition	Min	Typ	Max	Unit
V_{IH1}	Input H Voltage $\overline{RESET}$, EXTAL, $\overline{NMI}$		V_{DD} –0.6		V_{DD} +0.3	V
V_{IH2}	Input H Voltage Except $\overline{RESET}$, EXTAL, $\overline{NMI}$		2.0		V_{DD} +0.3	V
V_{IL1}	Input L Voltage RESET, EXTAL, NMI		–0.3		0.6	V
V_{IL2}	Input L Voltage Except RESET, EXTAL, NMI		–0.3		0.8	V
V_{OH}	Outputs H Voltage All outputs	I_{OH} = –200 µA	2.15			V
		I_{OH} = –20 µA	V_{DD} –0.6			V
V_{OL}	Outputs L Voltage All Outputs	I_{OL} = 4 mA			0.4	V
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL	V_{IN} = 0.5 ~ V_{DD} –0.5			1.0	µA
I_{TL}	Three State Leakage Current	V_{IN} = 0.5 ~ V_{DD} –0.5			1.0	µA
I_{DD1}	Power Dissipation (Normal Operation)	F = 20 MHz		30	60	mA
		4 MHz		4	10	
	Power Dissipation (SYSTEM STOP mode)	F = 20 MHz		5	10	
		4 MHz		2	5	
C_P	Pin Capacitance	V_{IN} = 0V, f = 1 MHz T_A = 25° C			12	pF

Note:
1. V_{IHmin} = V_{DD} –1.0V, V_{ILmax} = 0.6V (All output terminals are at NO LOAD.) V_{DD} = 3.0V.

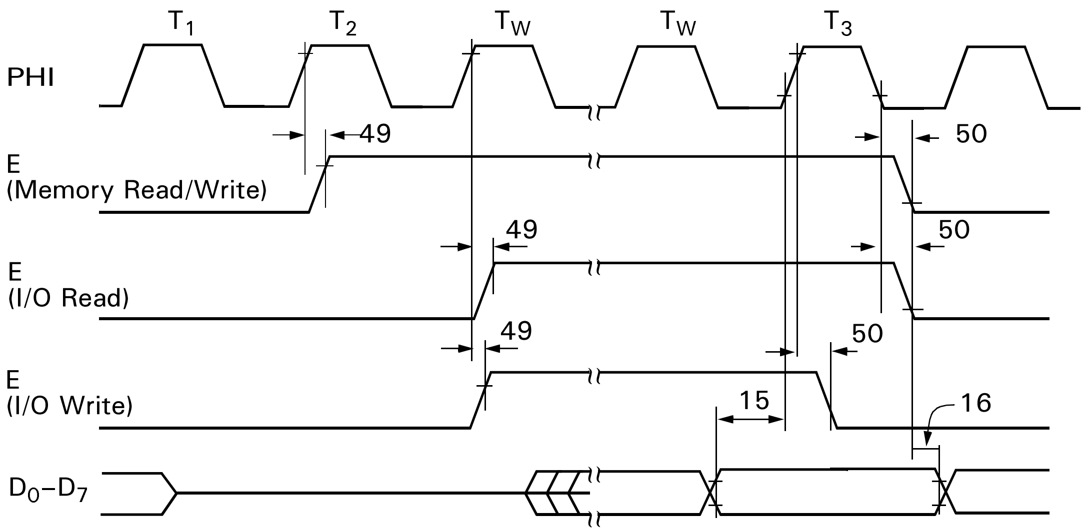

Figure 24. E Clock Timing
(Memory Read/Write Cycle, I/O Read/Write Cycle)

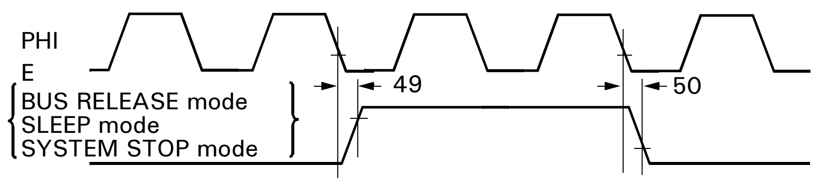

Figure 25. E Clock Timing
(BUS RELEASE Mode, SLEEP Mode, SYSTEM STOP Mode)

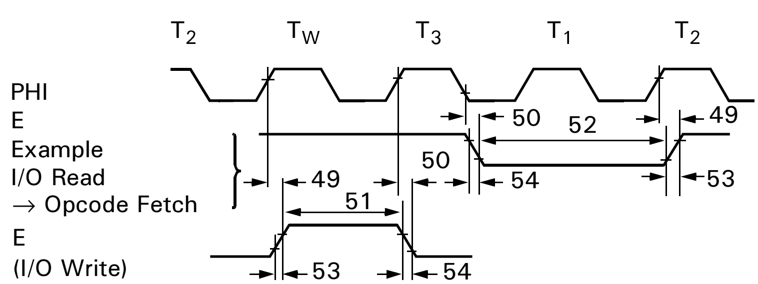

Figure 26. E Clock Timing
(Minimum Timing Example of P_{WEL} and P_{WEH})

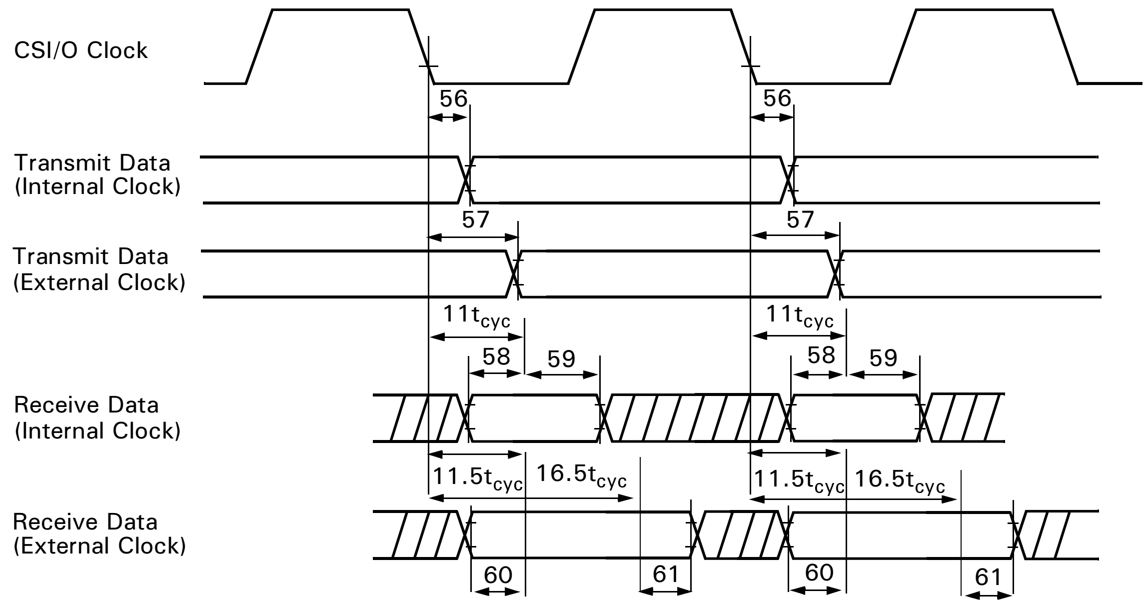

Figure 29. CSI/O Receive/Transmit Timing

External Clock Rise Time
and Fall Time

Input Rise Time and Fall Time
(Except EXTAL, $\overline{\text{RESET}}$)

Figure 30. Rise Time and Fall Times

CPU CONTROL REGISTER

CPU Control Register (CCR). This register controls the basic clock rate, certain aspects of Power-Down modes, and output drive/low-noise options (Figure 31).

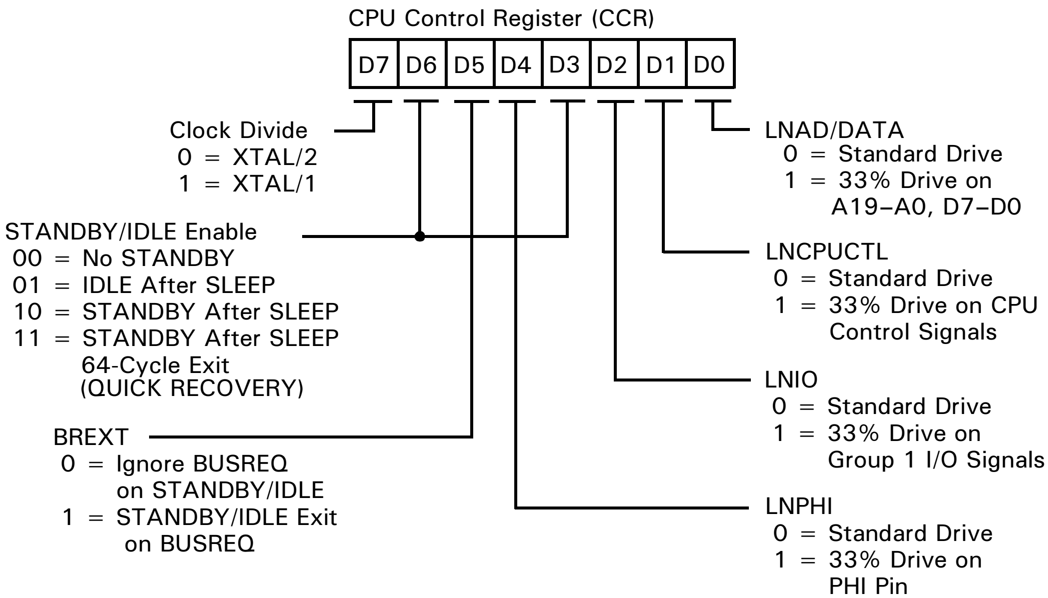

Figure 31. CPU Control Register (CCR) Address 1FH

Bit 7. Clock Divide Select. If this bit is 0, as it is after a RESET, the Z8S180/Z8L180 divides the frequency on the XTAL pin(s) by two to obtain its Master clock PHI. If this bit is programmed as 1, the part uses the XTAL frequency as PHI without division.

If an external oscillator is used in divide-by-one mode, the minimum pulse width requirement provided in the AC Characteristics must be satisfied.

Bits 6 and 3. STANDBY/IDLE Control. When these bits are both 0, a SLP instruction makes the Z8S180/Z8L180 enter SLEEP or SYSTEM STOP mode, depending on the IOSTOP bit (ICR5).

When D6 is 0 and D3 is 1, setting the IOSTOP bit (ICR5) and executing a SLP instruction puts the Z8S180/Z8L180 into IDLE mode in which the on-chip oscillator runs, but its output is blocked from the rest of the part, including PHI out.

When D6 is 1 and D3 is 0, setting IOSTOP (ICR5) and executing a SLP instruction puts the part into STANDBY mode, in which the on-chip oscillator is stopped and the part allows 2^{17} (128K) clock cycles for the oscillator to stabilize when it restarts.

When D6 and D3 are both 1, setting IOSTOP (ICR5) and executing a SLP instruction puts the part into QUICK RECOVERY STANDBY mode, in which the on-chip oscillator is stopped, and the part allows only 64 clock cycles for the oscillator to stabilize when it restarts.

The latter section, HALT and LOW POWER modes, describes the subject more fully.

Bit 5 BREXT. This bit controls the ability of the Z8S180/Z8L180 to honor a bus request during STANDBY mode. If this bit is set to 1 and the part is in STANDBY mode, a BUSREQ is honored after the clock stabilization timer is timed out.

Bit 4 LNPHI. This bit controls the drive capability on the PHI Clock output. If this bit is set to 1, the PHI Clock output is reduced to 33 percent of its drive capability.

Bit 2 LNIO. This bit controls the drive capability of certain external I/O pins of the Z8S180/Z8L180. When this bit is set to 1, the output drive capability of the following pins is reduced to 33 percent of the original drive capability:

$\overline{\text{RTS0}}$	TxS
CKA1/$\overline{\text{TEND0}}$	CKA0/$\overline{\text{DREQ0}}$
TXA0	TXA1
$\overline{\text{TENDi}}$	CKS

Bit 1 LNCPUCTL. This bit controls the drive capability of the CPU Control pins. When this bit is set to 1, the output drive capability of the following pins is reduced to 33 percent of the original drive capability:

$\overline{\text{BUSACK}}$	$\overline{\text{RD}}$
$\overline{\text{WR}}$	$\overline{\text{M1}}$
$\overline{\text{MREQ}}$	$\overline{\text{IORQ}}$
$\overline{\text{RFSH}}$	$\overline{\text{HALT}}$
E	TEST
ST	

Bit 0 LNAD/DATA. This bit controls the drive capability of the Address/Data bus output drivers. If this bit is set to 1, the output drive capability of the Address and Data bus outputs is reduced to 33 percent of its original drive capability.

ASCI CHANNEL CONTROL REGISTER B

ASCI Control Register B 0 (CNTLB0: I/O Address = 02H)
ASCI Control Register B 1 (CNTLB1: I/O Address = 03H)

Bit	7	6	5	4	3	2	1	0
	MPBT	MP	$\overline{CTS}$/PS	PEO	DR	SS2	SS1	SS0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 34. ASCI Channel Control Register B

MPBT: Multiprocessor Bit Transmit (Bit 7). When multiprocessor communication format is selected (MP bit = 1), MPBT is used to specify the MPB data bit for transmission. If MPBT = 1, then MPB = 1 is transmitted. If MPBT = 0, then MPB = 0 is transmitted. The MPBT state is undefined during and after RESET.

MP: Multiprocessor Mode (Bit 6). When MP is set to 1, the data format is configured for multiprocessor mode based on MOD2 (number of data bits) and MOD0 (number of stop bits) in CNTLA. The format is as follows:

Start bit + 7 or 8 data bits + MPB bit + 1 or 2 stop bits

Multiprocessor (MP = 1) format offers no provision for parity. If MP = 0, the data format is based on MOD0, MOD1, MOD2, and may include parity. The MP bit is cleared to 0 during RESET.

$\overline{CTS}$/PS: Clear to Send/Prescale (Bit 5). When read, $\overline{CTS}$/PS reflects the state of the external $\overline{CTS}$ input. If the $\overline{CTS}$ input pin is High, $\overline{CTS}$/PS is read as 1.

Note: When the $\overline{CTS}$ input pin is High, the TDRE bit is inhibited (that is, held at 0).

For channel 1, the $\overline{CTS}$ input is multiplexed with RXS pin (Clocked Serial Receive Data). Thus, $\overline{CTS}$/PS is only valid when read if the channel 1 CTS1E bit = 1 and the $\overline{CTS}$ input pin function is selected. The READ data of $\overline{CTS}$/PS is not affected by $\overline{RESET}$.

If the SS2–0 bits in this register are not 111, and the BRG mode bit in the ASEXT register is 0, then writing to this bit sets the prescale (PS) control. Under those circumstances, a 0 indicates a divide-by-10 prescale function while a 1 indicates divide-by-30. The bit resets to 0.

PEO: Parity Even Odd (Bit 4) . PEO selects oven or odd parity. PEO does not affect the enabling/disabling of parity (MOD1 bit of CNTLA). If PEO is cleared to 0, even parity is selected. If PEO is set to 1, odd parity is selected. PEO is cleared to 0 during RESET.

DR: Divide Ratio (Bit 3). If the X1 bit in the ASEXT register is 0, this bit specifies the divider used to obtain baud rate from the data sampling clock. If DR is reset to 0, divide-by-16 is used, while if DR is set to 1, divide-by-64 is used. DR is cleared to 0 during RESET.

SS2,1,0: Source/Speed Select 2,1,0 (Bits 2–0). First, if these bits are 111, as they are after a RESET, the CKA pin is used as a clock input, and is divided by 1, 16, or 64 depending on the DR bit and the X1 bit in the ASEXT register.

If these bits are not 111 and the BRG mode bit is ASEXT is 0, then these bits specify a power-of-two divider for the PHI clock as indicated in Table 10.

Setting or leaving these bits as 111 makes sense for a channel only when its CKA pin is selected for the CKA function. CKA0/CKS offers the CKA0 function when bit 4 of the System Configuration Register is 0. $\overline{DCD0}$/CKA1 offers the CKA1 function when bit 0 of the Interrupt Edge register is 1.

Table 10. Divide Ratio

SS2	SS1	SS0	Divide Ratio
0	0	0	÷1
0	0	1	÷2
0	1	0	÷4
0	1	1	÷8
1	0	0	÷16
1	0	1	÷32
1	1	0	÷64
1	1	1	External Clock

ASCI0 requests an interrupt when $\overline{DCD0}$ goes High. RIE is cleared to 0 by RESET.

$\overline{DCD0}$: Data Carrier Detect (Bit 2 STAT0). This bit is set to 1 when the pin is High. It is cleared to 0 on the first READ of STAT0 following the pin's transition from High to Low and during RESET. When bit 6 of the ASEXT0 register is 0 to select auto-enabling, and the pin is negated (High), the receiver is reset and its operation is inhibited.

$\overline{CTS1E}$: Clear To Send (Bit 2 STAT1). Channel 1 features an external $\overline{CTS1}$ input, which is multiplexed with the receive data pin RSX for the CSI/O. Setting this bit to 1 selects the CTS1 function; clearing the bit to 0 selects the RXS function.

TDRE: Transmit Data Register Empty (Bit 1). TDRE = 1 indicates that the TDR is empty and the next transmit data byte is written to TDR. After the byte is written to TDR, TDRE is cleared to 0 until the ASCI transfers the byte from TDR to the TSR and then TDRE is again set to 1. TDRE is set to 1 in IOSTOP mode and during RESET. On ASCI0, if the $\overline{CTS0}$ pin is auto-enabled in the ASEXT0 register and the pin is High, TDRE is reset to 0.

TIE: Transmit Interrupt Enable (Bit 0). TIE should be set to 1 to enable ASCI transmit interrupt requests. If TIE = 1, an interrupt is requested when TDRE = 1. TIE is cleared to 0 during RESET.

ASCI TRANSMIT DATA REGISTERS

Register addresses 06H and 07H hold the ASCI transmit data for channel 0 and channel 1, respectively.

ASCI Transmit Data Registers Channel 0

Mnemonic TDR0
Address 06H

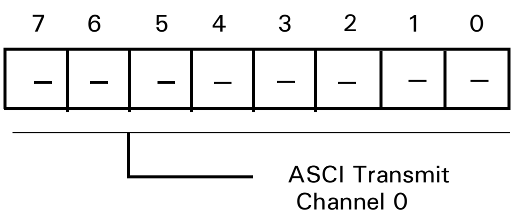

Figure 36. ASCI Register

ASCI Transmit Data Registers Channel 1

Mnemonic TDR1
Address 07H

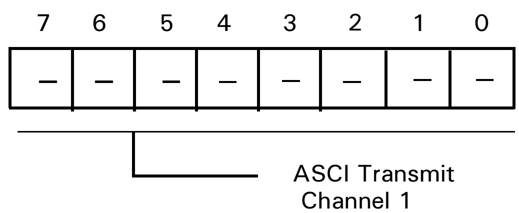

Figure 37. ASCI Register

DMA MODE REGISTER

The DMA Mode Register (DMODE) is used to set the addressing and transfer mode for channel 0.

DMA Mode Register

Mnemonic DMODE
Address 31H

Bit	7	6	5	4	3	2	1	0
	—	—	DM1	DM0	SM1	SM0	MMOD	—
			R/W	R/W	R/W	R/W	R/W	

Figure 72. DMA Mode Register (DMODE: I/O Address = 31H)

DM1, DM0: Destination Mode Channel 0 (Bits 5,4). This mode specifies whether the destination for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred. DM1 and DM0 are cleared to 0 during RESET.

Table 14. Channel 0 Destination

DM1	DM0	Memory I/O	Memory Increment/Decrement
0	0	Memory	+1
0	1	Memory	–1
1	0	Memory	fixed
1	1	I/O	fixed

SM1, SM0: Source Mode Channel 0 (Bits 3, 2) . This mode specifies whether the source for channel 0 transfers is memory or I/O, and whether the address should be incremented or decremented for each byte transferred.

Table 15. Channel 0 Source

SM1	SM0	Memory I/O	Memory Increment/Decrement
0	0	Memory	+1
0	1	Memory	–1
1	0	Memory	fixed
1	1	I/O	fixed

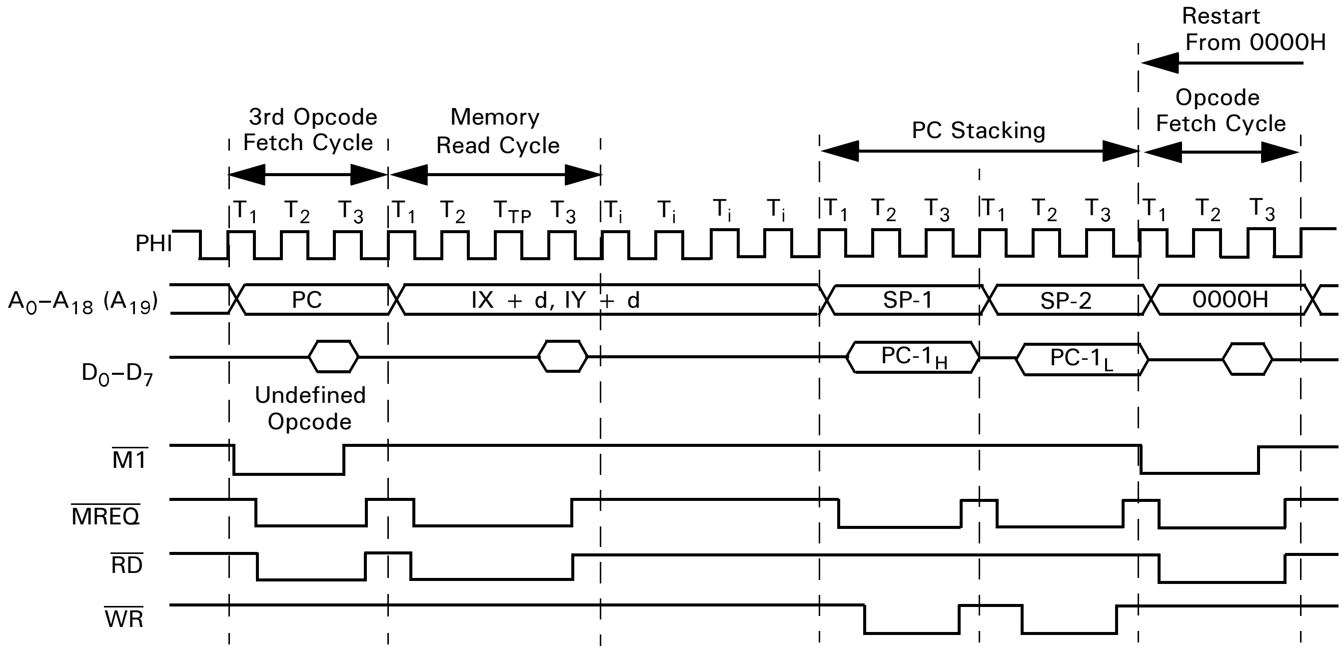

Figure 76. TRAP Timing—3rd Opcode Undefined

MMU COMMON BASE REGISTER

The Common Base Register (CBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical address for Common Area 1 accesses. All bits of CBR are reset to 0 during RESET.

MMU Common Base Register

Mnemonic CBR
Address 38H

Bit	7	6	5	4	3	2	1	0
	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 78. MMU Common Base Register (CBR: I/O Address = 38H)

MMU BANK BASE REGISTER

The Bank Base Register (BBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical address for Bank Area accesses. All bits of BBR are reset to 0 during RESET.

MMU Bank Base Register

Mnemonic BBR
Address 39H

Bit	7	6	5	4	3	2	1	0
	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 79. MMU Bank Base Register (BBR: I/O Address = 39H)

MMU COMMON/BANK AREA REGISTER

The Common/Bank Area Register (CBAR) specifies boundaries within the Z8S180/Z8L180 64-KB logical address space for up to three areas; Common Area), Bank Area and Common Area 1.

MMU Common/Bank Area Register

Mnemonic CBAR
Address 3AH

Bit	7	6	5	4	3	2	1	0
	CA3	CA2	CA1	CA0	BA3	BA2	BA1	BA0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 80. MMU Common/Bank Area Register (CBAR: I/O Address = 3AH)

CA3–CA0:CA (Bits 7–4). CA specifies the start (Low) address (on 4-KB boundaries) for Common Area 1. This condition also determines the most recent address of the Bank Area. All bits of CA are set to 1 during RESET.

BA3–BA0 (Bits 3–0). BA specifies the start (Low) address (on 4-KB boundaries) for the Bank Area. This condition also determines the most recent address of Common Area 0. All bits of BA are set to 1 during RESET.

OPERATION MODE CONTROL REGISTER

The Z8S180/Z8L180 is descended from two different ancestor processors, ZiLOG's original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR) can be programmed to select between certain differences between the Z80 and the 64180.

Operation Mode Control Register

Mnemonic OMCR
Address 3EH

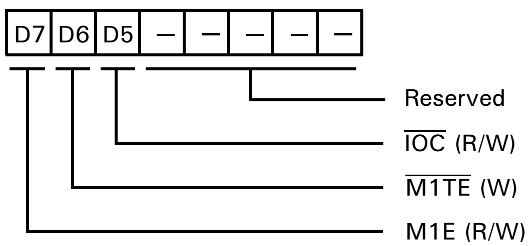

Figure 81. Operating Control Register (OMCR: I/O Address = 3EH)

M1E ($\overline{M1}$ Enable). This bit controls the $\overline{M1}$ output and is set to a 1 during reset.

When M1E = 1, the $\overline{M1}$ output is asserted Low during the opcode fetch cycle, the $\overline{INT0}$ acknowledge cycle, and the first machine cycle of the $\overline{NMI}$ acknowledge.

On the Z8S180/Z8L180, this choice makes the processor fetch one RETI instruction. When fetching a RETI from zero-wait-state memory, the processor uses three clock machine cycles that are not fully Z80-timing-compatible.

When M1E = 0, the processor does not drive $\overline{M1}$ Low during instruction fetch cycles. After fetching one RETI instruction with normal timing, the processor returns and refetches the instruction using Z80-compatible cycles that drive $\overline{M1}$ Low. This timing compatibility may be required by external Z80 peripherals to properly decode the RETI instruction.

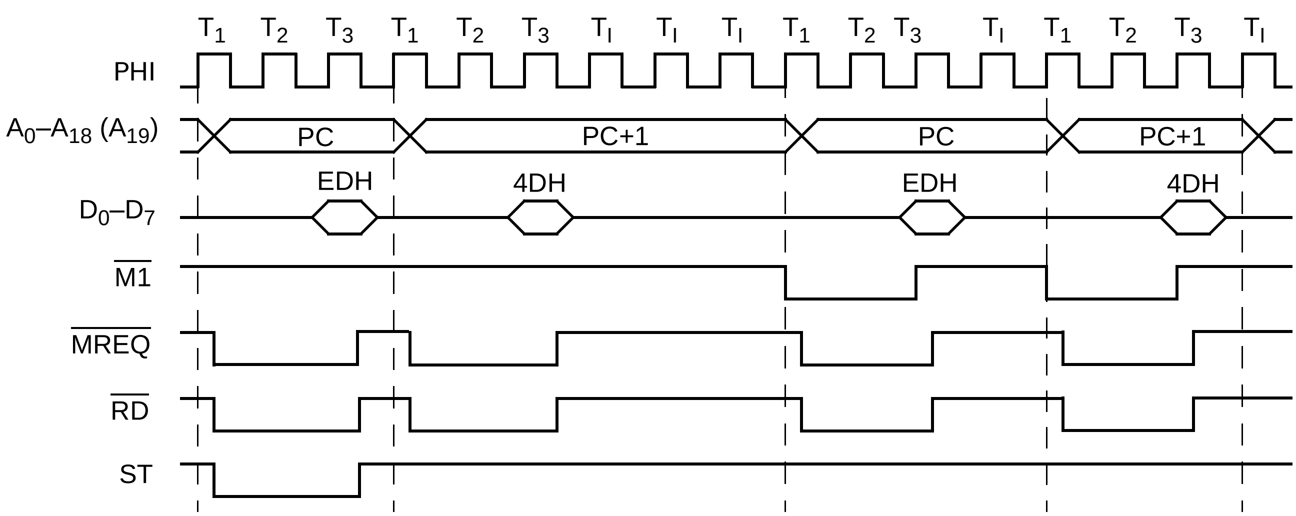

Figure 82. RETI Instruction Sequence with M1E = 0

I/O CONTROL REGISTER

The I/O Control Register (ICR) allows relocation of the internal I/O addresses. ICR also controls the enabling and disabling of IOSTOP mode (Figure 83).

Bit	7	6	5	4	3	2	1	0
	IOA7	IOA6	IOSTP	–	–	–	–	–
	R/W	R/W	R/W					

Figure 83. I/O Control Register (ICR: I/O Address = 3FH)

IOA7, 6: I/O Address Relocation (Bits 7,6). IOA7 and IOA6 relocate internal I/O as indicated in Figure 84.

Note: The high-order 8 bits of 16-bit internal I/O address are always 0. IOA7 and IOA6 are cleared to 0 during RESET.

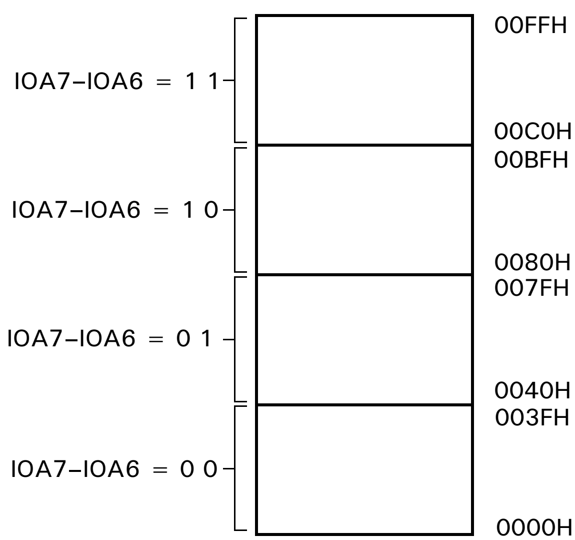

Figure 84. I/O Address Relocation

IOSTP: IOSTOP Mode (Bit 5). IOSTOP mode is enabled when IOSTP is set to 1. Normal I/O operation resumes when IOSTP is reprogrammed or RESET to 0.