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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	20MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8s18020vsc1960

PIN IDENTIFICATION (Continued)

Table 1. Z8S180/Z8L180 Pin Identification (Continued)

Pin Number and Package Type			Default Function	Secondary Function	Control
QFP	PLCC	DIP			
13	19	17	A4		
14			NC		
15	20	18	A5		
16	21	19	A6		
17	22	20	A7		
18	23	21	A8		
19	24	22	A9		
20	25	23	A10		
21	26	24	A11		
22			NC		
23			NC		
24	27	25	A12		
25	28	26	A13		
26	29	27	A14		
27	30	28	A15		
28	31	29	A16		
29	32	30	A17		
30			NC		
31	33	31	A18	T _{OUT}	Bit 2 or Bit 3 of TCR
32	34	32	V _{DD}		
33	35		A19		
34	36	33	V _{SS}		
35	37	34	D0		
36	38	35	D1		
37	39	36	D2		
38	40	37	D3		
39	41	38	D4		
40	42	39	D5		
41	43	40	D6		
42			NC		
43			NC		
44	44	41	D7		
45	45	42	$\overline{\text{RTS0}}$		
46	46	43	$\overline{\text{CTS0}}$		
47	47	44	$\overline{\text{DCD0}}$		
48	48	45	TXA0		
49	49	46	RXA0		
50	50	47	CKA0	$\overline{\text{DREQ0}}$	Bit 3 or Bit 5 of DMODE
51			NC		
52	51	48	TXA1		

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)

Pin Number and Package Type			Pin Status				
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
39	41	38	D4		3T	3T	3T
40	42	39	D5		3T	3T	3T
41	43	40	D6		3T	3T	3T
42			NC				
43			NC				
44	44	41	D7		3T	3T	3T
45	45	42	$\overline{\text{RTS0}}$		High	OUT	High
46	46	43	$\overline{\text{CTS0}}$		IN	OUT	IN
47	47	44	$\overline{\text{DCD0}}$		IN	IN	IN
48	48	45	TXA0		High	OUT	OUT
49	49	46	RXA0		IN	IN	IN
50	50	47	CKA0		3T	I/O	I/O
			$\overline{\text{DREQ0}}$		N/A	IN	IN
51			NC				
52	51	48	TXA1		High	OUT	OUT
53	52		TEST				
54	53	49	RXA1		IN	IN	IN
55	54	50	CKA1		3T	I/O	I/O
			$\overline{\text{TEND0}}$		N/A	High	High
56	55	51	TXS		High	OUT	OUT
57	56	52	RXS		IN	IN	IN
			$\overline{\text{CTS1}}$		N/A	IN	IN
58	57	53	CKS		3T	I/O	I/O
59	58	54	$\overline{\text{DREQ1}}$		IN	3T	IN
60	59	55	$\overline{\text{TEND1}}$		High	OUT	High
61	60	56	$\overline{\text{HALT}}$		High	High	Low
62			NC				
63			NC				
64	61	57	$\overline{\text{RFSH}}$		High	OUT	High
65	62	58	$\overline{\text{IORQ}}$		High	3T	High
66	63	59	$\overline{\text{MREQ}}$		High	3T	High
67	64	60	E		Low	OUT	OUT
68	65	61	$\overline{\text{M1}}$		High	High	High
69	66	62	$\overline{\text{WR}}$		High	3T	High
70	67	63	$\overline{\text{RD}}$		High	3T	High
71	68	64	PHI		OUT	OUT	OUT
72	1	1	V _{SS}		GND	GND	GND
73	2		V _{SS}		GND	GND	GND
74	3	2	XTAL		OUT	OUT	OUT
75			NC				

PIN IDENTIFICATION (Continued)

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
76	4	3	EXTAL		IN	IN	IN
77	5	4	$\overline{\text{WAIT}}$		IN	IN	IN
78	6	5	$\overline{\text{BUSACK}}$		High	OUT	OUT
79	7	6	$\overline{\text{BUSREQ}}$		IN	IN	IN
80	8	7	$\overline{\text{RESET}}$		IN	IN	IN

PIN DESCRIPTIONS

A0–A19. Address Bus (Output, 3-state). A0–A19 form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 1 MB) and I/O data bus exchanges (up to 64 KB). The address bus enters a high-impedance state during reset and external bus acknowledge cycles. Address line A18 is multiplexed with the output of PRT channel 1 (T_{OUT} , selected as address output on reset), and address line A19 is not available in DIP versions of the Z8S180.

BUSACK. Bus Acknowledge (Output, active Low). \overline{BUSACK} indicates that the requesting device, the MPU address and data bus, and some control signals enter their high-impedance state.

BUSREQ. Bus Request (Input, active Low). This input is used by external devices (such as DMA controllers) to request access to the system bus. This request demands a higher priority than \overline{NMI} and is always recognized at the end of the current machine cycle. This signal stops the CPU from executing further instructions, places addresses, data buses, and other control signals into the high-impedance state.

CKA0, CKA1. Asynchronous Clock 0 and 1 (bidirectional). When in output mode, these pins are the transmit and receive clock outputs from the ASCII baud rate generators. When in input mode, these pins serve as the external clock inputs for the ASCII baud rate generators. CKA0 is multiplexed with $\overline{DREQ0}$, and CKA1 is multiplexed with $\overline{TEND0}$.

CKS. Serial Clock (bidirectional). This line is the clock for the CSI/O channel.

CTS0–CTS1. Clear to send 0 and 1 (Inputs, active Low). These lines are modem control signals for the ASCII channels. $\overline{CTS1}$ is multiplexed with RXS.

D0–D7. Data Bus = (bidirectional, 3-state). D0–D7 constitute an 8-bit bidirectional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high-impedance state during reset and external bus acknowledge cycles.

DCD0. Data Carrier Detect 0 (Input, active Low); a programmable modem control signal for ASCII channel 0.

DREQ0, DREQ1. DMA Request 0 and 1 (Input, active Low). \overline{DREQ} is used to request a DMA transfer from one of the on-chip DMA channels. The DMA channels monitor these inputs to determine when an external device is ready for a READ or WRITE operation. These inputs can be programmed to be either level or edge sensed. $\overline{DREQ0}$ is multiplexed with CKA0.

E. Enable Clock (Output). This pin functions as a synchronous, machine-cycle clock output during bus transactions.

EXTAL. External Clock Crystal (Input). Crystal oscillator connections. An external clock can be input to the Z8S180/Z8L180 on this pin when a crystal is not used. This input is Schmitt triggered.

HALT. HALT/SLEEP (Output, active Low). This output is asserted after the CPU executes either the HALT or SLEEP instruction and is waiting for either a nonmaskable or a maskable interrupt before operation can resume. It is also used with the $\overline{M1}$ and ST signals to decode the status of the CPU machine cycle.

INT0. Maskable Interrupt Request 0 (Input, active Low). This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the \overline{NMI} and \overline{BUSREQ} signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the $\overline{M1}$ and \overline{IORQ} signals become active.

INT1, INT2. Maskable Interrupt Request 1 and 2 (Inputs, active Low). This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the \overline{NMI} , \overline{BUSREQ} , and $\overline{INT0}$ signals are inactive. The CPU acknowledges these requests with an interrupt acknowledge cycle. Unlike the acknowledgment for $\overline{INT0}$, neither the $\overline{M1}$ or \overline{IORQ} signals become active during this cycle.

IORQ. I/O Request (Output, active Low, 3-state). \overline{IORQ} indicates that the address bus contains a valid I/O address for an I/O READ or I/O WRITE operation. \overline{IORQ} is also generated, along with $\overline{M1}$, during the acknowledgment of the $\overline{INT0}$ input signal to indicate that an interrupt response vector can be placed onto the data bus. This signal is analogous to the \overline{IOE} signal of the Z64180.

M1. Machine Cycle 1 (Output, active Low). Together with \overline{MREQ} , $\overline{M1}$ indicates that the current cycle is the opcode-fetch cycle of instruction execution. Together with \overline{IORQ} , $\overline{M1}$ indicates that the current cycle is for interrupt acknowledgment. It is also used with the \overline{HALT} and ST signal to decode the status of the CPU machine cycle. This signal is analogous to the \overline{LIR} signal of the Z64180.

MREQ. Memory Request (Output, active Low, 3-state). \overline{MREQ} indicates that the address bus holds a valid address for a memory READ or memory WRITE operation. This signal is analogous to the \overline{ME} signal of Z64180.

NMI. Nonmaskable Interrupt (Input, negative edge triggered). \overline{NMI} demands a higher priority than \overline{INT} and is al-

Table 4. Multiplexed Pin Descriptions

A18/TOUT	During RESET, this pin is initialized as A18. If either the TOC1 or the TOC0 bit of the Timer Control register (TCR) is set to 1, the T _{OUT} function is selected. If TOC1 and TOC0 are cleared to 0, the A18 function is selected.
CKA0/ $\overline{\text{DREQ0}}$	During RESET, this pin is initialized as CKA0. If either DM1 or SM1 in the DMA Mode register (DMODE) is set to 1, the $\overline{\text{DREQ0}}$ function is selected.
CKA1/ $\overline{\text{TEND0}}$	During RESET, this pin is initialized as CKA1. If the CKA1D bit in ASCI control register ch1 (CNTLA1) is set to 1, the $\overline{\text{TEND0}}$ function is selected. If the CKA1D bit is set to 0, the CKA1 function is selected.
RXS/ $\overline{\text{CTS1}}$	During RESET, this pin is initialized as RXS. If the CTS1E bit in the ASCI status register ch1 (STAT1) is set to 1, the $\overline{\text{CTS1}}$ function is selected. If the CTS1E bit is set to 0, the RXS function is selected.



Figure 5. Timer Initialization, Count Down, and Reload Timing

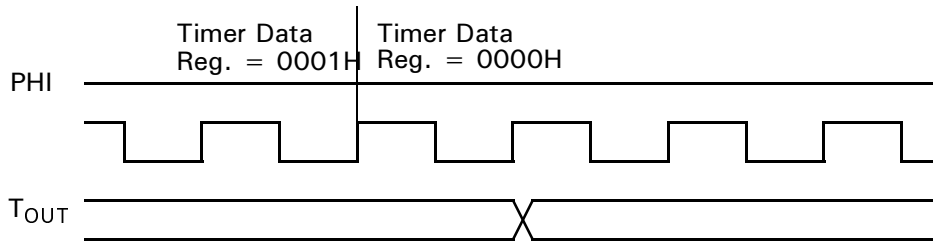


Figure 6. Timer Output Timing

Clocked Serial I/O (CSI/O). The CSI/O channel provides a half-duplex serial transmitter and receiver. This channel can be used for simple high-speed data connection to another microprocessor or microcomputer. TRDR is used for both CSI/O transmission and reception. Thus, the system design must ensure that the constraints of half-duplex operation are met (Transmit and Receive operation cannot occur simultaneously). For example, if a CSI/O transmission is attempted while the CSI/O is receiving data, a CSI/O does not work.

Note: TRDR is not buffered. Performing a CSI/O transmit while the previous transmission is still in progress causes the data to be immediately updated and corrupts the transmit operation. Similarly, reading TRDR while a transmit or receive is in progress should be avoided.

ARCHITECTURE (Continued)



Figure 7. CSI/O Block Diagram

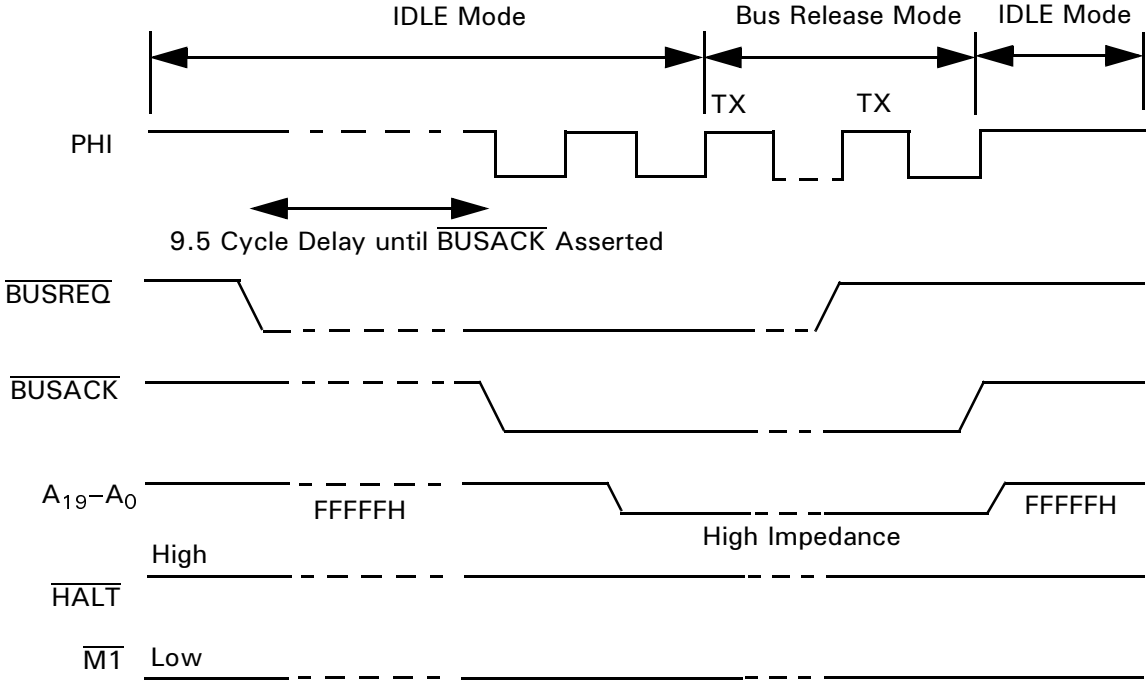


Figure 16. Bus Granting to External Master in IDLE Mode

STANDBY Mode (With or Without QUICK RECOVERY).

Software can put the Z8S180/Z8L180 into this mode by setting the IOSTOP bit (ICR5) to 1, CCR6 to 1, and executing the SLP instruction. This mode stops the on-chip oscillator and thus draws the least power of any mode, less than 10µA.

As with IDLE mode, the Z8S180/Z8L180 leaves STANDBY mode in response to a Low on $\overline{\text{RESET}}$, on $\overline{\text{NMI}}$, or a Low on $\overline{\text{INT0-2}}$ that is enabled by a 1 in the corresponding bit in the INT/TRAP Control Register. This action grants the bus to an external Master if the BREXT bit in the CPU Control Register (CCR5) is 1. The time required for all of these operations is greatly increased by the necessity for restarting the on-chip oscillator, and ensuring that it stabilizes to square-wave operation.

When an external clock is connected to the EXTAL pin rather than a crystal to the XTAL and EXTAL pins and the external clock runs continuously, there is little necessity to use STANDBY mode because no time is required to restart the oscillator, and other modes restart faster. However, if external logic stops the clock during STANDBY mode (for example, by decoding $\overline{\text{HALT}}$ Low and $\overline{\text{M1}}$ High for several clock cycles), then STANDBY mode can be useful to allow the external clock source to stabilize after it is re-enabled.

When external logic drives $\overline{\text{RESET}}$ Low to bring the device out of STANDBY mode, and a crystal is in use or an external clock source is stopped, the external logic must hold $\overline{\text{RESET}}$ Low until the on-chip oscillator or external clock source is restarted and stabilized.

The clock-stability requirements of the Z8S180/Z8L180 are much less in the divide-by-two mode that is selected by a RESET sequence and controlled by the Clock Divide bit in the CPU Control Register (CCR7). As a result, software performs the following actions:

1. Sets CCR7 to 0 for divide-by-two mode before an SLP instruction and STANDBY mode.
2. Delays setting CCR7 back to 1 for divide-by-one mode as long as possible to allow additional clock stabilization time after a RESET, interrupt, or in-line RESTART after an SLP 01 instruction.

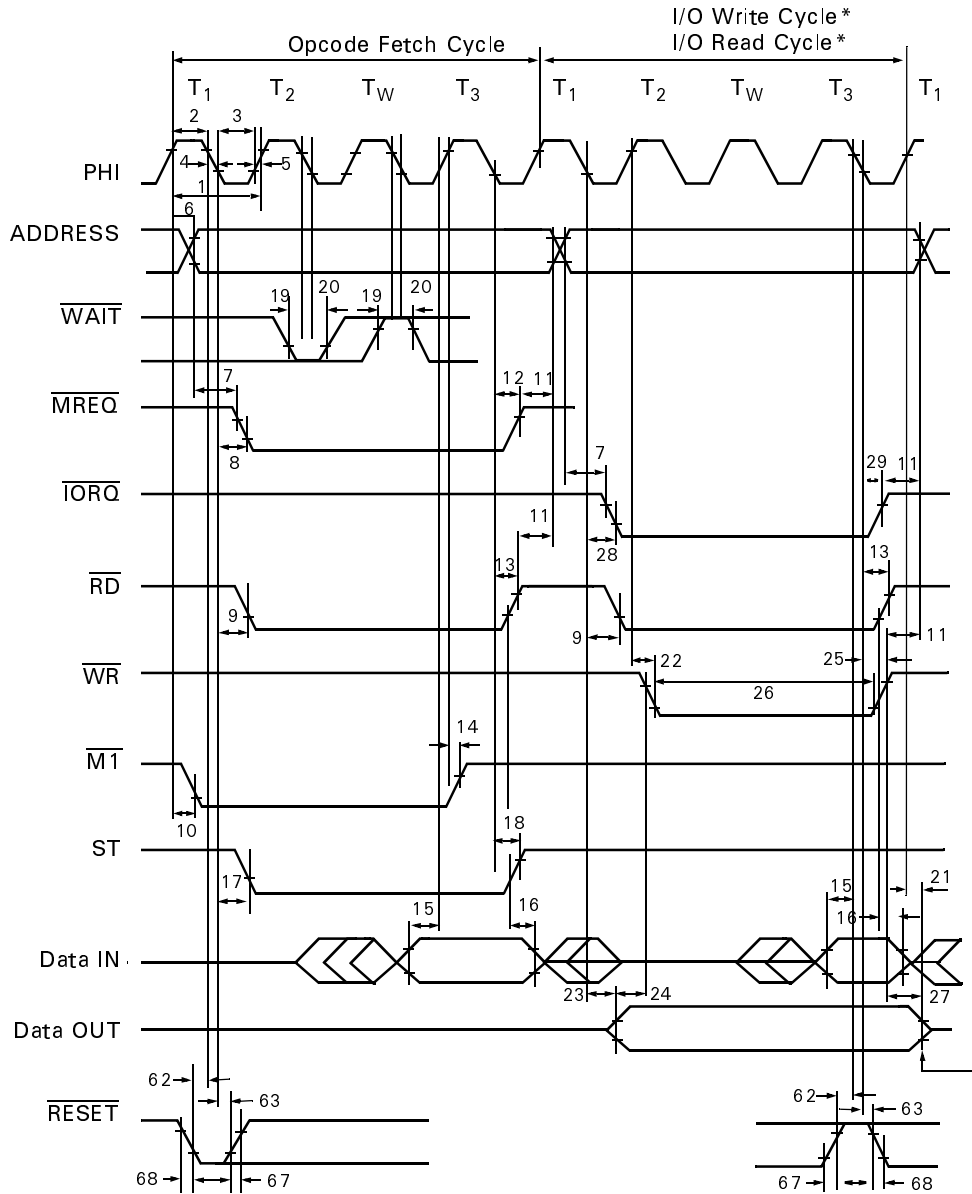
If CCR6 is set to 1 before the SLP instruction places the MPU in STANDBY mode, the value of the CCR3 bit determines the length of the delay before the oscillator restarts and stabilizes when it leaves STANDBY mode due to an external interrupt request. When CCR3 is 0, the Z8S180/Z8L180 waits 2^{17} (131,072) clock cycles. When CCR3 is 1, it waits 64 clock cycles. This state is called QUICK RECOVERY mode. The same delay applies to grant-

AC CHARACTERISTICS—Z8S180 (Continued)

Table 8. Z8S180 AC Characteristics (Continued)
 $V_{DD} = 5V \pm 10\%$ or $V_{DD} = 3.3V \pm 10\%$; 33-MHz Characteristics Apply Only to 5V Operation

Number	Symbol	Item	Z8S180—20 MHz		Z8S180—33 MHz		Unit
			Min	Max	Min	Max	
32	t_{INTH}	\overline{INT} Hold Time from PHI Fall	10	—	10	—	ns
33	t_{NMIW}	\overline{NMI} Pulse Width	35	—	25	—	ns
34	t_{BRS}	\overline{BUSREQ} Set-up Time to PHI Fall	10	—	10	—	ns
35	t_{BRH}	\overline{BUSREQ} Hold Time from PHI Fall	10	—	10	—	ns
36	t_{BAD1}	PHI Rise to \overline{BUSACK} Fall Delay	—	25	—	15	ns
37	t_{BAD2}	PHI Fall to \overline{BUSACK} Rise Delay	—	25	—	15	ns
38	t_{BZD}	PHI Rise to Bus Floating Delay Time	—	40	—	30	ns
39	t_{MEWH}	\overline{MREQ} Pulse Width (High)	35	—	25	—	ns
40	t_{MEWL}	\overline{MREQ} Pulse Width (Low)	35	—	25	—	ns
41	t_{RFD1}	PHI Rise to \overline{RFSH} Fall Delay	—	20	—	15	ns
42	t_{RFD2}	PHI Rise to \overline{RFSH} Rise Delay	—	20	—	15	ns
43	t_{HAD1}	PHI Rise to \overline{HALT} Fall Delay	—	15	—	15	ns
44	t_{HAD2}	PHI Rise to \overline{HALT} Rise Delay	—	15	—	15	ns
45	t_{DROS}	$\overline{DREQ1}$ Set-up Time to PHI Rise	20	—	15	—	ns
46	t_{DROH}	$\overline{DREQ1}$ Hold Time from PHI Rise	20	—	15	—	ns
47	t_{TED1}	PHI Fall to \overline{TENDi} Fall Delay	—	25	—	15	ns
48	t_{TED2}	PHI Fall to \overline{TENDi} Rise Delay	—	25	—	15	ns
49	t_{ED1}	PHI Rise to E Rise Delay	—	30	—	15	ns
50	t_{ED2}	PHI Fall or Rise to E Fall Delay	—	30	—	15	ns
51	P_{WEH}	E Pulse Width (High)	25	—	20	—	ns
52	P_{WEL}	E Pulse Width (Low)	50	—	40	—	ns
53	t_{Er}	Enable Rise Time	—	10	—	10	ns
54	t_{Ef}	Enable Fall Time	—	10	—	10	ns
55	t_{TOD}	PHI Fall to Timer Output Delay	—	75	—	50	ns
56	t_{STDI}	CSI/O Transmit Data Delay Time (Internal Clock Operation)	—	2	—	2	tcyc
57	t_{STDE}	CSI/O Transmit Data Delay Time (External Clock Operation)	—	$7.5 t_{CYC} + 75$	—	$75 t_{CYC} + 60$	ns
58	t_{SRSI}	CSI/O Receive Data Set-up Time (Internal Clock Operation)	1	—	1	—	tcyc
59	t_{SRHI}	CSI/O Receive Data Hold Time (Internal Clock Operation)	1	—	1	—	tcyc
60	t_{SRSE}	CSI/O Receive Data Set-up Time (External Clock Operation)	1	—	1	—	tcyc
61	t_{SRHE}	CSI/O Receive Data Hold Time (External Clock Operation)	1	—	1	—	tcyc
62	t_{RES}	\overline{RESET} Set-up Time to PHI Fall	40	—	25	—	ns

TIMING DIAGRAMS



Note: *Memory Read/Write Cycle timing is the same as I/O Read/Write Cycle except there are no automatic wait states (T_W), and \overline{MREQ} is active instead of \overline{IORQ} .

Figure 20. CPU Timing
(Opcode Fetch Cycle, Memory Read Cycle,
Memory Write Cycle, I/O Write Cycle, I/O Read Cycle)

ASCII REGISTER DESCRIPTION

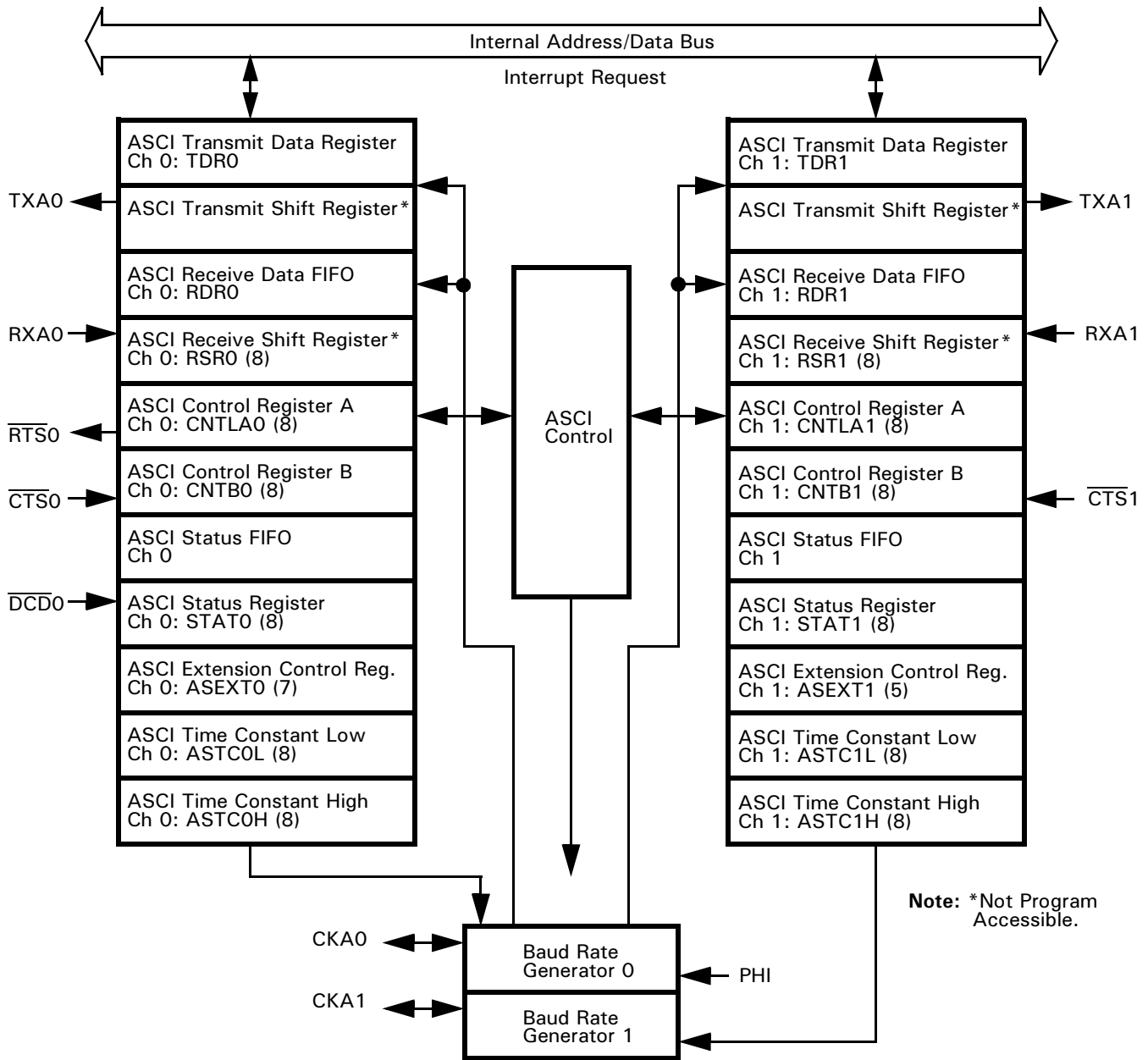


Figure 32. ASCII Block Diagram

ASCII Transmit Shift Register 0,1. When the ASCII Transmit Shift Register (TSR) receives data from the ASCII Transmit Data Register (TDR), the data is shifted out to the TXA pin. When transmission is completed, the next byte (if available) is automatically loaded from TDR into TSR and the next transmission starts. If no data is available for trans-

mission, TSR idles by outputting a continuous High level. This register is not program-accessible

ASCII Transmit Data Register 0,1 (TDR0, 1: I/O address = 06H, 07H). Data written to the ASCII Transmit Data Register is transferred to the TSR as soon as TSR is empty. Data can be written while TSR is shifting out the previous byte of data. Thus, the ASCII transmitter is double buffered.

Data can be written into and read from the ASCII Transmit Data Register. If data is read from the ASCII Transmit Data Register, the ASCII data transmit operation is not affected by this READ operation.

ASCII Receive Shift Register 0,1 (RSR0,1). This register receives data shifted in on the RXA pin. When full, data is automatically transferred to the ASCII Receive Data Register (RDR) if it is empty. If RSR is not empty when the next incoming data byte is shifted in, an overrun error occurs. This register is not program accessible.

ASCII Receive Data FIFO 0,1 (RDR0, 1:I/O Address = 08H, 09H). The ASCII Receive Data Register is a read-only register. When a complete incoming data byte is assembled in RSR, it is automatically transferred to the 4 character Receive Data First-In First-Out (FIFO) memory. The oldest character in the FIFO (if any) can be read from the Receive Data Register (RDR). The next incoming data byte can be shifted into RSR while the FIFO is full. Thus, the ASCII receiver is well buffered.

ASCII STATUS FIFO

This four-entry FIFO contains Parity Error, Framing Error, Rx Overrun, and Break status bits associated with each character in the receive data FIFO. The status of the oldest character (if any) can be read from the ASCII status registers.

acter in the receive data FIFO. The status of the oldest character (if any) can be read from the ASCII status registers.

ASCII CHANNEL CONTROL REGISTER A

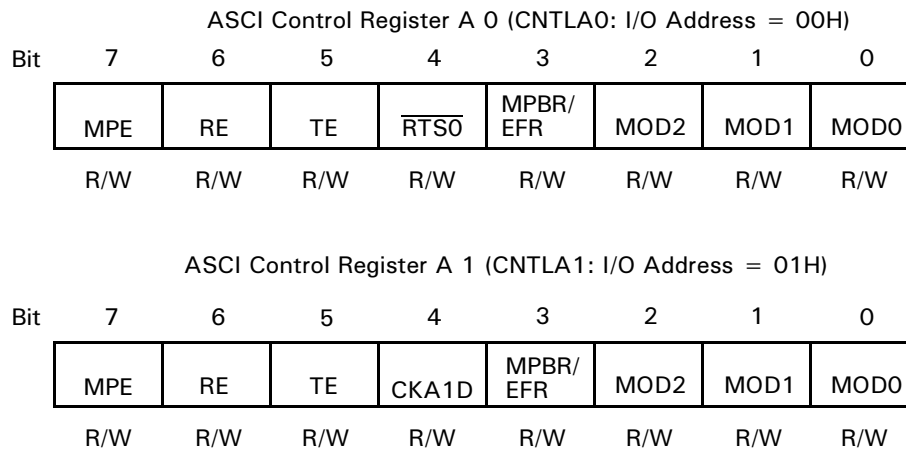


Figure 33. ASCII Channel Control Register A

MPE: Multi-Processor Mode Enable (Bit 7). The ASCII features a multiprocessor communication mode that utilizes an extra data bit for selective communication when a number of processors share a common serial bus. Multiprocessor data format is selected when the MP bit in CNTLB is set to 1. If multiprocessor mode is not selected (MP bit in CNTLB = 0), MPE has no effect. If multiprocessor mode is selected, MPE enables or disables the *wake-up* feature as follows. If MBE is set to 1, only received bytes in which the multiprocessor bit (MPB) = 1 can affect the RDRF and error flags. Effectively, other bytes (with MPB = 0) are *ignored* by the ASCII. If MPE is reset to 0, all bytes, regardless of

the state of the MPB data bit, affect the REDR and error flags. MPE is cleared to 0 during RESET.

RE: Receiver Enable (Bit 6). When RE is set to 1, the ASCII transmitter is enabled. When TE is reset to 0, the transmitter is disabled and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the previous contents of TDRE are held. TE is cleared to 0 in IOSTOP mode during RESET.

TE: Transmitter Enable (Bit 5). When TE is set to 1, the ASCII receiver is enabled. When $\overline{\text{TE}}$ is reset to 0, the transmitter is disabled and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the pre-

ASCII STATUS REGISTER 0,1

Each ASCII channel status register (STAT0,1) allows interrogation of ASCII communication, error and modem control

signal status, and the enabling or disabling of ASCII interrupts.

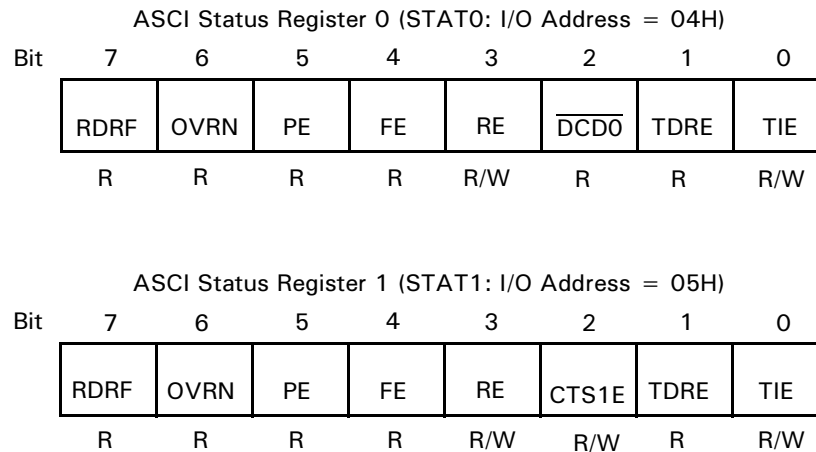


Figure 35. ASCII Status Registers

RDRF: Receive Data Register Full (Bit 7). RDRF is set to 1 when an incoming data byte is loaded into an empty Rx FIFO. If a framing or parity error occurs, RDRF is still set and the receive data (which generated the error) is still loaded into the FIFO. RDRF is cleared to 0 by reading RDR and most recently received character in the FIFO from IOSTOP mode, during RESET and for ASCII0 if the $\overline{\text{DCD0}}$ input is auto-enabled and is negated (High).

OVRN: Overrun Error (Bit 6). An overrun condition occurs if the receiver finishes assembling a character but the Rx FIFO is full so there is no room for the character. However, this status bit is not set until the most recent character received before the overrun becomes the oldest byte in the FIFO. This bit is cleared when software writes a 1 to the EFR bit in the CNTLA register. The bit may also be cleared by RESET in IOSTOP mode or ASCII0 if the $\overline{\text{DCD0}}$ pin is auto enabled and is negated (High).

Note: When an overrun occurs, the receiver does not place the character in the shift register into the FIFO, nor any subsequent characters, until the most recent good character enters the top of the FIFO so that OVRN is set. Software then writes a 1 to EFR to clear it.

PE: Parity Error (Bit 5). A parity error is detected when parity checking is enabled. When the MOD1 bit in the

CNTLA register is 1, a character is assembled in which the parity does not match the PEO bit in the CNTLB register. However, this status bit is not set until or unless the error character becomes the oldest one in the Rx FIFO. PE is cleared when software writes a 1 to the EFR bit in the CNTRLA register. PE is also cleared by RESET in IOSTOP mode, or on ASCII0, if the $\overline{\text{DCD0}}$ pin is auto-enabled and is negated (High).

FE: Framing Error (Bit 4). A framing error is detected when the stop bit of a character is sampled as 0/SPACE. However, this status bit is not set until/unless the error character becomes the oldest one in the Rx FIFO. FE is cleared when software writes a 1 to the EFR bit in the CNTLA register. FE is also cleared by RESET in IOSTOP mode, or on ASCII0, if the $\overline{\text{DCD0}}$ pin is auto-enabled and is negated (High).

REI: Receive Interrupt Enable (Bit 3). RIE should be set to 1 to enable ASCII receive interrupt requests. When RIE is 1, the Receiver requests an interrupt when a character is received and RDRF is set, but only if neither DMA channel requires its request-routing field to be set to receive data from this ASCII. That is, if SM1-0 are 11 and SAR17-16 are 10, or DIM1 is 1 and IAR17-16 are 10, then ASCII1 does not request an interrupt for RDRF. If RIE is 1, either ASCII requests an interrupt when OVRN, PE or FE is set, and

never both set to 1 at the same time. TE is cleared to 0 during RESET and IOSTOP mode.

SS2, 1, 0: Speed Select 2, 1, 0 (Bits 2–0). SS2, SS1 and SS0 select the CSI/O transmit/receive clock source and speed. SS2, SS1 and SS0 are all set to 1 during RESET. Table 11 indicates CSI/O Baud Rate Selection.

Table 11. CSI/O Baud Rate Selection

SS2	SS1	SS0	Divide Ratio
0	0	0	÷20
0	0	1	÷40
0	1	0	÷80
0	1	1	÷160
1	0	0	÷320
1	0	1	÷640
1	1	0	÷1280
1	1	1	External Clock Input (Less Than ÷20)

After RESET, the CKS pin is configured as an external clock input (SS2, SS1, SS0 = 1). Changing these values causes CKS to become an output pin and the selected clock is output when transmit or receive operations are enabled.

CSI/O Transmit/Receive Data Register

Mnemonic TRDR
Address 0BH



Figure 41. CSI/O Transmit/Receive Data Register

Timer Data Register Channel 0 Low

Mnemonic TMDROL
Address 0CH



Figure 42. Timer Register Channel 0 Low

Timer Data Register Channel 0H

Mnemonic TMDROH
Address 0DH

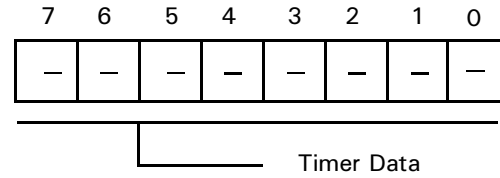


Figure 43. Timer Data Register Channel 0 High

Timer Reload Register Channel 0 Low

Mnemonic RLDR0L
Address 0EH

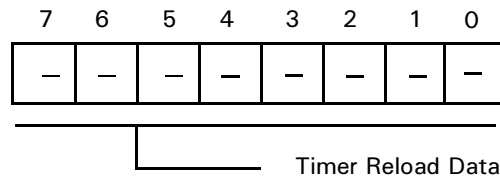


Figure 44. Timer Reload Register Low

Timer Reload Register Channel 0 High

Mnemonic RLDR0H
Address 0FH

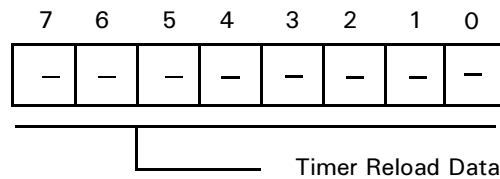


Figure 45. Timer Reload Register Channel 0 High

ASCI EXTENSION CONTROL REGISTER CHANNEL 0 AND CHANNEL 1

The ASCII Extension Control Registers (ASEXT0 and ASEXT1) control functions that have been added to the

ASCI in the Z8S180/Z8L180 family. All bits in this register reset to 0.

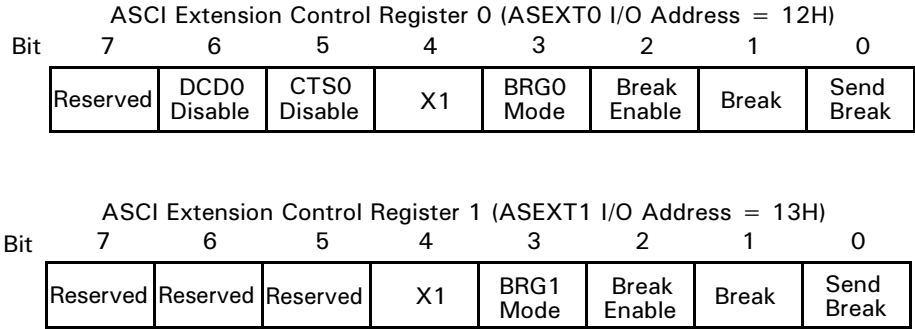


Figure 47. ASCII Extension Control Registers, Channels 0 and 1

DCD0 Disable (Bit 6, ASCIO Only). If this bit is 0, then the $\overline{\text{DCD0}}$ pin auto-enables the ASCIO receiver, such that when the pin is negated/High, the Receiver is held in a RESET state. If this bit is 1, the state of the $\overline{\text{DCD}}$ -pin has no effect on receiver operation. In either state of this bit, software can read the state of the $\overline{\text{DCD0}}$ pin in the STAT0 register, and the receiver interrupts on a rising edge of $\overline{\text{DCD0}}$.

CTS0 Disable (Bit 5, ASCIO Only). If this bit is 0, then the $\overline{\text{CTS0}}$ pin auto-enables the ASCIO transmitter, in that when the pin is negated/High, the TDRE bit in the STAT0 register is forced to 0. If this bit is 1, the state of the $\overline{\text{CTS0}}$ pin has no effect on the transmitter. Regardless of the state of this bit, software can read the state of the $\overline{\text{CTS0}}$ pin the CNTLBO register.

X1 (Bit 4). If this bit is 1, the clock from the Baud Rate Generator or CKA pin is taken as a 1X-bit clock (sometimes called *isochronous mode*). In this mode, receive data on the RXA pin must be synchronized to the clock on the CKA pin, regardless of whether CKA is an input or an output. If this bit is 0, the clock from the Baud Rate Generator or CKA pin is divided by 16 or 64 per the DR bit in the CNTLB register, to obtain the actual bit rate. In this mode, receive data on the RXA pin is not required to be synchronized to a clock.

BRG Mode (Bit 3). If the SS2-0 bits in the CNTLB register are not 111, and this bit is 0, the ASCII Baud Rate Generator

divides PHI by 10 or 30, depending on the PS bit in CNTLB, and factored by a power of two (selected by the SS2-0 bits), to obtain the clock that is presented to the transmitter and receiver and output on the CKA pin. If SS2-0 are not 111, and this bit is 1, the Baud Rate Generator divides PHI by twice the sum of the 16-bit value (programmed into the Time Constant registers) and 2. This mode is identical to the operation of the baud rate generator in the ESCC.

Break Enable (Bit 2). If this bit is 1, the receiver detects BREAK conditions and report them in bit 1, and the transmitter sends BREAKs under the control of bit 0.

Break Detect (Bit 1). The receiver sets this read-only bit to 1 when an all-zero character with a Framing Error becomes the oldest character in the Rx FIFO. The bit is cleared when software writes a 0 to the EFR bit in CNTLA register, also by RESET, by IOSTOP mode, and for ASCIO, if the $\overline{\text{DCD0}}$ pin is auto-enabled and is negated (High).

Send Break (Bit 0). If this bit and bit 2 are both 1, the transmitter holds the TXA pin Low to send a BREAK condition. The duration of the BREAK is under software control (one of the PRTs or CTCs can be used to time it). This bit resets to 0, in which state TXA carries the serial output of the transmitter.

CLOCK MULTIPLIER REGISTER

(Z180 MPU Address 1EH)

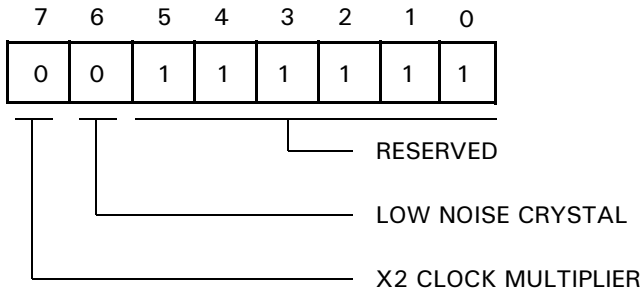


Figure 54. Clock Multiplier Register

Bit 7. X2 Clock Multiplier Mode. When this bit is set to 1, the programmer can double the internal clock speed from the speed of the external clock. This feature only operates effectively with frequencies of 10–16 MHz (20–32 MHz internal). When this bit is set to 0, the Z8S180/Z8L180 device operates in normal mode. At power-up, this feature is disabled.

Bit 6. Low Noise Crystal Option. Setting this bit to 1 enables the low-noise option for the EXTAL and XTAL pins. This option reduces the gain in addition to reducing the output drive capability to 30% of its original drive capability. The Low Noise Crystal Option is recommended in the use of crystals for PCMCIA applications, where the crystal may be driven too hard by the oscillator. Setting this bit to 0 is selected for normal operation of the EXTAL and XTAL pins. The default for this bit is 0.

Note: Operating restrictions for device operation are listed below. If a low-noise option is required, and normal device operation is required, use the clock multiplier feature.

Table 13. Low Noise Option

Low Noise ADDR 1E, bit 6 = 1	Normal ADDR 1E, bit 6 = 0
20 MHz @ 4.5V, 100°C	33 MHz @ 4.5V, 100°C
10 MHz @ 3.0V, 100°C	20 MHz @ 3.0V, 100°C

DMA BYTE COUNT REGISTER CHANNEL 0

The DMA Byte Count Register Channel 0 specifies the number of bytes to be transferred. This register contains 16 bits and may specify up to 64-KB transfers. When one byte is transferred, the register is decremented by one. If n bytes should be transferred, n must be stored before the DMA operation.

Note: All DMA Count Register channels are undefined during RESET.

DMA Byte Count Register Channel 0 Low

Mnemonic BCR0L
Address 26H



Figure 61. DMA Byte Count Register 0 Low

DMA Byte Count Register Channel 0 High

Mnemonic BCR0H
Address 27H

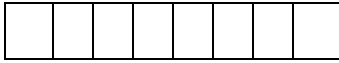


Figure 62. DMA Byte Count Register 0 High

DMA Byte Count Register Channel 1 Low

Mnemonic BCR1L
Address 2EH



Figure 63. DMA Byte Count Register 1 Low

DMA Byte Count Register Channel 1 High

Mnemonic BCR1H
Address 2FH



Figure 64. DMA Byte Count Register 1 High

MMU COMMON BASE REGISTER

The Common Base Register (CBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical

address for Common Area 1 accesses. All bits of CBR are reset to 0 during RESET.

MMU Common Base Register

Mnemonic CBR
Address 38H

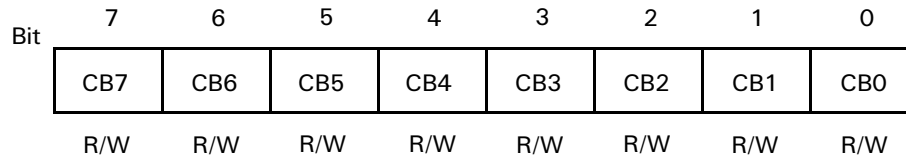


Figure 78. MMU Common Base Register (CBR: I/O Address = 38H)

MMU BANK BASE REGISTER

The Bank Base Register (BBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical ad-

dress for Bank Area accesses. All bits of BBR are reset to 0 during RESET.

MMU Bank Base Register

Mnemonic BBR
Address 39H

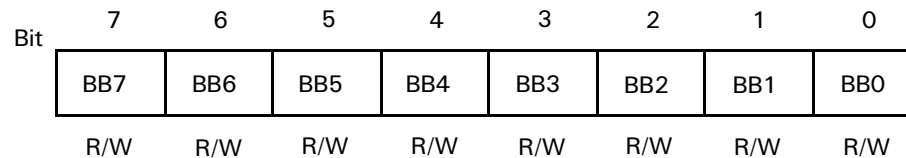


Figure 79. MMU Bank Base Register (BBR: I/O Address = 39H)

MMU COMMON/BANK AREA REGISTER

The Common/Bank Area Register (CBAR) specifies boundaries within the Z8S180/Z8L180 64-KB logical address

space for up to three areas; Common Area), Bank Area and Common Area 1.

MMU Common/Bank Area Register

Mnemonic CBAR
Address 3AH

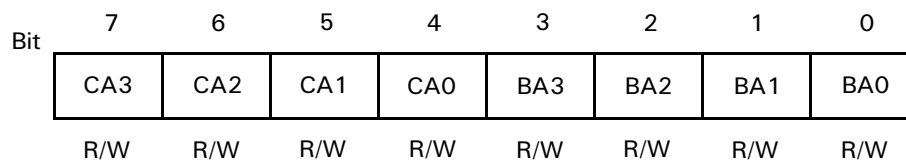


Figure 80. MMU Common/Bank Area Register (CBAR: I/O Address = 3AH)

CA3–CA0:CA (Bits 7–4). CA specifies the start (Low) address (on 4-KB boundaries) for Common Area 1. This condition also determines the most recent address of the Bank Area. All bits of CA are set to 1 during RESET.

BA3–BA0 (Bits 3–0). BA specifies the start (Low) address (on 4-KB boundaries) for the Bank Area. This condition also determines the most recent address of Common Area 0. All bits of BA are set to 1 during RESET.

OPERATION MODE CONTROL REGISTER

The Z8S180/Z8L180 is descended from two different ancestor processors, ZiLOG’s original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR) can be programmed to select between certain differences between the Z80 and the 64180.

Operation Mode Control Register

Mnemonic OMCR
Address 3EH

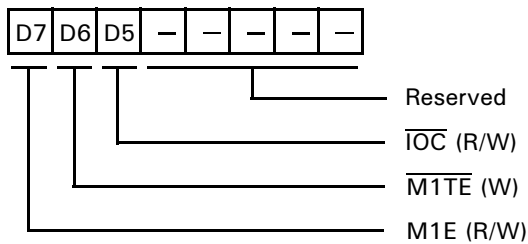


Figure 81. Operating Control Register (OMCR: I/O Address = 3EH)

M1E ($\overline{M1}$ Enable). This bit controls the $\overline{M1}$ output and is set to a 1 during reset.

When $M1E = 1$, the $\overline{M1}$ output is asserted Low during the opcode fetch cycle, the $\overline{INT0}$ acknowledge cycle, and the first machine cycle of the \overline{NMI} acknowledge.

On the Z8S180/Z8L180, this choice makes the processor fetch one RETI instruction. When fetching a RETI from zero-wait-state memory, the processor uses three clock machine cycles that are not fully Z80-timing-compatible.

When $M1E = 0$, the processor does not drive $\overline{M1}$ Low during instruction fetch cycles. After fetching one RETI instruction with normal timing, the processor returns and refetches the instruction using Z80-compatible cycles that drive $\overline{M1}$ Low. This timing compatibility may be required by external Z80 peripherals to properly decode the RETI instruction.

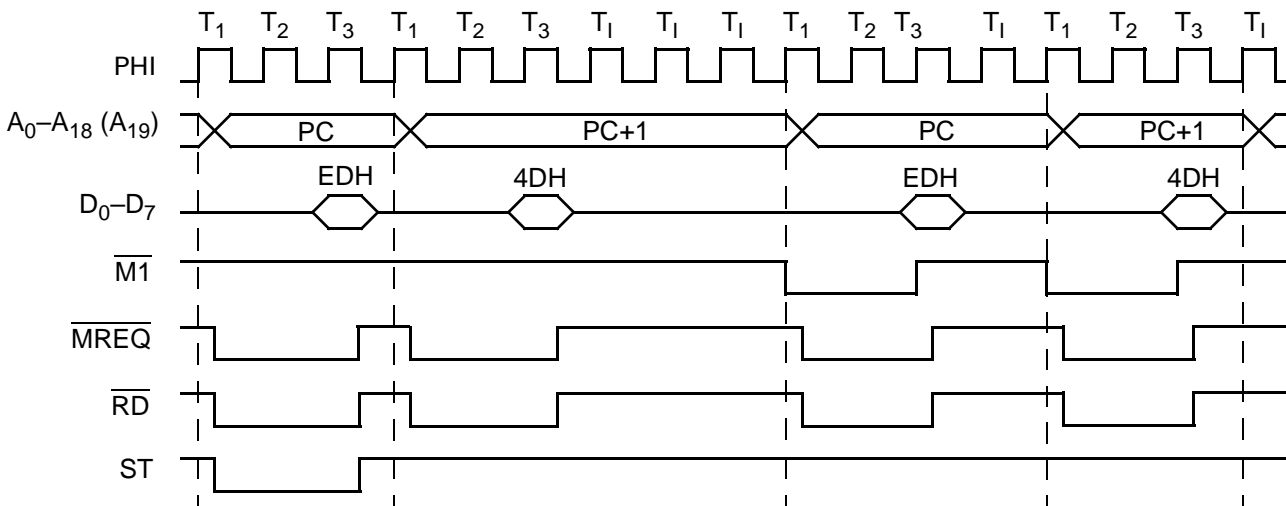


Figure 82. RETI Instruction Sequence with M1E = 0

PACKAGE INFORMATION

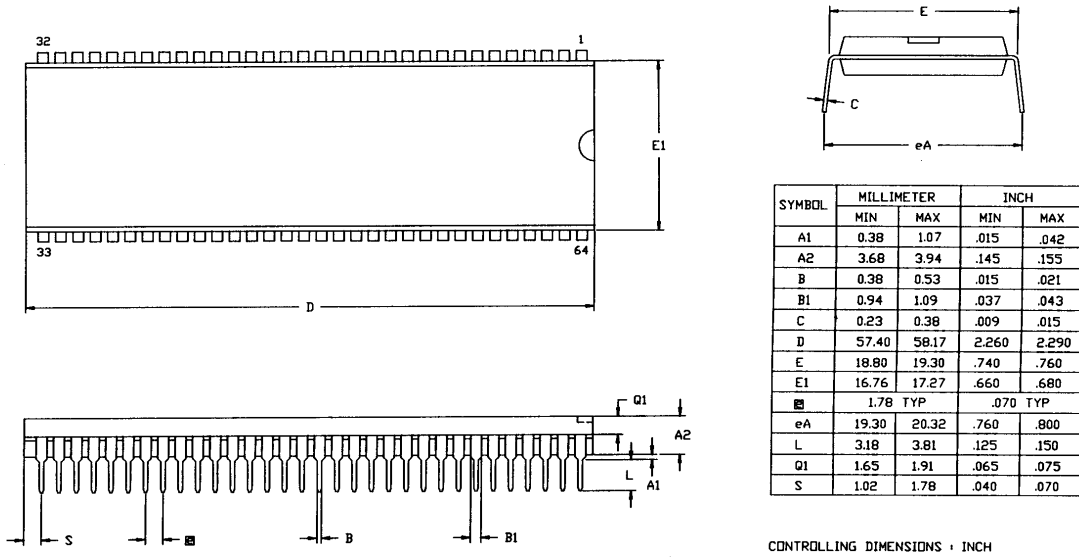


Figure 85. 64-Pin DIP Package Diagram



Figure 86. 80-Pin QFP Package Diagram