Zilog - Z8S18033FEG Datasheet

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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	33MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	-40°C ~ 100°C (TA)
Security Features	-
Package / Case	80-BQFP
Supplier Device Package	80-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8s18033feg

PIN IDENTIFICATION

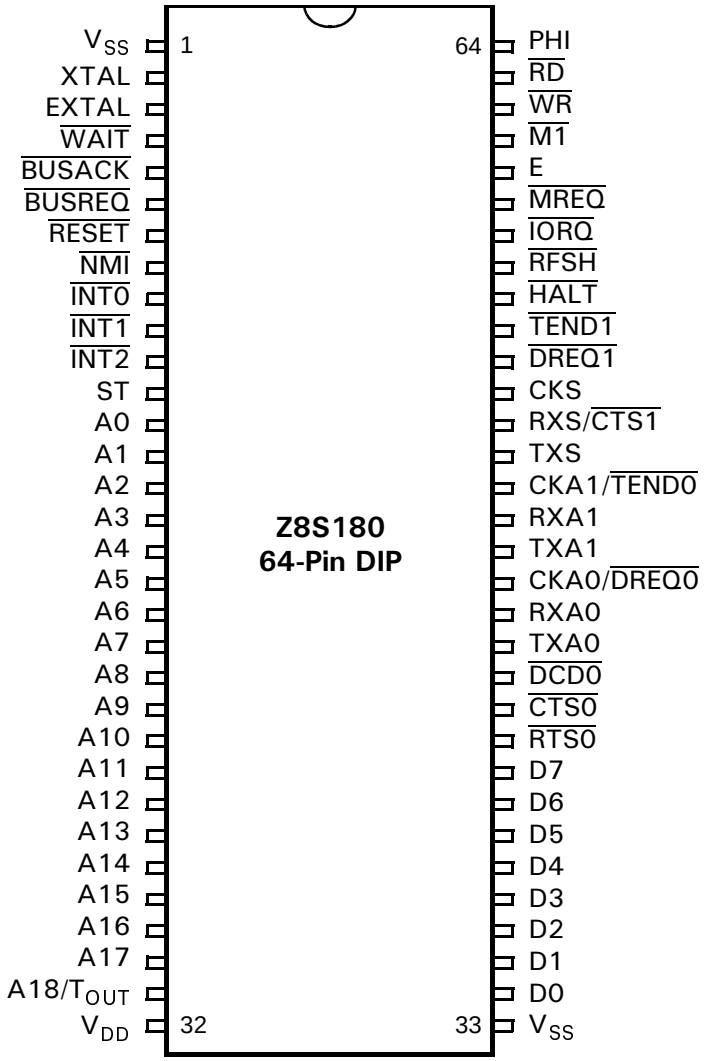


Figure 2. Z8S180 64-Pin DIP Pin Configuration

PIN IDENTIFICATION (Continued)

Table 1. Z8S180/Z8L180 Pin Identification (Continued)

Pin Number and Package Type			Default	Secondary	
QFP	PLCC	DIP	Function	Function	Control
13	19	17	A4		
14			NC		
15	20	18	A5		
16	21	19	A6		
17	22	20	A7		
18	23	21	A8		
19	24	22	A9		
20	25	23	A10		
21	26	24	A11		
22			NC		
23			NC		
24	27	25	A12		
25	28	26	A13		
26	29	27	A14		
27	30	28	A15		
28	31	29	A16		
29	32	30	A17		
30			NC		
31	33	31	A18	T_{OUT}	Bit 2 or Bit 3 of TCR
32	34	32	V_{DD}		
33	35		A19		
34	36	33	V_{SS}		
35	37	34	D0		
36	38	35	D1		
37	39	36	D2		
38	40	37	D3		
39	41	38	D4		
40	42	39	D5		
41	43	40	D6		
42			NC		
43			NC		
44	44	41	D7		
45	45	42	$\overline{RTS0}$		
46	46	43	$\overline{CTS0}$		
47	47	44	$\overline{DCD0}$		
48	48	45	TXA0		
49	49	46	RXA0		
50	50	47	CKA0	$\overline{DREQ0}$	Bit 3 or Bit 5 of DMODE
51			NC		
52	51	48	TXA1		

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
39	41	38	D4		3T	3T	3T
40	42	39	D5		3T	3T	3T
41	43	40	D6		3T	3T	3T
42			NC				
43			NC				
44	44	41	D7		3T	3T	3T
45	45	42	$\overline{RTS0}$		High	OUT	High
46	46	43	$\overline{CTS0}$		IN	OUT	IN
47	47	44	$\overline{DCD0}$		IN	IN	IN
48	48	45	TXA0		High	OUT	OUT
49	49	46	RXA0		IN	IN	IN
50	50	47	CKA0		3T	I/O	I/O
			$\overline{DREQ0}$		N/A	IN	IN
51			NC				
52	51	48	TXA1		High	OUT	OUT
53	52		TEST				
54	53	49	RXA1		IN	IN	IN
55	54	50	CKA1		3T	I/O	I/O
			$\overline{TEND0}$		N/A	High	High
56	55	51	TXS		High	OUT	OUT
57	56	52	RXS		IN	IN	IN
			$\overline{CTS1}$		N/A	IN	IN
58	57	53	CKS		3T	I/O	I/O
59	58	54	$\overline{DREQ1}$		IN	3T	IN
60	59	55	$\overline{TEND1}$		High	OUT	High
61	60	56	$\overline{HALT}$		High	High	Low
62			NC				
63			NC				
64	61	57	$\overline{RFSH}$		High	OUT	High
65	62	58	$\overline{IORQ}$		High	3T	High
66	63	59	$\overline{MREQ}$		High	3T	High
67	64	60	E		Low	OUT	OUT
68	65	61	$\overline{M1}$		High	High	High
69	66	62	$\overline{WR}$		High	3T	High
70	67	63	$\overline{RD}$		High	3T	High
71	68	64	PHI		OUT	OUT	OUT
72	1	1	V_{SS}		GND	GND	GND
73	2		V_{SS}		GND	GND	GND
74	3	2	XTAL		OUT	OUT	OUT
75			NC				

PIN DESCRIPTIONS

A0–A19. Address Bus (Output, 3-state). A0–A19 form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 1 MB) and I/O data bus exchanges (up to 64 KB). The address bus enters a high–impedance state during reset and external bus acknowledge cycles. Address line A18 is multiplexed with the output of PRT channel 1 (T_{OUT}, selected as address output on reset), and address line A19 is not available in DIP versions of the Z8S180.

$\overline{\text{BUSACK}}$. Bus Acknowledge (Output, active Low). $\overline{\text{BUSACK}}$ indicates that the requesting device, the MPU address and data bus, and some control signals enter their high-impedance state.

BUSREQ. Bus Request (Input, active Low). This input is used by external devices (such as DMA controllers) to request access to the system bus. This request demands a higher priority than $\overline{\text{NMI}}$ and is always recognized at the end of the current machine cycle. This signal stops the CPU from executing further instructions, places addresses, data buses, and other control signals into the high-impedance state.

CKA0, CKA1. Asynchronous Clock 0 and 1 (bidirectional). When in output mode, these pins are the transmit and receive clock outputs from the ASCI baud rate generators. When in input mode, these pins serve as the external clock inputs for the ASCI baud rate generators. CKA0 is multiplexed with $\overline{\text{DREQ0}}$, and CKA1 is multiplexed with $\overline{\text{TEND0}}$.

CKS. Serial Clock (bidirectional). This line is the clock for the CSI/O channel.

$\overline{\text{CTS0}}$–$\overline{\text{CTS1}}$. Clear to send 0 and 1 (Inputs, active Low). These lines are modem control signals for the ASCI channels. $\overline{\text{CTS1}}$ is multiplexed with RXS.

D0–D7. Data Bus = (bidirectional, 3-state). D0–D7 constitute an 8-bit bidirectional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high-impedance state during reset and external bus acknowledge cycles.

$\overline{\text{DCD0}}$. Data Carrier Detect 0 (Input, active Low); a programmable modem control signal for ASCI channel 0.

$\overline{\text{DREQ0}}$, $\overline{\text{DREQ1}}$. DMA Request 0 and 1 (Input, active Low). $\overline{\text{DREQ}}$ is used to request a DMA transfer from one of the on-chip DMA channels. The DMA channels monitor these inputs to determine when an external device is ready for a READ or WRITE operation. These inputs can be programmed to be either level or edge sensed. $\overline{\text{DREQ0}}$ is multiplexed with CKA0.

E. Enable Clock (Output). This pin functions as a synchronous, machine-cycle clock output during bus transactions.

EXTAL. External Clock Crystal (Input). Crystal oscillator connections. An external clock can be input to the Z8S180/Z8L180 on this pin when a crystal is not used. This input is Schmitt triggered.

$\overline{\text{HALT}}$. HALT/SLEEP (Output, active Low). This output is asserted after the CPU executes either the HALT or SLEEP instruction and is waiting for either a nonmaskable or a maskable interrupt before operation can resume. It is also used with the $\overline{\text{M1}}$ and ST signals to decode the status of the CPU machine cycle.

$\overline{\text{INT0}}$. Maskable Interrupt Request 0 (Input, active Low). This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the $\overline{\text{NMI}}$ and $\overline{\text{BUSREQ}}$ signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$ signals become active.

$\overline{\text{INT1}}$, $\overline{\text{INT2}}$. Maskable Interrupt Request 1 and 2 (Inputs, active Low). This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the $\overline{\text{NMI}}$, $\overline{\text{BUSREQ}}$, and $\overline{\text{INT0}}$ signals are inactive. The CPU acknowledges these requests with an interrupt acknowledge cycle. Unlike the acknowledgment for $\overline{\text{INT0}}$, neither the $\overline{\text{M1}}$ or $\overline{\text{IORQ}}$ signals become active during this cycle.

$\overline{\text{IORQ}}$. I/O Request (Output, active Low, 3-state). $\overline{\text{IORQ}}$ indicates that the address bus contains a valid I/O address for an I/O READ or I/O WRITE operation. $\overline{\text{IORQ}}$ is also generated, along with $\overline{\text{M1}}$, during the acknowledgment of the $\overline{\text{INT0}}$ input signal to indicate that an interrupt response vector can be place onto the data bus. This signal is analogous to the $\overline{\text{IOE}}$ signal of the Z64180.

$\overline{\text{M1}}$. Machine Cycle 1 (Output, active Low). Together with $\overline{\text{MREQ}}$, $\overline{\text{M1}}$ indicates that the current cycle is the opcode-fetch cycle of instruction execution. Together with $\overline{\text{IORQ}}$, $\overline{\text{M1}}$ indicates that the current cycle is for interrupt acknowledgment. It is also used with the $\overline{\text{HALT}}$ and ST signal to decode the status of the CPU machine cycle. This signal is analogous to the $\overline{\text{LIR}}$ signal of the Z64180.

$\overline{\text{MREQ}}$. Memory Request (Output, active Low, 3-state). $\overline{\text{MREQ}}$ indicates that the address bus holds a valid address for a memory READ or memory WRITE operation. This signal is analogous to the $\overline{\text{ME}}$ signal of Z64180.

$\overline{\text{NMI}}$. Nonmaskable Interrupt (Input, negative edge triggered). $\overline{\text{NMI}}$ demands a higher priority than $\overline{\text{INT}}$ and is al-

Table 4. Multiplexed Pin Descriptions

A18/TOUT	During RESET, this pin is initialized as A18. If either the TOC1 or the TOC0 bit of the Timer Control register (TCR) is set to 1, the T_{OUT} function is selected. If TOC1 and TOC0 are cleared to 0, the A18 function is selected.
CKA0/$\overline{\text{DREQ0}}$	During RESET, this pin is initialized as CKA0. If either DM1 or SM1 in the DMA Mode register (DMODE) is set to 1, the $\overline{\text{DREQ0}}$ function is selected.
CKA1/$\overline{\text{TEND0}}$	During RESET, this pin is initialized as CKA1. If the CKA1D bit in ASCI control register ch1 (CNTLA1) is set to 1, the $\overline{\text{TEND0}}$ function is selected. If the CKA1D bit is set to 0, the CKA1 function is selected.
RXS/$\overline{\text{CTS1}}$	During RESET, this pin is initialized as RXS. If the CTS1E bit in the ASCI status register ch1 (STAT1) is set to 1, the $\overline{\text{CTS1}}$ function is selected. If the CTS1E bit is set to 0, the RXS function is selected.

ARCHITECTURE (Continued)

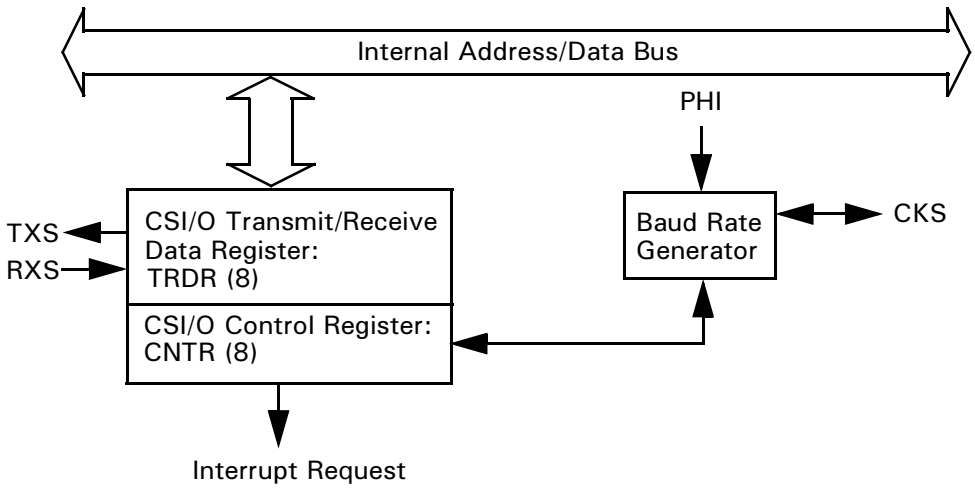


Figure 7. CSI/O Block Diagram

ing the bus to an external Master during STANDBY mode, when the BREXT bit in the CPU Control Register (CCR5) is 1.

As described previously for SLEEP and IDLE modes, when the MPU leaves STANDBY mode due to $\overline{NMI}$ Low or an enabled $\overline{INT0}$–$\overline{INT2}$ Low when the IEF, flag is 1 due to an IE instruction, it starts by performing the interrupt with the return address being that of the instruction following the SLP instruction. If the Z8S180/Z8L180 leaves STANDBY mode due to an external interrupt request that's enabled in the INT/TRAP Control Register, but the IEF, bit is 0 due to a DI instruction, the processor restarts by executing the instruction(s) following the SLP instruction. If $\overline{INT0}$, or $\overline{INT1}$ or $\overline{INT2}$ goes inactive before the end of the clock stabilization delay, the Z8S180/Z8L180 stays in STANDBY mode.

Figure 17 indicates the timing for leaving STANDBY mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes either 64 or 2^{17} (131,072) clocks to restart, depending on the CCR3 bit.

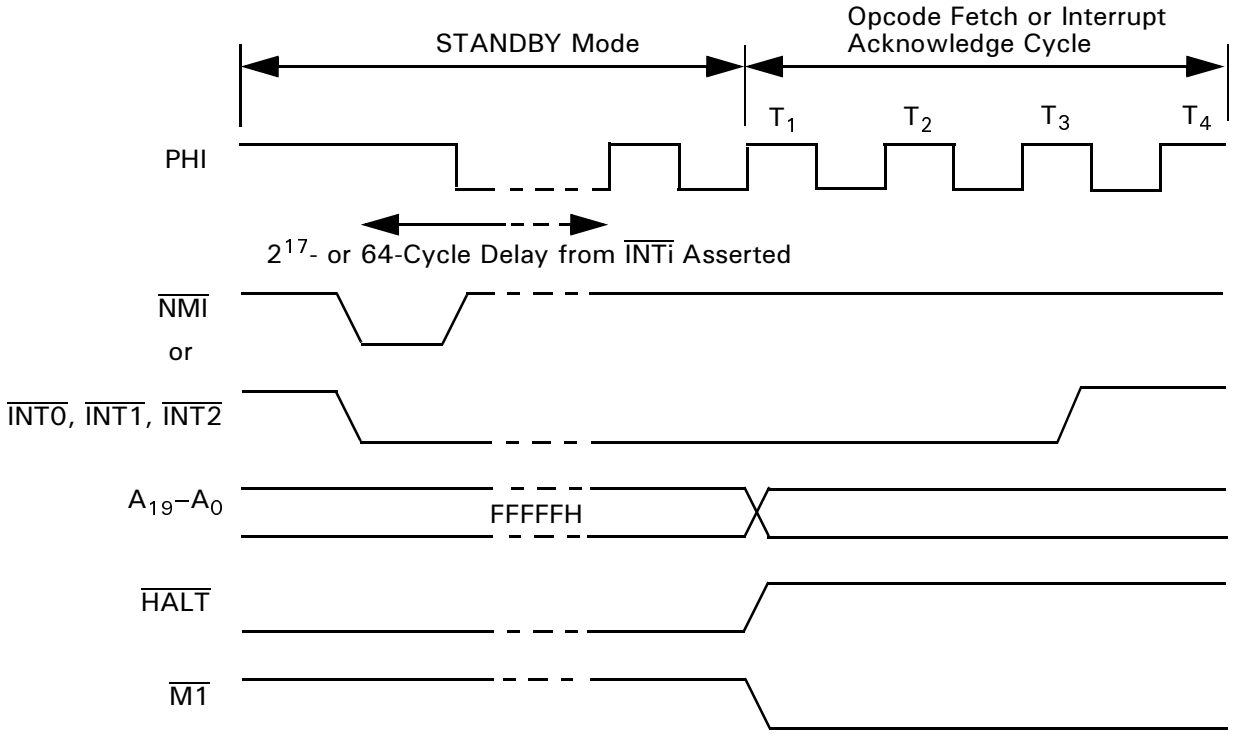


Figure 17. Z8S180/Z8L180 STANDBY Mode Exit Due to External Interrupt

While the Z8S180/Z8L180 is in STANDBY mode, it grants the bus to an external Master if the BREXT bit (CCR5) is 1. Figure 18 indicates the timing of this sequence. The device takes 64 or 2^{17} (131,072) clock cycles to grant the bus depending on the CCR3 bit. The latter (not the QUICK RECOVERY) case may be prohibitive for many demand-driven external Masters. If so, QUICK RECOVERY or IDLE mode can be used.

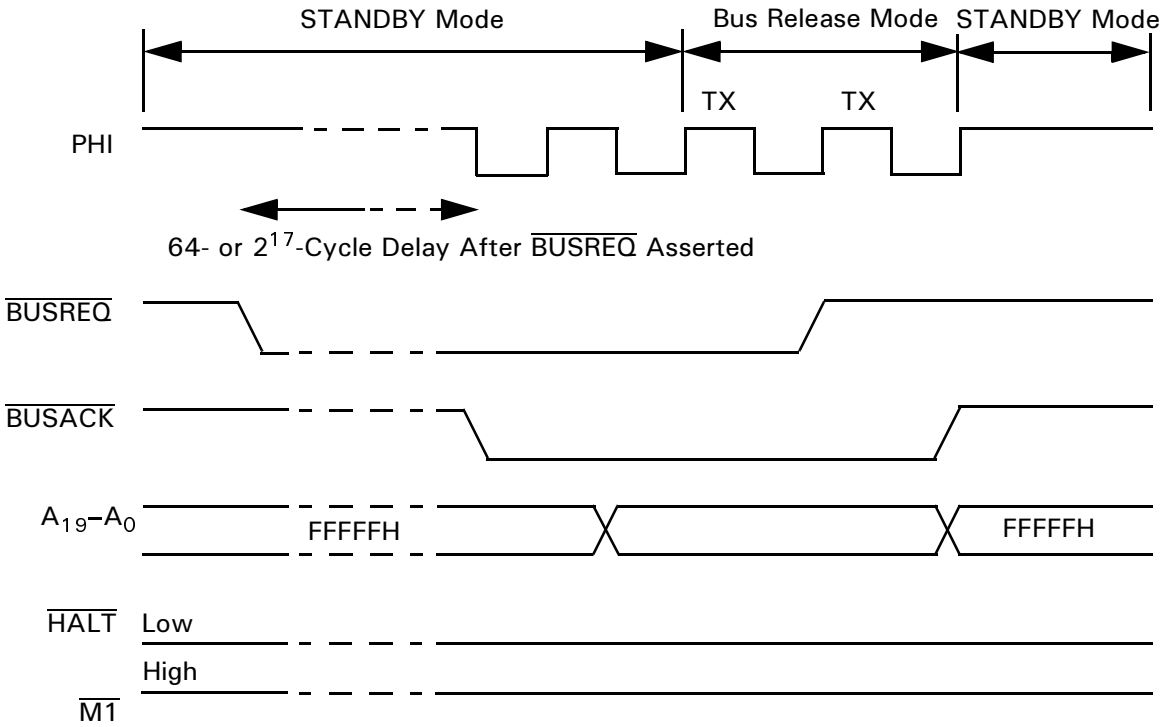


Figure 18. Bus Granting to External Master During STANDBY Mode

STANDARD TEST CONDITIONS

The following standard test conditions apply to DC Characteristics, unless otherwise noted. All voltages are referenced to V_{SS} (0V). Positive current flows into the referenced pin.

All AC parameters assume a load capacitance of 100 pF. Add a 10-ns delay for each 50-pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to V_{OL} MAX or V_{OL} MIN as indicated in Figures 20 through 30 (except for CLOCK, which is referenced to the 10% and 90% points). Ordering Information lists temperature ranges and product numbers. Find package drawings in Package Information.

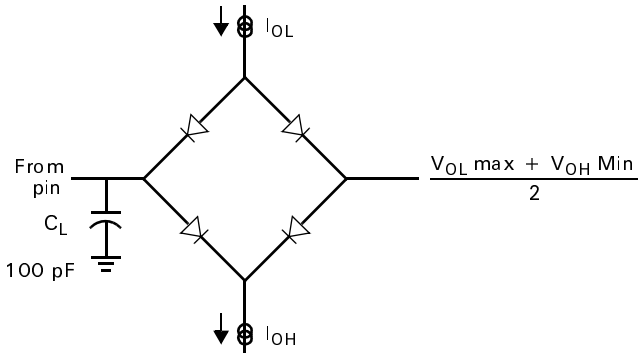


Figure 19. AC Parameter Test Circuit

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 ~ +7.0	V
Input Voltage	V_{IN}	–0.3 ~ V_{cc} +0.3	V
Operating Temperature	T_{OPR}	0 ~ 70	°C
Extended Temperature	T_{EXT}	–40 ~ 85	°C
Storage Temperature	T_{STG}	–55 ~ +150	°C

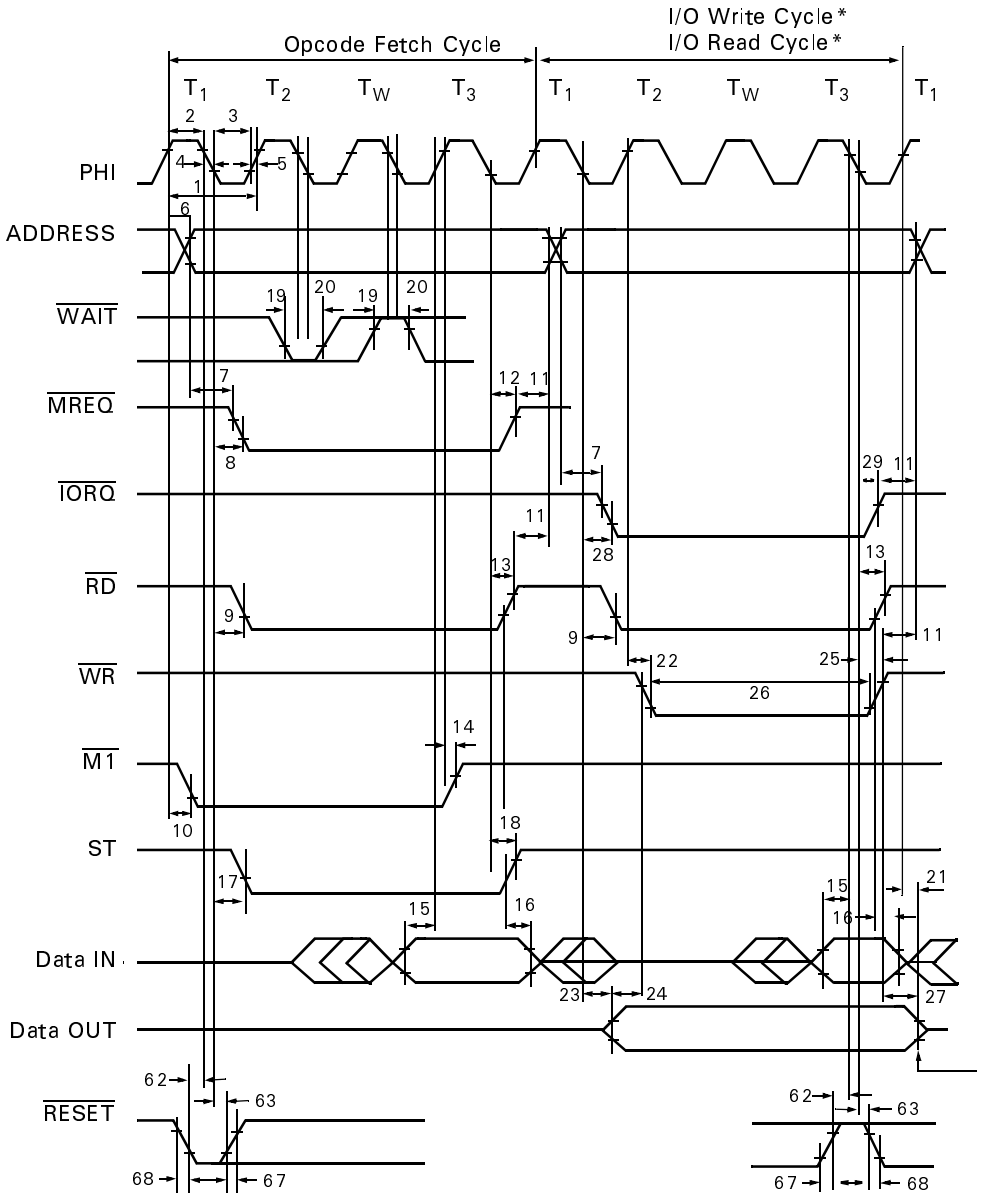
Note: Permanent damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability.

Table 7. Z8L180 DC Characteristics
V_{DD} = 3.3V ±10%; V_{SS} = 0V

Symbol	Item	Condition	Min	Typ	Max	Unit
V_{IH1}	Input H Voltage $\overline{RESET}$, EXTAL, $\overline{NMI}$		V_{DD} –0.6		V_{DD} +0.3	V
V_{IH2}	Input H Voltage Except $\overline{RESET}$, EXTAL, $\overline{NMI}$		2.0		V_{DD} +0.3	V
V_{IL1}	Input L Voltage RESET, EXTAL, NMI		–0.3		0.6	V
V_{IL2}	Input L Voltage Except RESET, EXTAL, NMI		–0.3		0.8	V
V_{OH}	Outputs H Voltage All outputs	I_{OH} = –200 µA	2.15			V
		I_{OH} = –20 µA	V_{DD} –0.6			V
V_{OL}	Outputs L Voltage All Outputs	I_{OL} = 4 mA			0.4	V
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL	V_{IN} = 0.5 ~ V_{DD} –0.5			1.0	µA
I_{TL}	Three State Leakage Current	V_{IN} = 0.5 ~ V_{DD} –0.5			1.0	µA
I_{DD1}	Power Dissipation (Normal Operation)	F = 20 MHz		30	60	mA
		4 MHz		4	10	
	Power Dissipation (SYSTEM STOP mode)	F = 20 MHz		5	10	
		4 MHz		2	5	
C_P	Pin Capacitance	V_{IN} = 0V, f = 1 MHz T_A = 25° C			12	pF

Note:
1. V_{IHmin} = V_{DD} –1.0V, V_{ILmax} = 0.6V (All output terminals are at NO LOAD.) V_{DD} = 3.0V.

TIMING DIAGRAMS



Note: *Memory Read/Write Cycle timing is the same as I/O Read/Write Cycle except there are no automatic wait states (T_W), and $\overline{MREQ}$ is active instead of $\overline{IORQ}$.

Figure 20. CPU Timing
(Opcode Fetch Cycle, Memory Read Cycle, Memory Write Cycle, I/O Write Cycle, I/O Read Cycle)

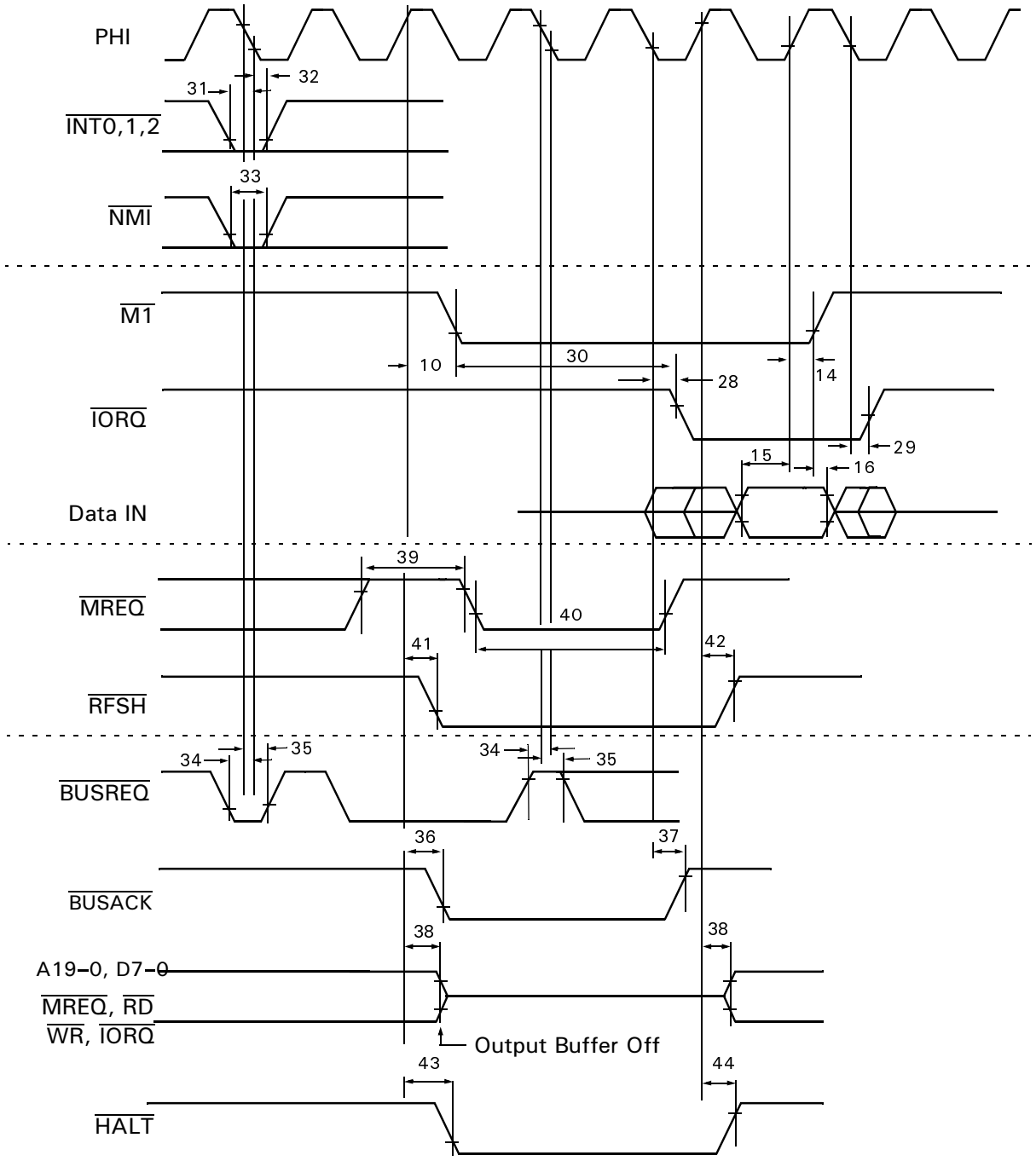


Figure 21. CPU Timing
(INT0 Acknowledge Cycle, Refresh Cycle, BUS RELEASE Mode, HALT Mode, SLEEP Mode, SYSTEM STOP Mode)

CPU CONTROL REGISTER

CPU Control Register (CCR). This register controls the basic clock rate, certain aspects of Power-Down modes, and output drive/low-noise options (Figure 31).

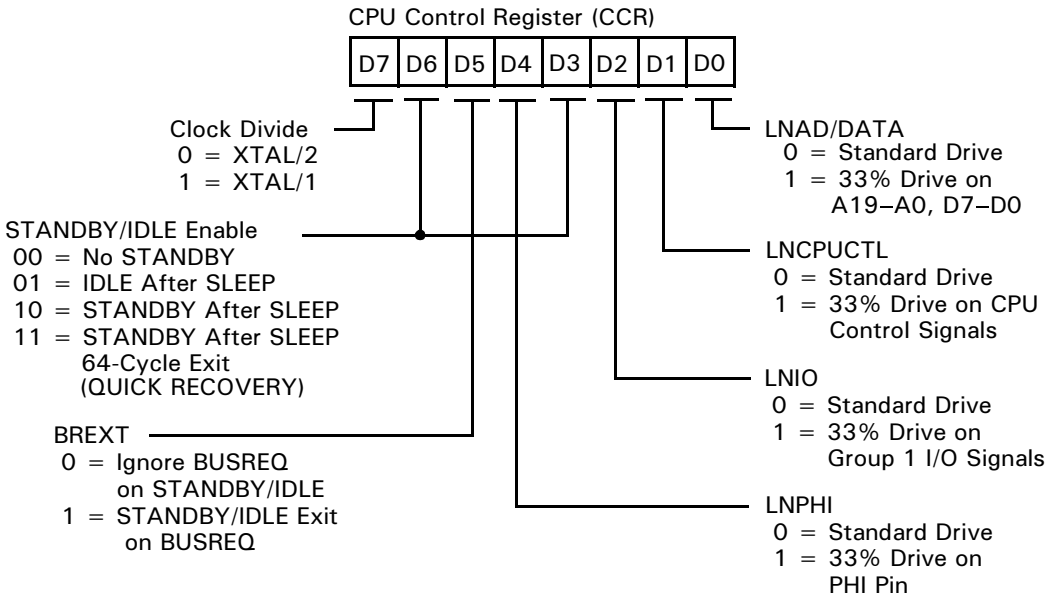


Figure 31. CPU Control Register (CCR) Address 1FH

Bit 7. Clock Divide Select. If this bit is 0, as it is after a RESET, the Z8S180/Z8L180 divides the frequency on the XTAL pin(s) by two to obtain its Master clock PHI. If this bit is programmed as 1, the part uses the XTAL frequency as PHI without division.

If an external oscillator is used in divide-by-one mode, the minimum pulse width requirement provided in the AC Characteristics must be satisfied.

Bits 6 and 3. STANDBY/IDLE Control. When these bits are both 0, a SLP instruction makes the Z8S180/Z8L180 enter SLEEP or SYSTEM STOP mode, depending on the IOSTOP bit (ICR5).

When D6 is 0 and D3 is 1, setting the IOSTOP bit (ICR5) and executing a SLP instruction puts the Z8S180/Z8L180 into IDLE mode in which the on-chip oscillator runs, but its output is blocked from the rest of the part, including PHI out.

When D6 is 1 and D3 is 0, setting IOSTOP (ICR5) and executing a SLP instruction puts the part into STANDBY mode, in which the on-chip oscillator is stopped and the part allows 2^{17} (128K) clock cycles for the oscillator to stabilize when it restarts.

When D6 and D3 are both 1, setting IOSTOP (ICR5) and executing a SLP instruction puts the part into QUICK RECOVERY STANDBY mode, in which the on-chip oscillator is stopped, and the part allows only 64 clock cycles for the oscillator to stabilize when it restarts.

The latter section, HALT and LOW POWER modes, describes the subject more fully.

Bit 5 BREXT. This bit controls the ability of the Z8S180/Z8L180 to honor a bus request during STANDBY mode. If this bit is set to 1 and the part is in STANDBY mode, a BUSREQ is honored after the clock stabilization timer is timed out.

Bit 4 LNPHI. This bit controls the drive capability on the PHI Clock output. If this bit is set to 1, the PHI Clock output is reduced to 33 percent of its drive capability.

Bit 2 LNIO. This bit controls the drive capability of certain external I/O pins of the Z8S180/Z8L180. When this bit is set to 1, the output drive capability of the following pins is reduced to 33 percent of the original drive capability:

$\overline{RTS0}$	TxS
CKA1/$\overline{TEND0}$	CKA0/$\overline{DREQ0}$
TXA0	TXA1
$\overline{TENDi}$	CKS

Bit 1 LNCPUCTL. This bit controls the drive capability of the CPU Control pins. When this bit is set to 1, the output drive capability of the following pins is reduced to 33 percent of the original drive capability:

$\overline{BUSACK}$	$\overline{RD}$
$\overline{WR}$	$\overline{M1}$
$\overline{MREQ}$	$\overline{IORQ}$
$\overline{RFSH}$	$\overline{HALT}$
E	TEST
ST	

Bit 0 LNAD/DATA. This bit controls the drive capability of the Address/Data bus output drivers. If this bit is set to 1, the output drive capability of the Address and Data bus outputs is reduced to 33 percent of its original drive capability.

ASCI REGISTER DESCRIPTION

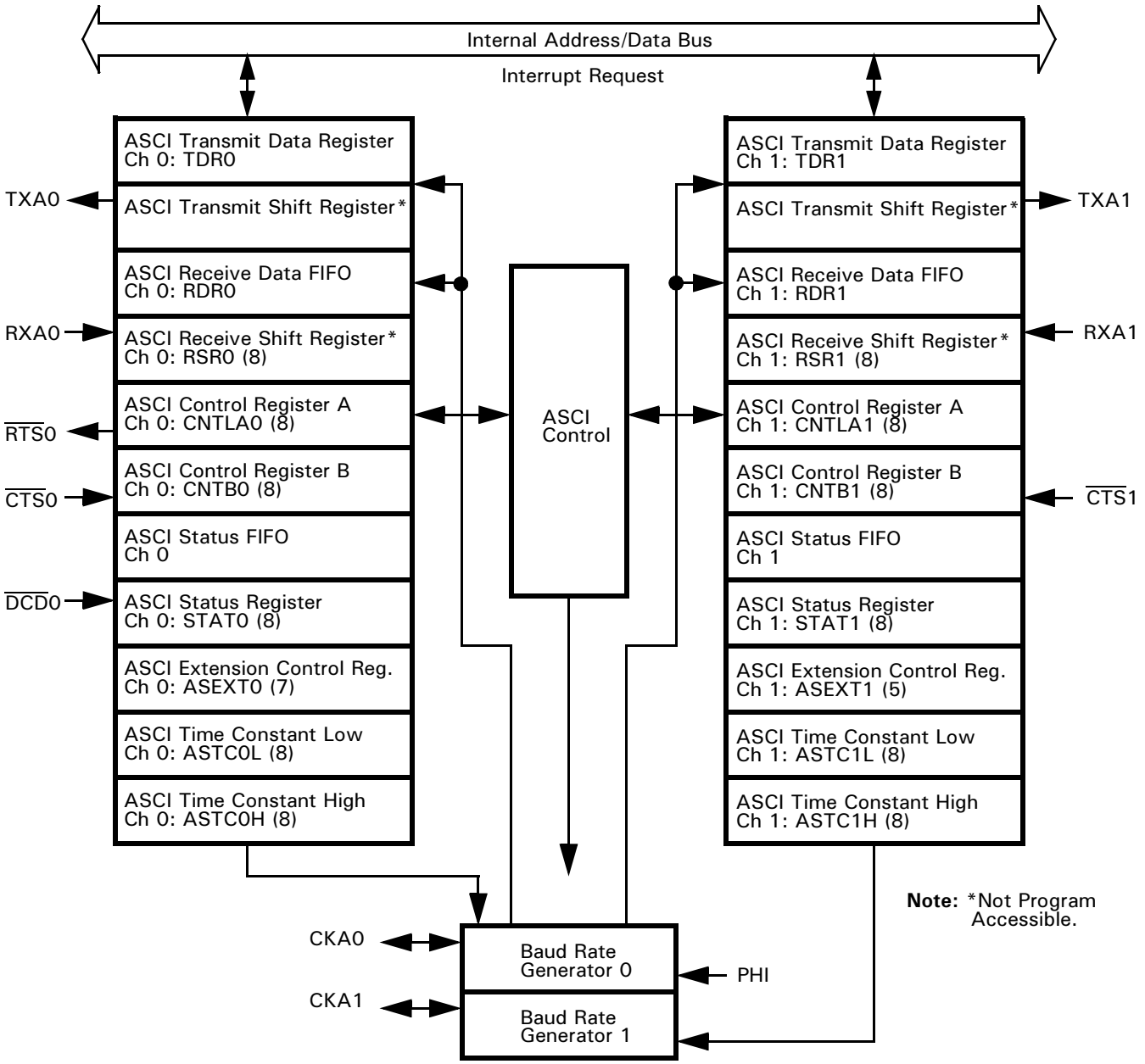


Figure 32. ASCI Block Diagram

ASCI Transmit Shift Register 0,1. When the ASCI Transmit Shift Register (TSR) receives data from the ASCI Transmit Data Register (TDR), the data is shifted out to the TXA pin. When transmission is completed, the next byte (if available) is automatically loaded from TDR into TSR and the next transmission starts. If no data is available for transmission, TSR idles by outputting a continuous High level. This register is not program-accessible

ASCI Transmit Data Register 0,1 (TDR0, 1: I/O address = 06H, 07H). Data written to the ASCI Transmit Data Register is transferred to the TSR as soon as TSR is empty. Data can be written while TSR is shifting out the previous byte of data. Thus, the ASCI transmitter is double buffered.

TIMER CONTROL REGISTER

The Timer Control Register (TCR) monitors both channels (PRT0, PRT1) TMDR status. It also controls the enabling and disabling of down-counting and interrupts, and controls the output pin A18/T_{OUT} for PRT1.

Bit	7	6	5	4	3	2	1	0
	TIF1	TIF0	TIE1	TIE0	TOC1	TOC0	TDE1	TDE0
	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Figure 46. Timer Control Register (TCR: I/O Address = 10H)

TIF1: Timer Interrupt Flag 1 (Bit 7) . When TMDR1 decrements to 0, TIF1 is set to 1. This condition generates an interrupt request if enabled by TIE1 = 1. TIF1 is reset to 0 when TCR is read and the higher or lower byte of TMDR1 is read. During RESET, TIF1 is cleared to 0.

TIF0: Timer Interrupt Flag 0 (Bit 6). When TMDR0 decrements to 0, TIF0 is set to 1. This condition generates an interrupt request if enabled by TIE0 = 1. TIF0 is reset to 0 when TCR is read and the higher or lower byte of TMDR0 is read. During RESET, TIF0 is cleared to 0.

TIE1: Timer Interrupt Enable 1 (Bit 5). When TIE0 is set to 1, TIF1 = 1 generates a CPU interrupt request. When TIE0 is reset to 0, the interrupt request is inhibited. During RESET, TIE0 is cleared to 0.

TOC1, 0: Timer Output Control (Bits 3, 2). TOC1 and TOC0 control the output of PRT1 using the multiplexed A18/T_{OUT} pin as indicated in Table 12. During RESET, TOC1 and TOC0 are cleared to 0. If bit 3 of the IAR1B register is 1, the T_{OUT} function is selected. By programming TOC1 and TOC0, the A18/T_{OUT} pin can be forced High, Low, or toggled when TMDR1 decrements to 0.

Table 12. Timer Output Control

TOC1	TOC0	Output	
0	0	Inhibited	The A18/T_{OUT} pin is not affected by the PRT
0	1	Toggled	If bit 3 of IAR1B is 1, the A18/T_{OUT} pin is toggled or set Low or High as indicated
1	0	0	
1	1	1	

TDE1, 0: Timer Down Count Enable (Bits 1, 0). TDE1 and TDE0 enable and disable down-counting for TMDR1 and TMDR0, respectively. When TDEn (n = 0,1) is set to 1, down-counting is stopped and TMDRn is freely read or written. TDE1 and TDE0 are cleared to 0 during RESET and TMDRn does not decrement until TDEn is set to 1.

ASCI EXTENSION CONTROL REGISTER CHANNEL 0 AND CHANNEL 1

The ASCI Extension Control Registers (ASEXT0 and ASEXT1) control functions that have been added to the ASCIs in the Z8S180/Z8L180 family. All bits in this register reset to 0.

ASCI Extension Control Register 0 (ASEXT0 I/O Address = 12H)

Bit	7	6	5	4	3	2	1	0
	Reserved	DCD0 Disable	CTS0 Disable	X1	BRG0 Mode	Break Enable	Break	Send Break

ASCI Extension Control Register 1 (ASEXT1 I/O Address = 13H)

Bit	7	6	5	4	3	2	1	0
	Reserved	Reserved	Reserved	X1	BRG1 Mode	Break Enable	Break	Send Break

Figure 47. ASCI Extension Control Registers, Channels 0 and 1

DCD0 Disable (Bit 6, ASCI0 Only). If this bit is 0, then the $\overline{\text{DCD0}}$ pin auto-enables the ASCI0 receiver, such that when the pin is negated/High, the Receiver is held in a RESET state. If this bit is 1, the state of the $\overline{\text{DCD}}$-pin has no effect on receiver operation. In either state of this bit, software can read the state of the $\overline{\text{DCD0}}$ pin in the STAT0 register, and the receiver interrupts on a rising edge of $\overline{\text{DCD0}}$.

CTS0 Disable (Bit 5, ASCI0 Only). If this bit is 0, then the $\overline{\text{CTS0}}$ pin auto-enables the ASCIO transmitter, in that when the pin is negated/High, the TDRE bit in the STAT0 register is forced to 0. If this bit is 1, the state of the $\overline{\text{CTS0}}$ pin has no effect on the transmitter. Regardless of the state of this bit, software can read the state of the $\overline{\text{CTS0}}$ pin the CNTLB0 register.

X1 (Bit 4). If this bit is 1, the clock from the Baud Rate Generator or CKA pin is taken as a 1X-bit clock (sometimes called *isochronous mode*). In this mode, receive data on the RXA pin must be synchronized to the clock on the CKA pin, regardless of whether CKA is an input or an output. If this bit is 0, the clock from the Baud Rate Generator or CKA pin is divided by 16 or 64 per the DR bit in the CNTLB register, to obtain the actual bit rate. In this mode, receive data on the RXA pin is not required to be synchronized to a clock.

BRG Mode (Bit 3). If the SS2–0 bits in the CNTLB register are not 111, and this bit is 0, the ASCI Baud Rate Generator divides PHI by 10 or 30, depending on the PS bit in CNTLB, and factored by a power of two (selected by the SS2–0 bits), to obtain the clock that is presented to the transmitter and receiver and output on the CKA pin. If SS2–0 are not 111, and this bit is 1, the Baud Rate Generator divides PHI by twice the sum of the 16-bit value (programmed into the Time Constant registers) and 2. This mode is identical to the operation of the baud rate generator in the ESCC.

Break Enable (Bit 2). If this bit is 1, the receiver detects BREAK conditions and report them in bit 1, and the transmitter sends BREAKs under the control of bit 0.

Break Detect (Bit 1). The receiver sets this read-only bit to 1 when an all-zero character with a Framing Error becomes the oldest character in the Rx FIFO. The bit is cleared when software writes a 0 to the EFR bit in CNTLA register, also by RESET, by IOSTOP mode, and for ASCI0, if the $\overline{\text{DCD0}}$ pin is auto-enabled and is negated (High).

Send Break (Bit 0). If this bit and bit 2 are both 1, the transmitter holds the TXA pin Low to send a BREAK condition. The duration of the BREAK is under software control (one of the PRTs or CTCs can be used to time it). This bit resets to 0, in which state TXA carries the serial output of the transmitter.

DMA SOURCE ADDRESS REGISTER CHANNEL 0

The DMA Source Address Register Channel 0 specifies the physical source address for channel 0 transfers. The register contains 20 bits and can specify up to 1024 KB memory addresses or up to 64-KB I/O addresses. Channel 0 source can be memory, I/O, or memory mapped I/O. For I/O, bits 17–16 of this register identify the Request Handshake signal.

DMA Source Address Register, Channel 0 Low

Mnemonic SAR0L
Address 20H

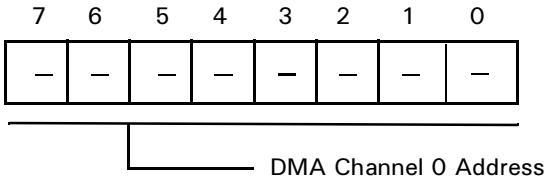


Figure 55. DMA Source Address Register 0 Low

DMA Source Address Register, Channel 0 High

Mnemonic SAR0H
Address 21H

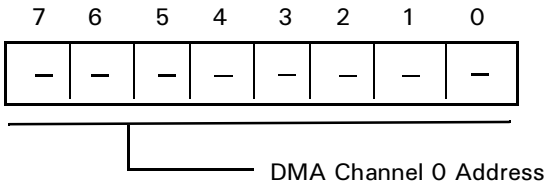


Figure 56. DMA Source Address Register 0 High

DMA Source Address Register Channel 0B

Mnemonic SAR0B
Address 22H

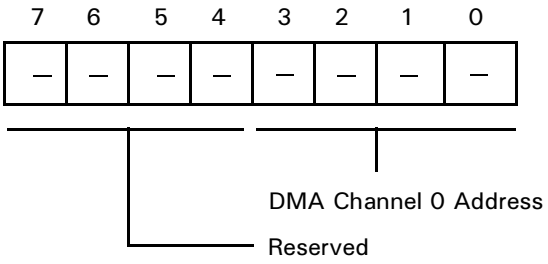


Figure 57. DMA Source Address Register 0B

If the source is in I/O space, bits 1–0 of this register select the DMA request signal for DMA0, as follows:

Bit 1 (A17)	Bit 0 (A16)	DMA Transfer Request
0	0	DREQ0 (external)
0	1	RDRF (ASCI0)
1	0	RDRF (ASCI1)
1	1	Reserved

DMA DESTINATION ADDRESS REGISTER CHANNEL 0

The DMA Destination Address Register Channel 0 specifies the physical destination address for channel 0 transfers. The register contains 20 bits and can specify up to 1024-KB memory addresses or up to 64-KB I/O addresses. Channel 0 destination can be memory, I/O, or memory mapped I/O. For I/O, the MS bits of this register identify the Request Handshake signal for channel 0.

DMA Destination Address Register Channel 0 Low

Mnemonic DAR0L
Address 23H

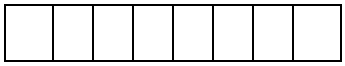


Figure 58. DMA Destination Address Register Channel 0 Low

DMA Destination Address Register Channel 0 High

Mnemonic DAR0H
Address 24H

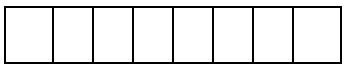


Figure 59. DMA Destination Address Register Channel 0 High

DMA Destination Address Register Channel 0B

Mnemonic DAR0B
Address 25H

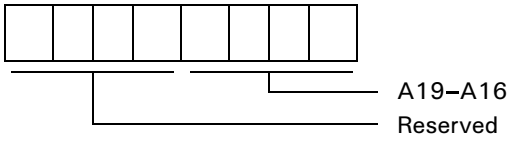


Figure 60. DMA Destination Address Register Channel 0B

If the DMA destination is in I/O space, bits 1–0 of this register select the DMA request signal for DMA0, as follows:

Bit 1 (A17)	Bit 0 (A16)	DMA Transfer Request
0	0	DREQ0 (external)
0	1	TDR0 (ASCI0)
1	0	TDR1 (ASCI1)
1	1	Not Used

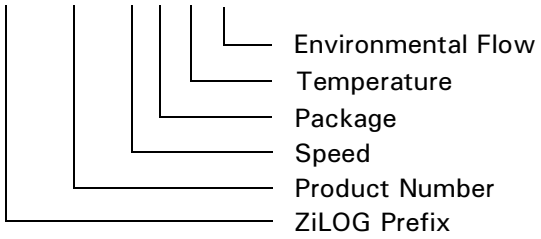
ORDERING INFORMATION

Codes	
Speed	10 = 10 MHz
	20 = 20 MHz
	33 = 33 MHz
Package	P = 60-Pin Plastic DIP
	V = 68-Pin PLCC
	F = 80-Pin QFP
Temperature	S = 0°C to +70°C
	E = –40°C to +85°C
Environmental	C = Plastic Standard

For fast results, contact your local ZiLOG sales office for assistance in ordering the part(s) required.

Example:

Z 8S180 10 P S C is a Z8S180 10-MHz 60-Pin DIP, 0° to +70°C, Plastic Standard Flow



Pre-Characterization Product

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or non-conformance with some aspects of the document may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

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