Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	33MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	80-BQFP
Supplier Device Package	80-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8s18033fsc

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
39	41	38	D4		3T	3T	3T
40	42	39	D5		3T	3T	3T
41	43	40	D6		3T	3T	3T
42			NC				
43			NC				
44	44	41	D7		3T	3T	3T
45	45	42	$\overline{\text{RTS0}}$		High	OUT	High
46	46	43	$\overline{\text{CTS0}}$		IN	OUT	IN
47	47	44	$\overline{\text{DCD0}}$		IN	IN	IN
48	48	45	TXA0		High	OUT	OUT
49	49	46	RXA0		IN	IN	IN
50	50	47	CKA0		3T	I/O	I/O
			$\overline{\text{DREQ0}}$		N/A	IN	IN
51			NC				
52	51	48	TXA1		High	OUT	OUT
53	52		TEST				
54	53	49	RXA1		IN	IN	IN
55	54	50	CKA1		3T	I/O	I/O
			$\overline{\text{TEND0}}$		N/A	High	High
56	55	51	TXS		High	OUT	OUT
57	56	52	RXS		IN	IN	IN
			$\overline{\text{CTS1}}$		N/A	IN	IN
58	57	53	CKS		3T	I/O	I/O
59	58	54	$\overline{\text{DREQ1}}$		IN	3T	IN
60	59	55	$\overline{\text{TEND1}}$		High	OUT	High
61	60	56	$\overline{\text{HALT}}$		High	High	Low
62			NC				
63			NC				
64	61	57	$\overline{\text{RFSH}}$		High	OUT	High
65	62	58	$\overline{\text{IORQ}}$		High	3T	High
66	63	59	$\overline{\text{MREQ}}$		High	3T	High
67	64	60	E		Low	OUT	OUT
68	65	61	$\overline{\text{M1}}$		High	High	High
69	66	62	$\overline{\text{WR}}$		High	3T	High
70	67	63	$\overline{\text{RD}}$		High	3T	High
71	68	64	PHI		OUT	OUT	OUT
72	1	1	V_{SS}		GND	GND	GND
73	2		V_{SS}		GND	GND	GND
74	3	2	XTAL		OUT	OUT	OUT
75			NC				

PIN IDENTIFICATION (Continued)

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
76	4	3	EXTAL		IN	IN	IN
77	5	4	$\overline{\text{WAIT}}$		IN	IN	IN
78	6	5	$\overline{\text{BUSACK}}$		High	OUT	OUT
79	7	6	$\overline{\text{BUSREQ}}$		IN	IN	IN
80	8	7	$\overline{\text{RESET}}$		IN	IN	IN

PIN DESCRIPTIONS

A0–A19. Address Bus (Output, 3-state). A0–A19 form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 1 MB) and I/O data bus exchanges (up to 64 KB). The address bus enters a high–impedance state during reset and external bus acknowledge cycles. Address line A18 is multiplexed with the output of PRT channel 1 (T_{OUT}, selected as address output on reset), and address line A19 is not available in DIP versions of the Z8S180.

BUSACK. Bus Acknowledge (Output, active Low). BUSACK indicates that the requesting device, the MPU address and data bus, and some control signals enter their high-impedance state.

BUSREQ. Bus Request (Input, active Low). This input is used by external devices (such as DMA controllers) to request access to the system bus. This request demands a higher priority than NMI and is always recognized at the end of the current machine cycle. This signal stops the CPU from executing further instructions, places addresses, data buses, and other control signals into the high-impedance state.

CKA0, CKA1. Asynchronous Clock 0 and 1 (bidirectional). When in output mode, these pins are the transmit and receive clock outputs from the ASCI baud rate generators. When in input mode, these pins serve as the external clock inputs for the ASCI baud rate generators. CKA0 is multiplexed with DREQ0, and CKA1 is multiplexed with TEND0.

CKS. Serial Clock (bidirectional). This line is the clock for the CSI/O channel.

CTS0–CTS1. Clear to send 0 and 1 (Inputs, active Low). These lines are modem control signals for the ASCI channels. CTS1 is multiplexed with RXS.

D0–D7. Data Bus = (bidirectional, 3-state). D0–D7 constitute an 8-bit bidirectional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high-impedance state during reset and external bus acknowledge cycles.

DCD0. Data Carrier Detect 0 (Input, active Low); a programmable modem control signal for ASCI channel 0.

DREQ0, DREQ1. DMA Request 0 and 1 (Input, active Low). DREQ is used to request a DMA transfer from one of the on-chip DMA channels. The DMA channels monitor these inputs to determine when an external device is ready for a READ or WRITE operation. These inputs can be programmed to be either level or edge sensed. DREQ0 is multiplexed with CKA0.

E. Enable Clock (Output). This pin functions as a synchronous, machine-cycle clock output during bus transactions.

EXTAL. External Clock Crystal (Input). Crystal oscillator connections. An external clock can be input to the Z8S180/Z8L180 on this pin when a crystal is not used. This input is Schmitt triggered.

HALT. HALT/SLEEP (Output, active Low). This output is asserted after the CPU executes either the HALT or SLEEP instruction and is waiting for either a nonmaskable or a maskable interrupt before operation can resume. It is also used with the M1 and ST signals to decode the status of the CPU machine cycle.

INT0. Maskable Interrupt Request 0 (Input, active Low). This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the NMI and BUSREQ signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the M1 and IORQ signals become active.

INT1, INT2. Maskable Interrupt Request 1 and 2 (Inputs, active Low). This signal is generated by external I/O devices. The CPU honors these requests at the end of the current instruction cycle as long as the NMI, BUSREQ, and INT0 signals are inactive. The CPU acknowledges these requests with an interrupt acknowledge cycle. Unlike the acknowledgment for INT0, neither the M1 or IORQ signals become active during this cycle.

IORQ. I/O Request (Output, active Low, 3-state). IORQ indicates that the address bus contains a valid I/O address for an I/O READ or I/O WRITE operation. IORQ is also generated, along with M1, during the acknowledgment of the INT0 input signal to indicate that an interrupt response vector can be place onto the data bus. This signal is analogous to the IOE signal of the Z64180.

M1. Machine Cycle 1 (Output, active Low). Together with MREQ, M1 indicates that the current cycle is the opcode-fetch cycle of instruction execution. Together with IORQ, M1 indicates that the current cycle is for interrupt acknowledgment. It is also used with the HALT and ST signal to decode the status of the CPU machine cycle. This signal is analogous to the LIR signal of the Z64180.

MREQ. Memory Request (Output, active Low, 3-state). MREQ indicates that the address bus holds a valid address for a memory READ or memory WRITE operation. This signal is analogous to the ME signal of Z64180.

NMI. Nonmaskable Interrupt (Input, negative edge triggered). NMI demands a higher priority than INT and is al-

PIN DESCRIPTIONS (Continued)

ways recognized at the end of an instruction, regardless of the state of the interrupt-enable flip-flops. This signal forces CPU execution to continue at location 0066H.

PHI. System Clock (Output). The output is used as a reference clock for the MPU and the external system. The frequency of this output may be one-half, equal to, or twice the crystal or input clock frequency.

$\overline{\text{RD}}$. Read (Output, active Low, 3-state). $\overline{\text{RD}}$ indicates that the CPU wants to read data from either memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus.

$\overline{\text{RFSH}}$. Refresh (Output, active Low). Together with $\overline{\text{MREQ}}$, $\overline{\text{RFSH}}$ indicates that the current CPU machine cycle and the contents of the address bus should be used for refresh of dynamic memories. The low-order 8 bits of the address bus (A7–A0) contain the refresh address. *This signal is analogous to the $\overline{\text{REF}}$ signal of the Z64180.*

$\overline{\text{RTS0}}$. Request to Send 0 (Output, active Low); a programmable MODEM control signal for ASCI channel 0.

RXA0, RXA1. Receive Data 0 and 1 (Input). These signals are the receive data for the ASCI channels.

RXS. Clocked Serial Receive Data (Input). This line is the receive data for the CSI/O channel. RXS is multiplexed with the $\overline{\text{CTS1}}$ signal for ASCI channel 1.

ST. Status (Output). This signal is used with the $\overline{\text{M1}}$ and $\overline{\text{HALT}}$ output to decode the status of the CPU machine cycle. See Table 3.

Table 3. Status Summary

ST	$\overline{\text{HALT}}$	$\overline{\text{M1}}$	Operation
0	1	0	CPU Operation (1st Opcode Fetch)
1	1	0	CPU Operation (2nd Opcode and 3rd Opcode Fetch)
1	1	1	CPU Operation (MC Except Opcode Fetch)
0	X	1	DMA Operation
0	0	0	HALT Mode
1	0	1	SLEEP Mode (Including SYSTEM STOP Mode)

Notes:
X = Do not care.
MC = Machine Cycle.

$\overline{\text{TEND0}}$, $\overline{\text{TEND1}}$. Transfer End 0 and 1 (Outputs, active Low). This output is asserted active during the most recent WRITE cycle of a DMA operation. It is used to indicate the end of the block transfer. $\overline{\text{TEND0}}$ is multiplexed with CKA1.

TEST. Test (Output, not in DIP version). This pin is for test and should be left open.

T_{OUT}. Timer Out (Output). T_{OUT} is the output from PRT channel 1. This line is multiplexed with A18 of the address bus.

TXA0, TXA1. Transmit Data 0 and 1 (Outputs). These signals are the transmitted data from the ASCI channels. Transmitted data changes are with respect to the falling edge of the transmit clock.

TXS. Clocked Serial Transmit Data (Output). This line is the transmitted data from the CSI/O channel.

$\overline{\text{WAIT}}$. Wait (Input, active Low). $\overline{\text{WAIT}}$ indicates to the MPU that the addressed memory or I/O devices are not ready for data transfer. This input is sampled on the falling edge of T2 (and subsequent WAIT states). If the input is sampled Low, then the additional WAIT states are inserted until the $\overline{\text{WAIT}}$ input is sampled High, at which time execution continues.

$\overline{\text{WR}}$. WRITE (Output, active Low, 3-state). $\overline{\text{WR}}$ indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

XTAL. Crystal Oscillator Connection (Input). This pin should be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (see DC Characteristics).

Several pins are used for different conditions, depending on the circumstance.

This condition provides a technique for synchronization with high-speed external events without incurring the latency imposed by an interrupt-response sequence. Figure 14 depicts the timing for exiting SLEEP mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes about 1.5 clock ticks to restart.

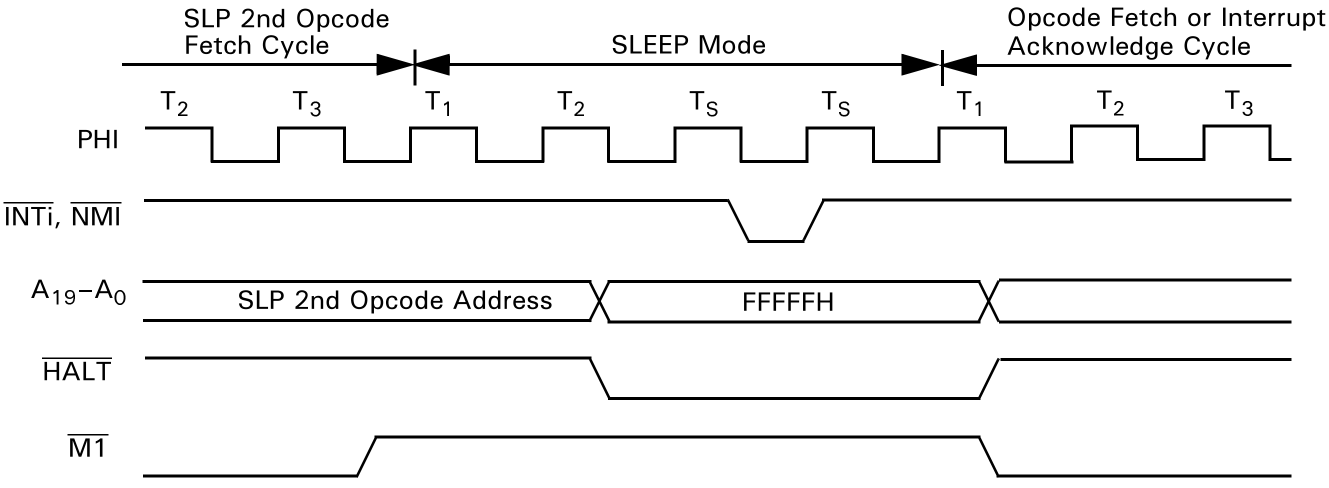


Figure 14. SLEEP Timing

IOSTOP Mode. IOSTOP mode is entered by setting the IOSTOP bit of the I/O Control Register (ICR) to 1. In this case, on-chip I/O (ASCI, CSI/O, PRT) stops operating. However, the CPU continues to operate. Recovery from IOSTOP mode is performed by resetting the IOSTOP bit in ICR to 0.

SYSTEM STOP Mode. SYSTEM STOP mode is the combination of SLEEP and IOSTOP modes. SYSTEM STOP mode is entered by setting the IOSTOP bit in ICR to 1 followed by execution of the SLP instruction. In this mode, on-chip I/O and CPU stop operating, reducing power consumption, but the PHI output continues to operate. Recovery from SYSTEM STOP mode is the same as recovery from SLEEP mode except that internal I/O sources (disabled by IOSTOP) cannot generate a recovery interrupt.

IDLE Mode. Software puts the Z8S180/Z8L180 into this mode by performing the following actions:

- Set the IOSTOP bit (ICR5) to 1
- Set CCR6 to 0
- Set CCR3 to 1
- Execute the SLP instruction

The oscillator keeps operating but its output is blocked to all circuitry including the PHI pin. DRAM refresh and all internal devices stop, but external interrupts can occur. Bus granting to external Masters can occur if the BREST bit in the CPU control Register (CCR5) was set to 1 before IDLE mode was entered.

The Z8S180/Z8L180 leaves IDLE mode in response to a Low on $\overline{\text{RESET}}$, an external interrupt request on $\overline{\text{NMI}}$, or an external interrupt request on $\overline{\text{INT0}}$, $\overline{\text{INT1}}$ or $\overline{\text{INT2}}$ that is enabled in the INT/TRAP Control Register. As previously described for SLEEP mode, when the Z8S180/Z8L180 leaves IDLE mode due to an $\overline{\text{NMI}}$, or due to an enabled external interrupt request when the $\overline{\text{IEF}}$ flag is 1 due to an EI instruction, the device starts by performing the interrupt with the return address of the instruction after the SLP instruction.

If an external interrupt enables the INT/TRAP control register while the IEF1 bit is 0, Z8S180/Z8L180 leaves IDLE mode; specifically, the processor restarts by executing the instructions following the SLP instruction.

Figure 15 indicates the timing for exiting IDLE mode due to an interrupt request.

Note: The Z8S180/Z8L180 takes about 9.5 clocks to restart.

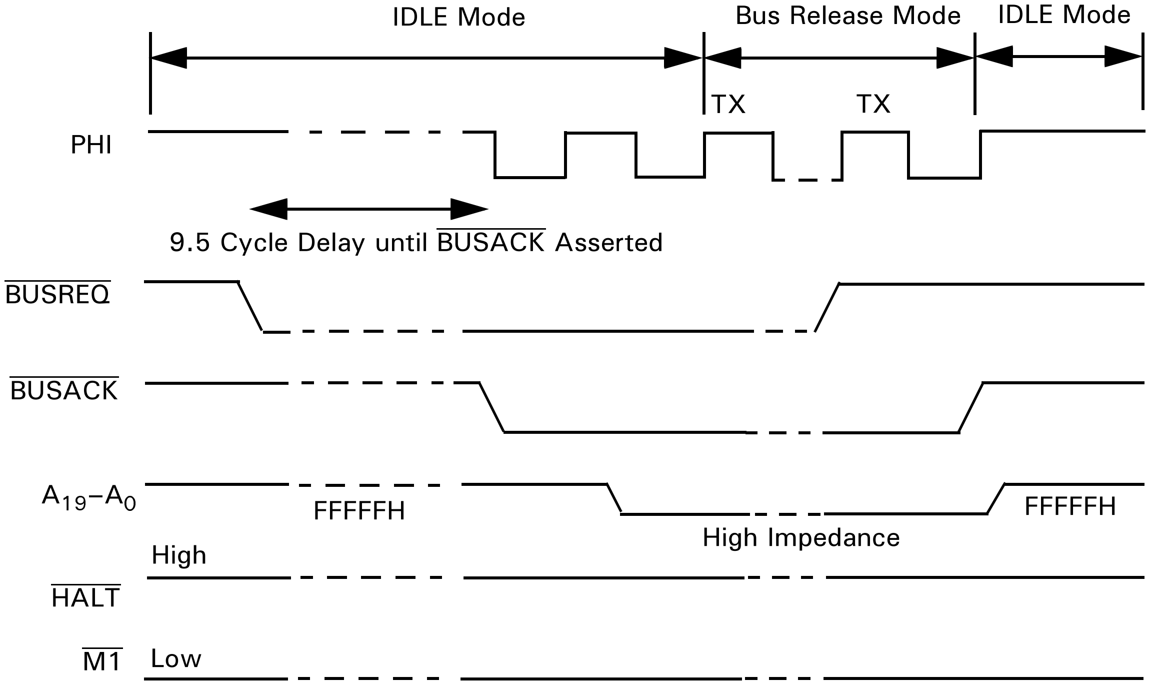


Figure 16. Bus Granting to External Master in IDLE Mode

STANDBY Mode (With or Without QUICK RECOVERY).

Software can put the Z8S180/Z8L180 into this mode by setting the IOSTOP bit (ICR5) to `1`, CCR6 to `1`, and executing the SLP instruction. This mode stops the on-chip oscillator and thus draws the least power of any mode, less than 10µA.

As with IDLE mode, the Z8S180/Z8L180 leaves STANDBY mode in response to a Low on RESET, on NMI, or a Low on INT0–2 that is enabled by a `1` in the corresponding bit in the INT/TRAP Control Register. This action grants the bus to an external Master if the BREXT bit in the CPU Control Register (CCR5) is `1`. The time required for all of these operations is greatly increased by the necessity for restarting the on-chip oscillator, and ensuring that it stabilizes to square-wave operation.

When an external clock is connected to the EXTAL pin rather than a crystal to the XTAL and EXTAL pins and the external clock runs continuously, there is little necessity to use STANDBY mode because no time is required to restart the oscillator, and other modes restart faster. However, if external logic stops the clock during STANDBY mode (for example, by decoding HALT Low and M1 High for several clock cycles), then STANDBY mode can be useful to allow the external clock source to stabilize after it is re-enabled.

When external logic drives RESET Low to bring the device out of STANDBY mode, and a crystal is in use or an external clock source is stopped, the external logic must hold RESET Low until the on-chip oscillator or external clock source is restarted and stabilized.

The clock-stability requirements of the Z8S180/Z8L180 are much less in the divide-by-two mode that is selected by a RESET sequence and controlled by the Clock Divide bit in the CPU Control Register (CCR7). As a result, software performs the following actions:

1. Sets CCR7 to `0` for divide-by-two mode before an SLP instruction and STANDBY mode.
2. Delays setting CCR7 back to `1` for divide-by-one mode as long as possible to allow additional clock stabilization time after a RESET, interrupt, or in-line RESTART after an SLP 01 instruction.

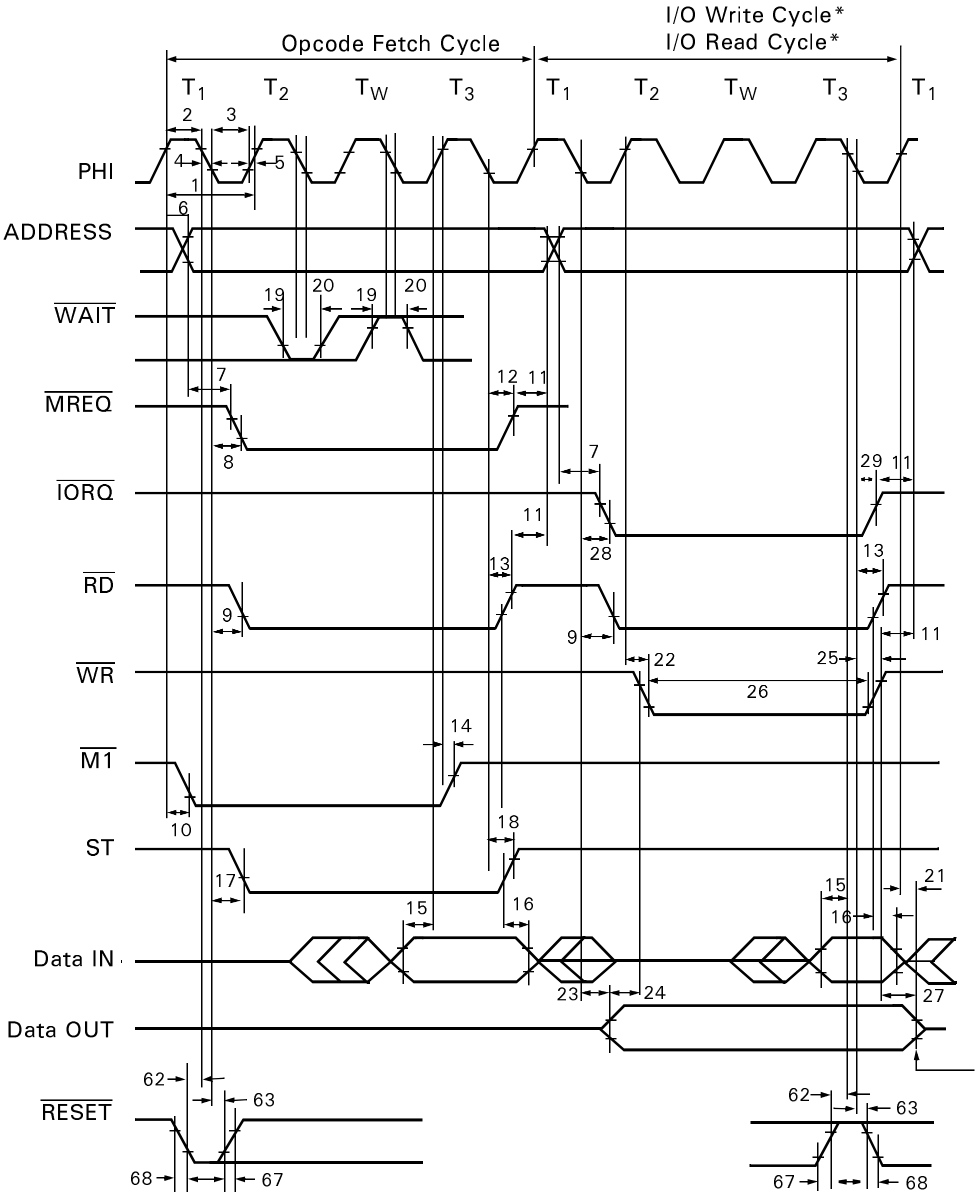
If CCR6 is set to `1` before the SLP instruction places the MPU in STANDBY mode, the value of the CCR3 bit determines the length of the delay before the oscillator restarts and stabilizes when it leaves STANDBY mode due to an external interrupt request. When CCR3 is `0`, the Z8S180/Z8L180 waits 2^{17} (131,072) clock cycles. When CCR3 is `1`, it waits 64 clock cycles. This state is called QUICK RECOVERY mode. The same delay applies to grant-

AC CHARACTERISTICS—Z8S180 (Continued)

Table 8. Z8S180 AC Characteristics (Continued)
V_{DD} = 5V ±10% or V_{DD} = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation

			Z8S180—20 MHz		Z8S180—33 MHz		
Number	**Symbol**	**Item**	**Min**	**Max**	**Min**	**Max**	**Unit**
32	t_{INTH}	$\overline{\text{INT}}$ Hold Time from PHI Fall	10	—	10	—	ns
33	t_{NMIW}	$\overline{\text{NMI}}$ Pulse Width	35	—	25	—	ns
34	t_{BRS}	$\overline{\text{BUSREQ}}$ Set-up Time to PHI Fall	10	—	10	—	ns
35	t_{BRH}	$\overline{\text{BUSREQ}}$ Hold Time from PHI Fall	10	—	10		ns
36	t_{BAD1}	PHI Rise to $\overline{\text{BUSACK}}$ Fall Delay	—	25	—	15	ns
37	t_{BAD2}	PHI Fall to $\overline{\text{BUSACK}}$ Rise Delay	—	25	—	15	ns
38	t_{BZD}	PHI Rise to Bus Floating Delay Time	—	40	—	30	ns
39	t_{MEWH}	$\overline{\text{MREQ}}$ Pulse Width (High)	35	—	25	—	ns
40	t_{MEWL}	$\overline{\text{MREQ}}$ Pulse Width (Low)	35	—	25	—	ns
41	t_{RFD1}	PHI Rise to $\overline{\text{RFSH}}$ Fall Delay	—	20	—	15	ns
42	t_{RFD2}	PHI Rise to $\overline{\text{RFSH}}$ Rise Delay	—	20	—	15	ns
43	t_{HAD1}	PHI Rise to $\overline{\text{HALT}}$ Fall Delay	—	15	—	15	ns
44	t_{HAD2}	PHI Rise to $\overline{\text{HALT}}$ Rise Delay	—	15	—	15	ns
45	t_{DRQS}	$\overline{\text{DREQ1}}$ Set-up Time to PHI Rise	20	—	15	—	ns
46	t_{DRQH}	$\overline{\text{DREQ1}}$ Hold Time from PHI Rise	20	—	15	—	ns
47	t_{TED1}	PHI Fall to $\overline{\text{TENDi}}$ Fall Delay	—	25	—	15	ns
48	t_{TED2}	PHI Fall to $\overline{\text{TENDi}}$ Rise Delay	—	25	—	15	ns
49	t_{ED1}	PHI Rise to E Rise Delay	—	30	—	15	ns
50	t_{ED2}	PHI Fall or Rise to E Fall Delay	—	30	—	15	ns
51	P_{WEH}	E Pulse Width (High)	25	—	20	—	ns
52	P_{WEL}	E Pulse Width (Low)	50	—	40	—	ns
53	t_{Er}	Enable Rise Time	—	10	—	10	ns
54	t_{Ef}	Enable Fall Time	—	10	—	10	ns
55	t_{TOD}	PHI Fall to Timer Output Delay	—	75	—	50	ns
56	t_{STDI}	CSI/O Transmit Data Delay Time (Internal Clock Operation)	—	2	—	2	tcyc
57	t_{STDE}	CSI/O Transmit Data Delay Time (External Clock Operation)	—	7.5 t_{CYC} +75	—	75 t_{CYC} +60	ns
58	t_{SRSI}	CSI/O Receive Data Set-up Time (Internal Clock Operation)	1	—	1	—	tcyc
59	t_{SRHI}	CSI/O Receive Data Hold Time (Internal Clock Operation)	1	—	1	—	tcyc
60	t_{SRSE}	CSI/O Receive Data Set-up Time (External Clock Operation)	1	—	1	—	tcyc
61	t_{SRHE}	CSI/O Receive Data Hold Time (External Clock Operation)	1	—	1	—	tcyc
62	t_{RES}	$\overline{\text{RESET}}$ Set-up Time to PHI Fall	40	—	25	—	ns

TIMING DIAGRAMS



Note: *Memory Read/Write Cycle timing is the same as I/O Read/Write Cycle except there are no automatic wait states (T_W), and $\overline{\text{MREQ}}$ is active instead of $\overline{\text{IORQ}}$.

Figure 20. CPU Timing (Opcode Fetch Cycle, Memory Read Cycle, Memory Write Cycle, I/O Write Cycle, I/O Read Cycle)

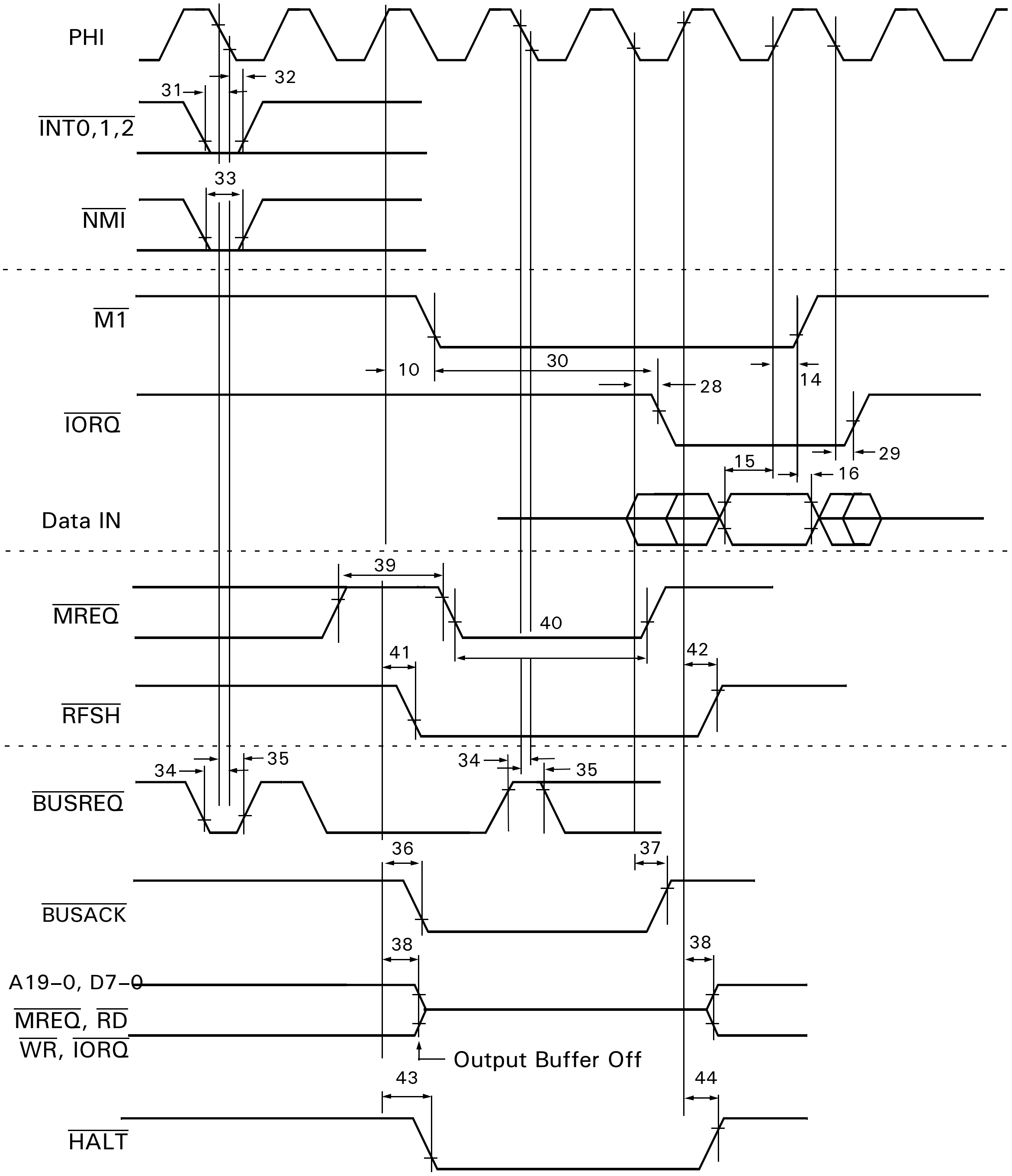


Figure 21. CPU Timing
(INT0 Acknowledge Cycle, Refresh Cycle, BUS RELEASE Mode, HALT Mode, SLEEP Mode, SYSTEM STOP Mode)

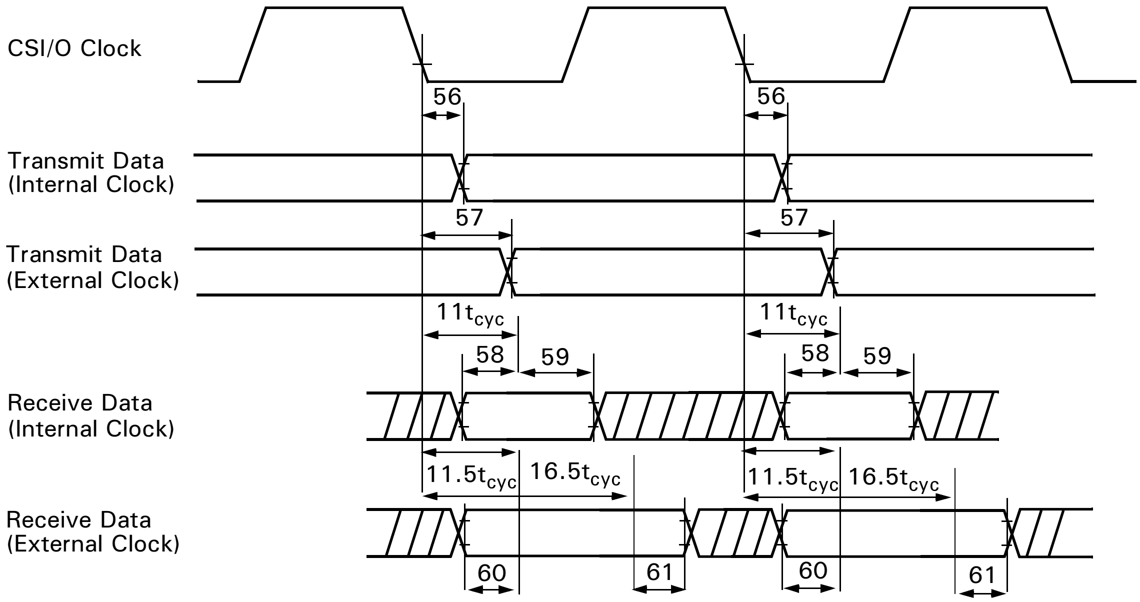
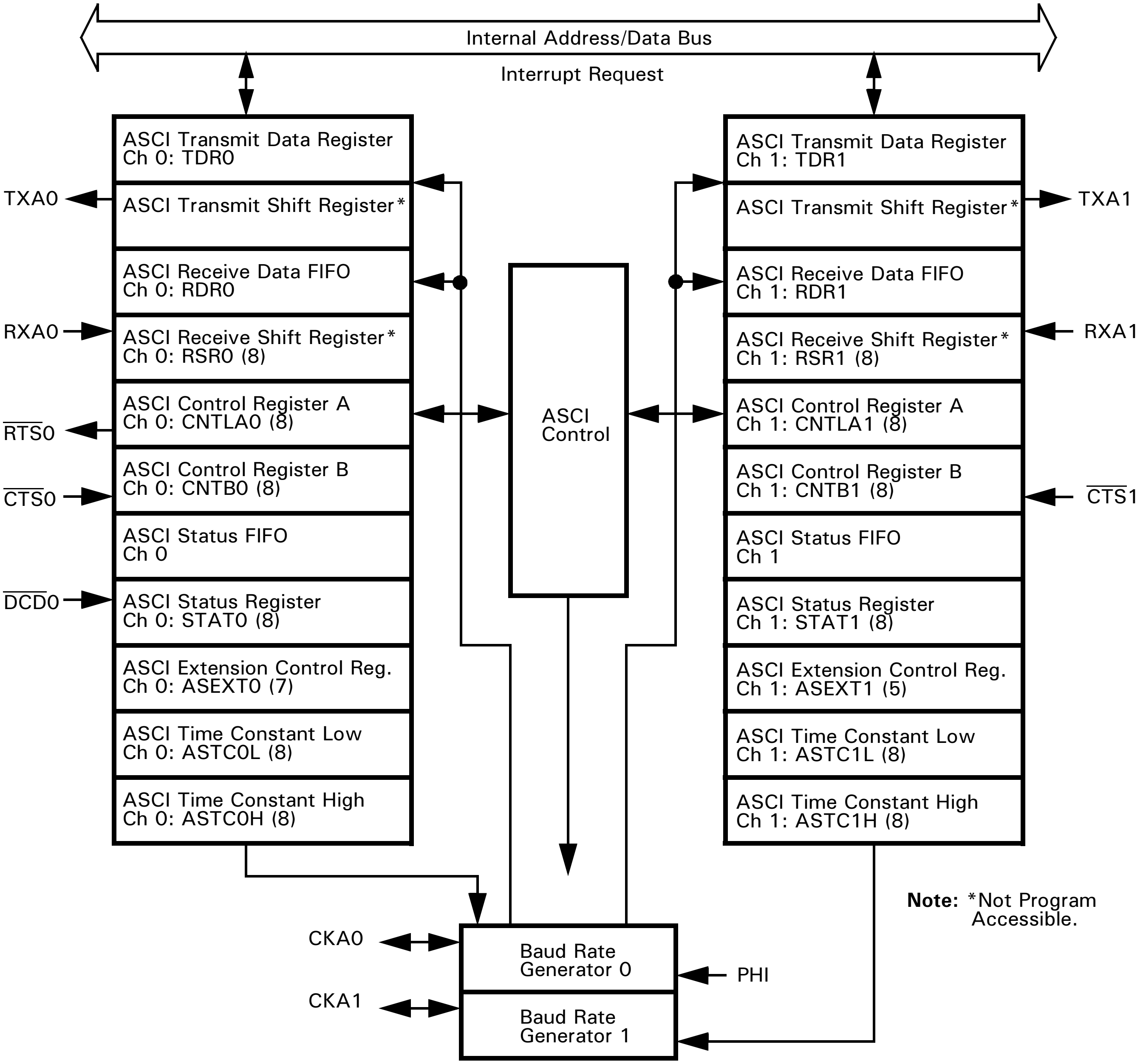


Figure 29. CSI/O Receive/Transmit Timing

Figure 30. Rise Time and Fall Times

ASCI REGISTER DESCRIPTION



Note: *Not Program Accessible.

Figure 32. ASCI Block Diagram

ASCI Transmit Shift Register 0,1. When the ASCI Transmit Shift Register (TSR) receives data from the ASCI Transmit Data Register (TDR), the data is shifted out to the TXA pin. When transmission is completed, the next byte (if available) is automatically loaded from TDR into TSR and the next transmission starts. If no data is available for transmission, TSR idles by outputting a continuous High level. This register is not program-accessible

ASCI Transmit Data Register 0,1 (TDR0, 1: I/O address = 06H, 07H). Data written to the ASCI Transmit Data Register is transferred to the TSR as soon as TSR is empty. Data can be written while TSR is shifting out the previous byte of data. Thus, the ASCI transmitter is double buffered.

Data can be written into and read from the ASCI Transmit Data Register. If data is read from the ASCI Transmit Data Register, the ASCI data transmit operation is not affected by this READ operation.

ASCI Receive Shift Register 0,1 (RSR0,1). This register receives data shifted in on the RXA pin. When full, data is automatically transferred to the ASCI Receive Data Register (RDR) if it is empty. If RSR is not empty when the next incoming data byte is shifted in, an overrun error occurs. This register is not program accessible.

ASCI Receive Data FIFO 0,1 (RDR0, 1:I/O Address = 08H, 09H). The ASCI Receive Data Register is a read-only register. When a complete incoming data byte is assembled in RSR, it is automatically transferred to the 4 character Receive Data First-In First-Out (FIFO) memory. The oldest character in the FIFO (if any) can be read from the Receive Data Register (RDR). The next incoming data byte can be shifted into RSR while the FIFO is full. Thus, the ASCI receiver is well buffered.

ASCI STATUS FIFO

This four-entry FIFO contains Parity Error, Framing Error, Rx Overrun, and Break status bits associated with each character in the receive data FIFO. The status of the oldest character (if any) can be read from the ASCI status registers.

ASCI CHANNEL CONTROL REGISTER A

ASCI Control Register A 0 (CNTLA0: I/O Address = 00H)

Bit	7	6	5	4	3	2	1	0
	MPE	RE	TE	$\overline{\text{RTS0}}$	MPBR/ EFR	MOD2	MOD1	MOD0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ASCI Control Register A 1 (CNTLA1: I/O Address = 01H)

Bit	7	6	5	4	3	2	1	0
	MPE	RE	TE	CKA1D	MPBR/ EFR	MOD2	MOD1	MOD0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 33. ASCI Channel Control Register A

MPE: Multi-Processor Mode Enable (Bit 7). The ASCI features a multiprocessor communication mode that utilizes an extra data bit for selective communication when a number of processors share a common serial bus. Multiprocessor data format is selected when the MP bit in CNTLB is set to 1. If multiprocessor mode is not selected (MP bit in CNTLB = 0), MPE has no effect. If multiprocessor mode is selected, MPE enables or disables the *wake-up* feature as follows. If MBE is set to 1, only received bytes in which the multiprocessor bit (MPB) = 1 can affect the RDRF and error flags. Effectively, other bytes (with MPB = 0) are *ignored* by the ASCI. If MPE is reset to 0, all bytes, regardless of the state of the MPB data bit, affect the REDR and error flags. MPE is cleared to 0 during RESET.

RE: Receiver Enable (Bit 6). When RE is set to 1, the ASCI transmitter is enabled. When TE is reset to 0, the transmitter is disables and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the previous contents of TDRE are held. TE is cleared to 0 in IOSTOP mode during RESET.

TE: Transmitter Enable (Bit 5). When TE is set to 1, the ASCI receiver is enabled. When $\overline{\text{TE}}$ is reset to 0, the transmitter is disabled and any transmit operation in progress is interrupted. However, the TDRE flag is not reset and the pre-

ASCI RECEIVE REGISTER

Register addresses 08H and 09H hold the ASCI receive data for channel 0 and channel 1, respectively.

ASCI Receive Register Channel 0

Mnemonic RDR0
Address 08H

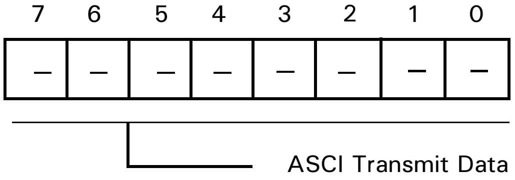


Figure 38. ASCI Receive Register Channel 0

ASCI Receive Register Channel 1

Mnemonic RDR1
Address 09H

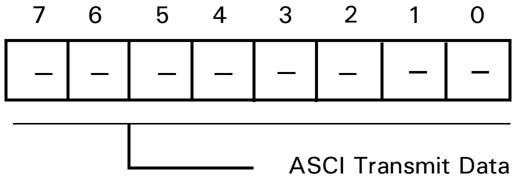


Figure 39. ASCI Receive Register Channel 1

CSI/O CONTROL/STATUS REGISTER

The CSI/O Control/Status Register (CNTR) is used to monitor CSI/O status, enable and disable the CSI/O, enable and disable interrupt generation, and select the data clock speed and source.

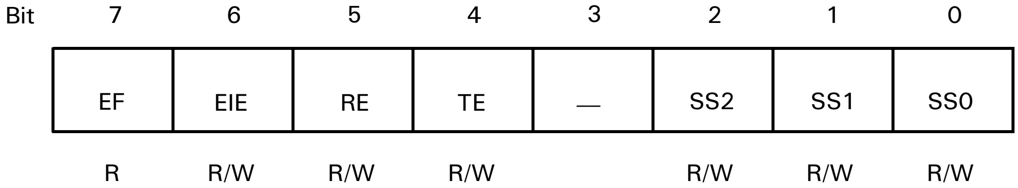


Figure 40. CSI/O Control Register (CNTR: I/O Address = 000AH)

EF: End Flag (Bit 7). EF is set to 1 by the CSI/O to indicate completion of an 8-bit data transmit or receive operation. If End Interrupt Enable (EIE) bit = 1 when EF is set to 1, a CPU interrupt request is generated. Program access of TRDR only occurs if EF = 1. The CSI/O clears EF to 0 when TRDR is read or written. EF is cleared to 0 during RESET and IOSTOP mode.

EIE: End Interrupt Enable (Bit 6). EIE is set to 1 to generate a CPU interrupt request. The interrupt request is inhibited if EIE is reset to 0. EIE is cleared to 0 during RESET.

RE: Receive Enable (Bit 5). A CSI/O receive operation is started by setting RE to 1. When RE is set to 1, the data clock is enabled. In internal clock mode, the data clock is output from the CKS pin. In external clock mode, the clock is input on the CKS pin. In either case, data is shifted in on the RXS pin in synchronization with the (internal or external) data clock. After receiving 8 bits of data, the CSI/O automatically clears RE to 0, EF is set to 1, and an interrupt (if enabled by EIE = 1) is generated. RE and TE are never both set to 1 at the same time. RE is cleared to 0 during RESET and IOSTOP mode.

TE: Transmit Enable (Bit 4). A CSI/O transmit operation is started by setting TE to 1. When TE is set to 1, the data clock is enabled. When in internal clock mode, the data clock is output from the CKS pin. In external clock mode, the clock is input on the CKS pin. In either case, data is shifted out on the TXS pin synchronous with the (internal or external) data clock. After transmitting 8 bits of data, the CSI/O automatically clears TE to 0, sets EF to 1, and requests an interrupt if enabled by EIE = 1. TE and RE are

ASCI EXTENSION CONTROL REGISTER CHANNEL 0 AND CHANNEL 1 (Continued)

Timer Data Register Channel 1 Low

Mnemonic TMDR1L
Address 14H

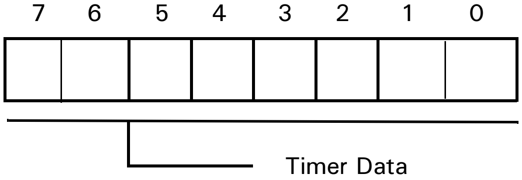


Figure 48. Timer Data Register 1 Low

Timer Data Register Channel 1 High

Mnemonic TMDR1H
Address 15H

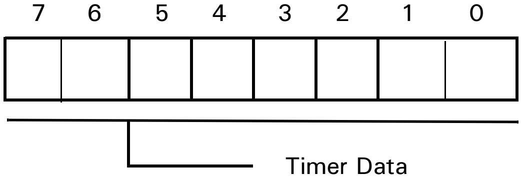


Figure 49. Timer Data Register 1 High

Timer Reload Register Channel 1 Low

Mnemonic RLDR1L
Address 16

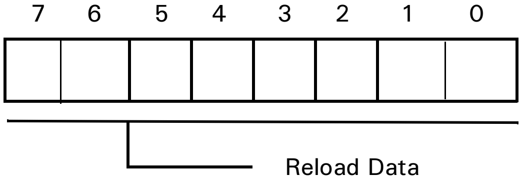


Figure 50. Timer Reload Channel 1 Low

Timer Reload Register Channel 1 High

Mnemonic RLDR1H
Address 17H

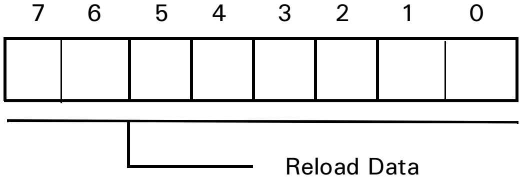


Figure 51. Timer Reload Register Channel 1 High

Free Running Counter (Read Only)

Mnemonic FRC
Address 18H

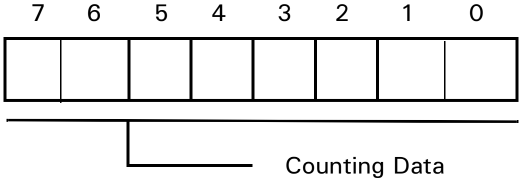


Figure 52. Free Running Counter

ASCI TIME CONSTANT REGISTERS

If the SS2–0 bits of the CNTLB register are not 111, and the BRG mode bit in the ASEXT register is 1, the ASCI divides the PHI clock by two times the registers' 16-bit value, plus two. As a result, the clock is presented to the transmitter and receiver for division by 1, 16, or 64, and is output on the CKA pin.

If the SS2–0 bits in an ASCI CNTLB register are not 111, and the BRG mode bit in its Extension Control Register is 1, its *new* baud rate generator divides PHI for serial clocking, as follows:

$$\text{bits/second} = f_{PHI}/(2*(TC+2) \text{ x sampling rate})$$

where TC is the 16-bit value programmed into the ASCI Time Constant High and Low registers. If the ASCI multiplexed CKA pin is selected for the CKA function, it outputs the clock before the final division by the sampling rate, as follows:

$$f_{CKAout} = f_{PHI}/(2*(TC+2))$$

Find the TC value for a particular serial bit rate as follows:

$$TC = (f_{PHI}/(2 \text{ x bits/second x sampling rate})) - 2$$

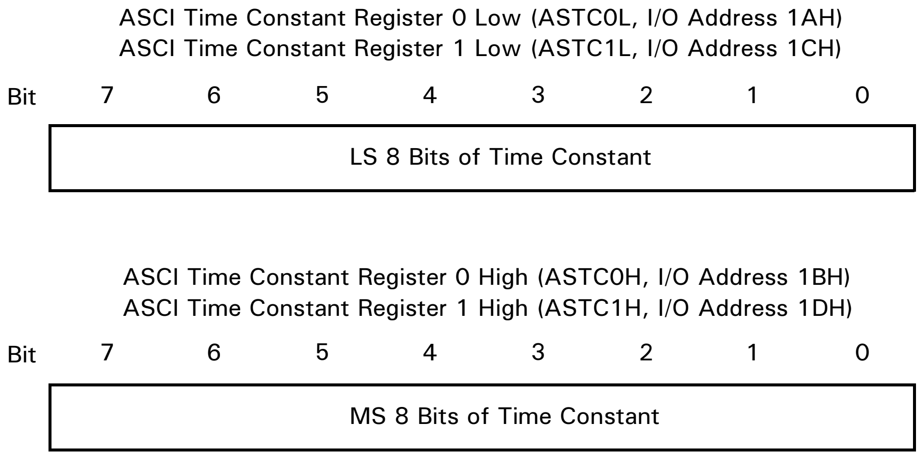


Figure 53. ASCI Time Constant Registers

DMA STATUS REGISTER

The DMA Status Register (DSTAT) is used to enable and disable DMA transfer and DMA termination interrupts. DSTAT also indicates DMA transfer status, Completed or In Progress.

DMA Status Register

Mnemonic DSTAT
Address 30H

Bit	7	6	5	4	3	2	1	0
	DE1	DE0	$\overline{\text{DWE1}}$	$\overline{\text{DWE0}}$	DIE1	DIE0	—	DME
	R/W	R/W	W	W	R/W	R/W		R

Figure 71. DMA Status Register (DSTAT: I/O Address = 30H)

DE1: DMA Enable Channel 1 (Bit 7). When DE1 = 1 and DME = 1, channel 1 DMA is enabled. When a DMA transfer terminates (BCR1 = 0), DE1 is reset to 0 by the DMAC. When DE1 = 0 and the DMA interrupt is enabled (DIE1 = 1), a DMA interrupt request is made to the CPU.

To perform a software WRITE to DE1, $\overline{\text{DWE1}}$ should be written with a 0 during the same register WRITE access. Writing DE1 to 0 disables channel 1 DMA, but DMA is restartable. Writing DE1 to 1 enables channel 1 DMA and automatically sets DMA Main Enable (DME) to 1. DE1 is cleared to 0 during RESET.

DE0: DMA Enable Channel 0 (Bit 6). When DE0 = 1 and DME = 1, channel 0 DMA is enabled. When a DMA transfer terminates (BCR0 = 0), DE0 is reset to 0 by the DMAC. When DE0 = 0 and the DMA interrupt is enabled (DIE0 = 1), a DMA interrupt request is made to the CPU.

To perform a software WRITE to DE0, $\overline{\text{DWE0}}$ should be written with 0 during the same register WRITE access. Writing DE0 to 0 disables channel 0 DMA. Writing DE0 to 1 enables channel 0 DMA and automatically sets DMA Main Enable (DME) to 1. DE0 is cleared to 0 during RESET.

$\overline{\text{DWE1}}$: DE1 Bit Write Enable (Bit 5). When performing any software WRITE to DE1, this bit should be written with 0 during the same access. $\overline{\text{DWE1}}$ always reads as 1.

$\overline{\text{DWE0}}$: DE0 Bit Write Enable (Bit 4). When performing any software WRITE to DE0, this bit should be written with 0 during the same access. $\overline{\text{DWE0}}$ always reads as 1.

DIE1: DMA Interrupt Enable Channel 1 (Bit 3). When DIE0 is set to 1, the termination channel 1 DMA transfer (indicated when DE1 = 0) causes a CPU interrupt request to be generated. When DIE0 = 0, the channel 0 DMA termination interrupt is disabled. DIE0 is cleared to 0 during RESET.

DIE0: DMA Interrupt Enable Channel 0 (Bit 2). When DIE0 is set to 1, the termination channel 0 of DMA transfer (indicated when DE0 = 0) causes a CPU interrupt request to be generated. When DIE0 = 0, the channel 0 DMA termination interrupt is disabled. DIE0 is cleared to 0 during RESET.

DME: DMA Main Enable (Bit 0). A DMA operation is only enabled when its DE bit (DE0 for channel 0, DE1 for channel 1) and the DME bit is set to 1.

When $\overline{\text{NMI}}$ occurs, DME is reset to 0, thus disabling DMA activity during the $\overline{\text{NMI}}$ interrupt service routine. To restart DMA, DE– and/or DE1 should be written with a 1 (even if the contents are already 1). This condition automatically sets DME to 1, allowing DMA operations to continue.

Note: DME cannot be directly written. The bit is cleared to 0 by $\overline{\text{NMI}}$ or indirectly set to 1 by setting DE0 and/or DE1 to 1. DME is cleared to 0 during RESET.

DMA/WAIT CONTROL REGISTER

The DMA/WAIT Control Register (DCNTL) controls the insertion of wait states into DMAC (and CPU) accesses of memory or I/O. Also, the register defines the Request signal for each channel as level or edge sense. DCNTL also sets the DMA transfer mode for channel 1, which is limited to memory to/from I/O transfers.

Bit	7	6	5	4	3	2	1	0
	MWI1	MWI0	IWI1	IWI0	DMS1	DMS0	DIM1	DIM0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 73. DMA/WAIT Control Register (DCNTL: I/O Address = 32H)

MWI1, MWI0: Memory Wait Insertion (Bits 7–6). This bit specifies the number of wait states introduced into CPU or DMAC memory access cycles. MWI1 and MWI0 are set to `1` during RESET.

MWI1	MWI0	Wait State
0	0	0
0	1	1
1	0	2
1	1	3

IWI1, IWI0: I/O Wait Insertion (Bits 5–4). This bit specifies the number of wait states introduced into CPU or DMAC I/O access cycles. IWI1 and IWI0 are set to `1` during RESET.

IWI1	IWI0	Wait State
0	0	1
0	1	2
1	0	3
1	1	4

Note: These wait states are added to the 3-clock I/O cycle that is used to access the on-chip I/O registers. It is equally valid to regard these as 0 to 3 wait states added to a 4-clock external I/O cycle.

DMS1, DMS0: DMA Request Sense (Bits 3–2). DMS1 and DMS0 specify the DMA request sense for channel 0 and channel 1 respectively. When reset to `0`, the input is level sense. When set to `1`, the input is edge sense. DMS1 and DMS0 are cleared to `0` during RESET.

DMSi	Sense
1	Edge Sense
0	Level Sense

Typically, for an input/source device, the associated DMS bit should be programmed as `0` for level sense. The device takes a relatively long time to update its Request signal after the DMA channel reads data (in the first of the two machine cycles involved in transferring a byte).

An output/destination device takes much less time to update its Request signal after the DMA channel starts a WRITE operation to it (the second machine cycle of the two cycles involved in transferring a byte). With zero-wait state I/O cycles, a device cannot update its request signal in the required time, so edge sensing must be used.

A one-wait-state I/O cycle also does not provide sufficient time for updating, so edge sensing is again required.

DIM1, DIM0: DMA Channel 1 I/O and Memory Mode (Bits 1–0). Specifies the source/destination and address modifier for channel 1 memory to/from I/O transfer modes. DIM1 and DIM0 are cleared to `0` during RESET.

Table 17. Channel 1 Transfer Mode

DIM1	DMI0	Transfer Mode	Address Increment/Decrement
0	0	Memory→I/O	MAR1 +1, IAR1 fixed
0	1	Memory→I/O	MAR1 –1, IAR1 fixed
1	0	I/O→Memory	IAR1 fixed, MAR1 +1
1	1	I/O→Memory	IAR1 fixed, MAR1 –1

All TRAPs occur after fetching an undefined second opcode byte following one of the prefix opcodes (`CBH`, `DDH`, `EDH`, or `FDH`) or after fetching an undefined third opcode byte following one of the double-prefix opcodes (`DDCBH` or `FDCBH`).

The state of the Undefined Fetch Object (UFO) bit in ITC allows TRAP software to correctly *adjust* the stacked PC, depending on whether the second or third byte of the opcode generated the TRAP. If `UFO = 0`, the starting address of the invalid instruction is the stacked `PC−1`. If `UFO = 1`, the starting address of the invalid instruction is equal to the stacked `PC−2`.

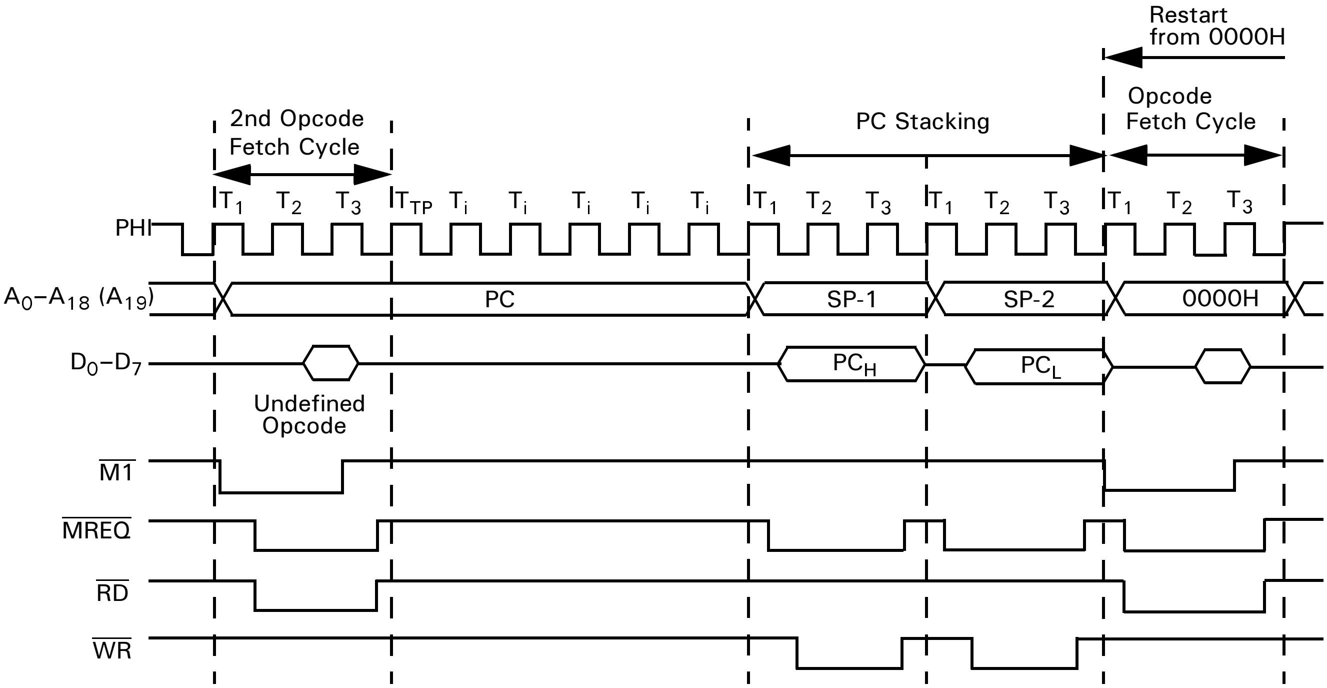


Figure 75. TRAP Timing—2nd Opcode Undefined

MMU COMMON BASE REGISTER

The Common Base Register (CBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical address for Common Area 1 accesses. All bits of CBR are reset to 0 during RESET.

MMU Common Base Register

Mnemonic CBR
Address 38H

Bit	7	6	5	4	3	2	1	0
	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 78. MMU Common Base Register (CBR: I/O Address = 38H)

MMU BANK BASE REGISTER

The Bank Base Register (BBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical address for Bank Area accesses. All bits of BBR are reset to 0 during RESET.

MMU Bank Base Register

Mnemonic BBR
Address 39H

Bit	7	6	5	4	3	2	1	0
	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 79. MMU Bank Base Register (BBR: I/O Address = 39H)

MMU COMMON/BANK AREA REGISTER

The Common/Bank Area Register (CBAR) specifies boundaries within the Z8S180/Z8L180 64-KB logical address space for up to three areas; Common Area), Bank Area and Common Area 1.

MMU Common/Bank Area Register

Mnemonic CBAR
Address 3AH

Bit	7	6	5	4	3	2	1	0
	CA3	CA2	CA1	CA0	BA3	BA2	BA1	BA0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 80. MMU Common/Bank Area Register (CBAR: I/O Address = 3AH)

CA3–CA0:CA (Bits 7–4). CA specifies the start (Low) address (on 4-KB boundaries) for Common Area 1. This condition also determines the most recent address of the Bank Area. All bits of CA are set to 1 during RESET.

BA3–BA0 (Bits 3–0). BA specifies the start (Low) address (on 4-KB boundaries) for the Bank Area. This condition also determines the most recent address of Common Area 0. All bits of BA are set to 1 during RESET.

OPERATION MODE CONTROL REGISTER

The Z8S180/Z8L180 is descended from two different ancestor processors, ZiLOG's original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR) can be programmed to select between certain differences between the Z80 and the 64180.

Operation Mode Control Register

Mnemonic OMCR
Address 3EH

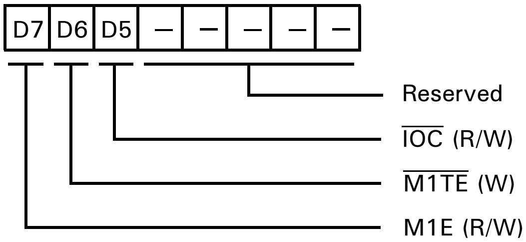


Figure 81. Operating Control Register (OMCR: I/O Address = 3EH)

M1E ($\overline{\text{M1}}$ Enable). This bit controls the $\overline{\text{M1}}$ output and is set to a 1 during reset.

When M1E = 1, the $\overline{\text{M1}}$ output is asserted Low during the opcode fetch cycle, the $\overline{\text{INT0}}$ acknowledge cycle, and the first machine cycle of the $\overline{\text{NMI}}$ acknowledge.

On the Z8S180/Z8L180, this choice makes the processor fetch one RETI instruction. When fetching a RETI from zero-wait-state memory, the processor uses three clock machine cycles that are not fully Z80-timing-compatible.

When M1E = 0, the processor does not drive $\overline{\text{M1}}$ Low during instruction fetch cycles. After fetching one RETI instruction with normal timing, the processor returns and refetches the instruction using Z80-compatible cycles that drive $\overline{\text{M1}}$ Low. This timing compatibility may be required by external Z80 peripherals to properly decode the RETI instruction.

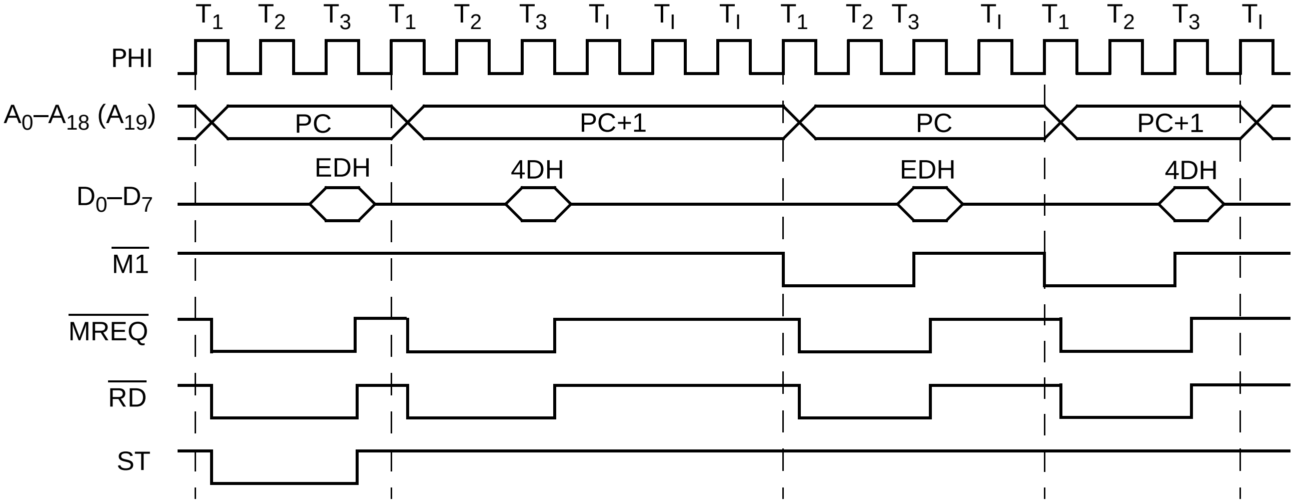


Figure 82. RETI Instruction Sequence with M1E = 0