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### Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	33MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	80-BQFP
Supplier Device Package	80-QFP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8s18033fsc00tr">https://www.e-xfl.com/product-detail/zilog/z8s18033fsc00tr</a>

PIN IDENTIFICATION

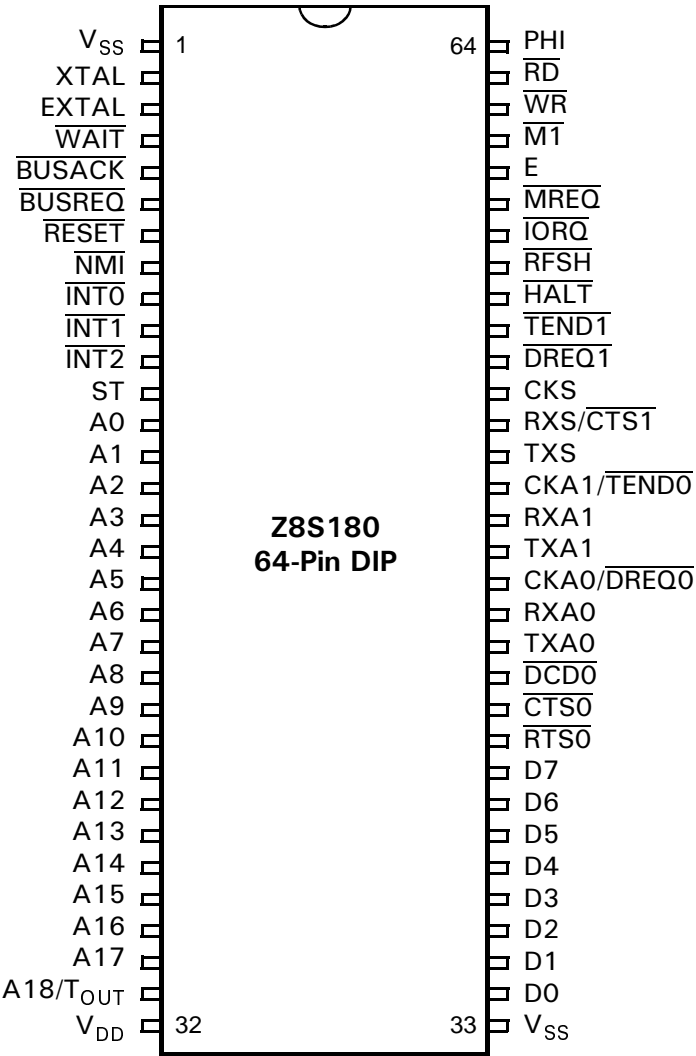


Figure 2. Z8S180 64-Pin DIP Pin Configuration

PIN IDENTIFICATION (Continued)

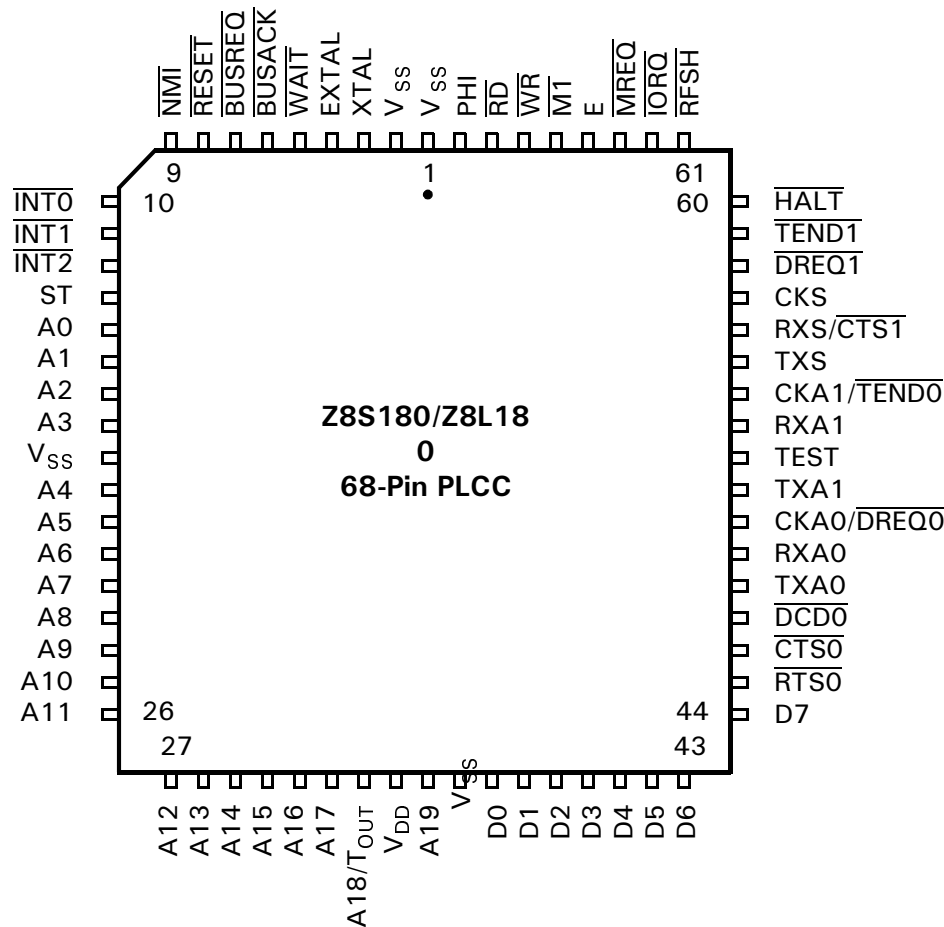


Figure 3. Z8S180/Z8L180 68-Pin PLCC Pin Configuration

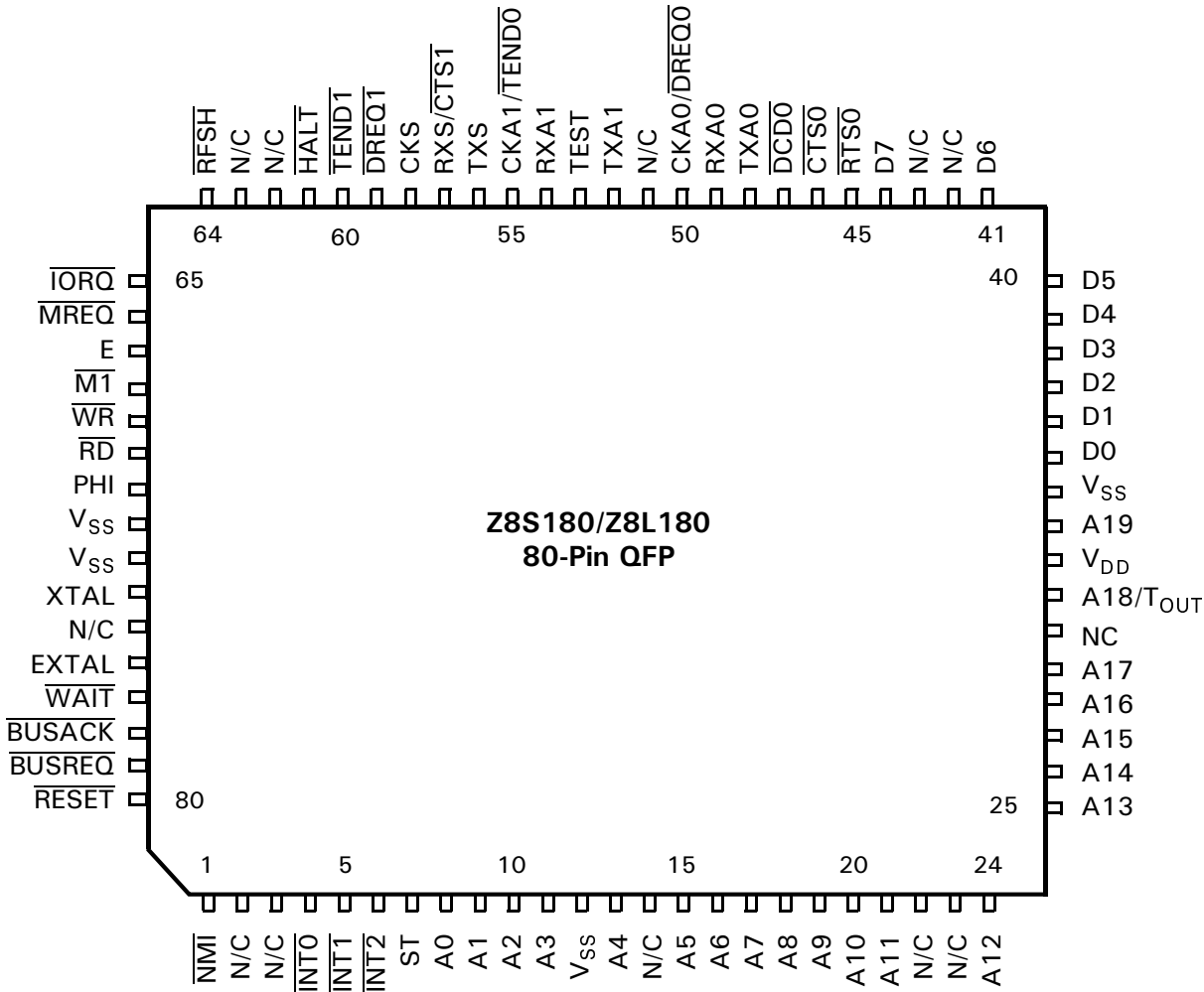


Figure 4. Z8S180/Z8L180 80-Pin QFP Pin Configuration

Table 1. Z8S180/Z8L180 Pin Identification

Pin Number and Package Type			Default Function	Secondary Function	Control
QFP	PLCC	DIP			
1	9	8	$\overline{\text{NMI}}$		
2			NC		
3			NC		
4	10	9	$\overline{\text{INT0}}$		
5	11	10	$\overline{\text{INT1}}$		
6	12	11	$\overline{\text{INT2}}$		
7	13	12	ST		
8	14	13	A0		
9	15	14	A1		
10	16	15	A2		
11	17	16	A3		
12	18		V <sub>SS</sub>		

## PIN IDENTIFICATION (Continued)

Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes

Pin Number and Package Type					Pin Status		
QFP	PLCC	DIP	Default Function	Secondary Function	RESET	BUSACK	SLEEP
1	9	8	$\overline{\text{NMI}}$		IN	IN	IN
2			NC				
3			NC				
4	10	9	$\overline{\text{INT0}}$		IN	IN	IN
5	11	10	$\overline{\text{INT1}}$		IN	IN	IN
6	12	11	$\overline{\text{INT2}}$		IN	IN	IN
7	13	12	ST		High	High	High
8	14	13	A0		3T	3T	High
9	15	14	A1		3T	3T	High
10	16	15	A2		3T	3T	High
11	17	16	A3		3T	3T	High
12	18		V <sub>SS</sub>		V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>
13	19	17	A4		3T	3T	High
14			NC				
15	20	18	A5		3T	3T	High
16	21	19	A6		3T	3T	High
17	22	20	A7		3T	3T	High
18	23	21	A8		3T	3T	High
19	24	22	A9		3T	3T	High
20	25	23	A10		3T	3T	High
21	26	24	A11		3T	3T	High
22			NC				
23			NC				
24	27	25	A12		3T	3T	High
25	28	26	A13		3T	3T	High
26	29	27	A14		3T	3T	High
27	30	28	A15		3T	3T	High
28	31	29	A16		3T	3T	High
29	32	30	A17		3T	3T	High
30			NC				
31	33	31	A18		3T	3T	High
			T <sub>OUT</sub>		N/A	OUT	OUT
32	34	32	V <sub>DD</sub>		V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DD</sub>
33	35		A19		3T	3T	High
34	36	33	V <sub>SS</sub>		V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>
35	37	34	D0		3T	3T	3T
36	38	35	D1		3T	3T	3T
37	39	36	D2		3T	3T	3T
38	40	37	D3		3T	3T	3T

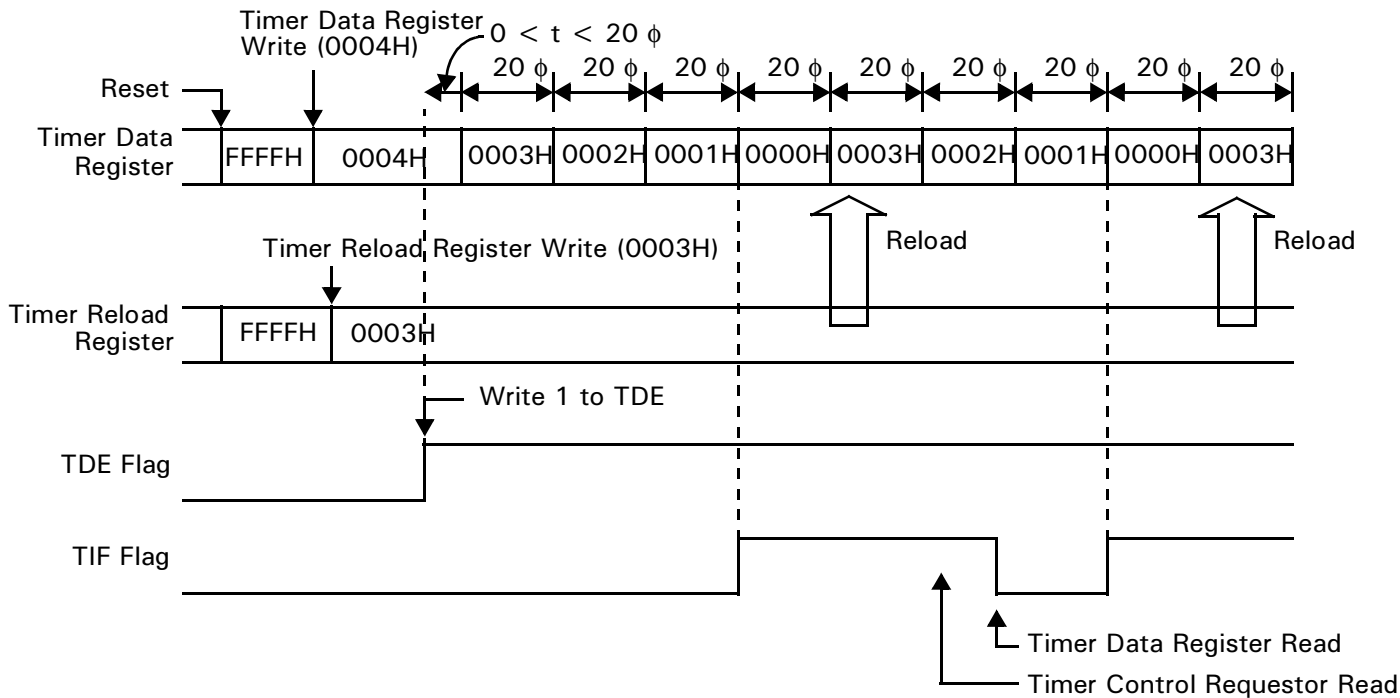


Figure 5. Timer Initialization, Count Down, and Reload Timing

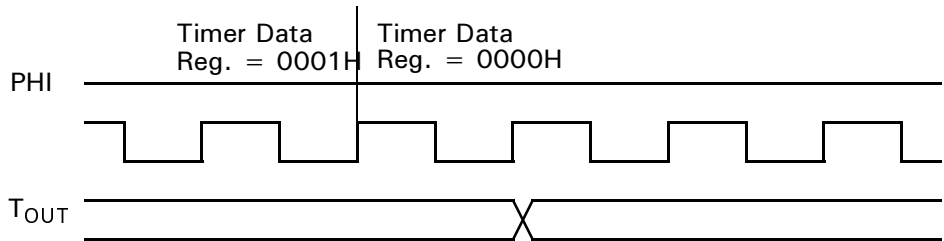


Figure 6. Timer Output Timing

**Clocked Serial I/O (CSI/O).** The CSI/O channel provides a half-duplex serial transmitter and receiver. This channel can be used for simple high-speed data connection to another microprocessor or microcomputer. TRDR is used for both CSI/O transmission and reception. Thus, the system design must ensure that the constraints of half-duplex operation are met (Transmit and Receive operation cannot occur simultaneously). For example, if a CSI/O transmission is attempted while the CSI/O is receiving data, a CSI/O does not work.

**Note:** TRDR is not buffered. Performing a CSI/O transmit while the previous transmission is still in progress causes the data to be immediately updated and corrupts the transmit operation. Similarly, reading TRDR while a transmit or receive is in progress should be avoided.

ARCHITECTURE (Continued)

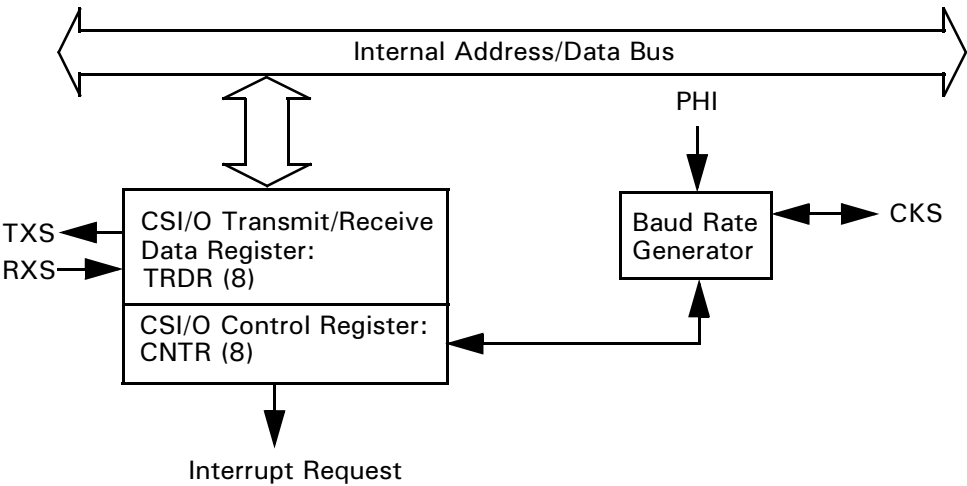


Figure 7. CSI/O Block Diagram

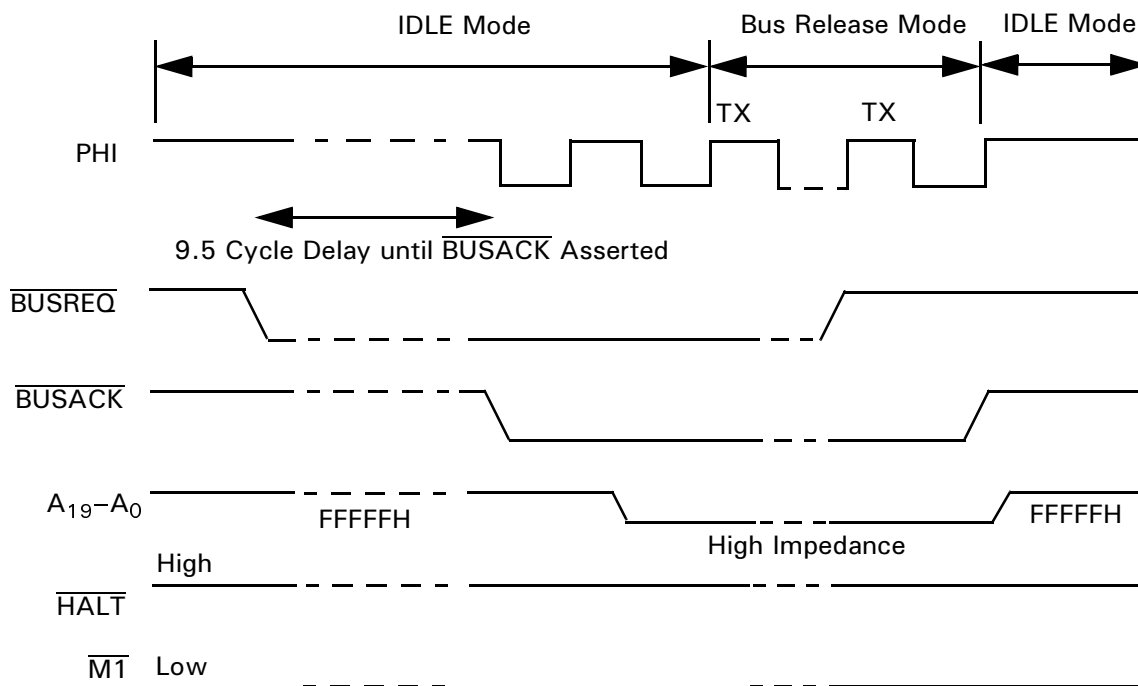


Figure 16. Bus Granting to External Master in IDLE Mode

**STANDBY Mode (With or Without QUICK RECOVERY).**

Software can put the Z8S180/Z8L180 into this mode by setting the IOSTOP bit (ICR5) to 1, CCR6 to 1, and executing the SLP instruction. This mode stops the on-chip oscillator and thus draws the least power of any mode, less than 10 $\mu$ A.

As with IDLE mode, the Z8S180/Z8L180 leaves STANDBY mode in response to a Low on  $\overline{\text{RESET}}$ , on  $\overline{\text{NMI}}$ , or a Low on  $\overline{\text{INT0-2}}$  that is enabled by a 1 in the corresponding bit in the INT/TRAP Control Register. This action grants the bus to an external Master if the BREXT bit in the CPU Control Register (CCR5) is 1. The time required for all of these operations is greatly increased by the necessity for restarting the on-chip oscillator, and ensuring that it stabilizes to square-wave operation.

When an external clock is connected to the EXTAL pin rather than a crystal to the XTAL and EXTAL pins and the external clock runs continuously, there is little necessity to use STANDBY mode because no time is required to restart the oscillator, and other modes restart faster. However, if external logic stops the clock during STANDBY mode (for example, by decoding  $\overline{\text{HALT}}$  Low and  $\overline{\text{M1}}$  High for several clock cycles), then STANDBY mode can be useful to allow the external clock source to stabilize after it is re-enabled.

When external logic drives  $\overline{\text{RESET}}$  Low to bring the device out of STANDBY mode, and a crystal is in use or an external clock source is stopped, the external logic must hold  $\overline{\text{RESET}}$  Low until the on-chip oscillator or external clock source is restarted and stabilized.

The clock-stability requirements of the Z8S180/Z8L180 are much less in the divide-by-two mode that is selected by a RESET sequence and controlled by the Clock Divide bit in the CPU Control Register (CCR7). As a result, software performs the following actions:

1. Sets CCR7 to 0 for divide-by-two mode before an SLP instruction and STANDBY mode.
2. Delays setting CCR7 back to 1 for divide-by-one mode as long as possible to allow additional clock stabilization time after a RESET, interrupt, or in-line RESTART after an SLP 01 instruction.

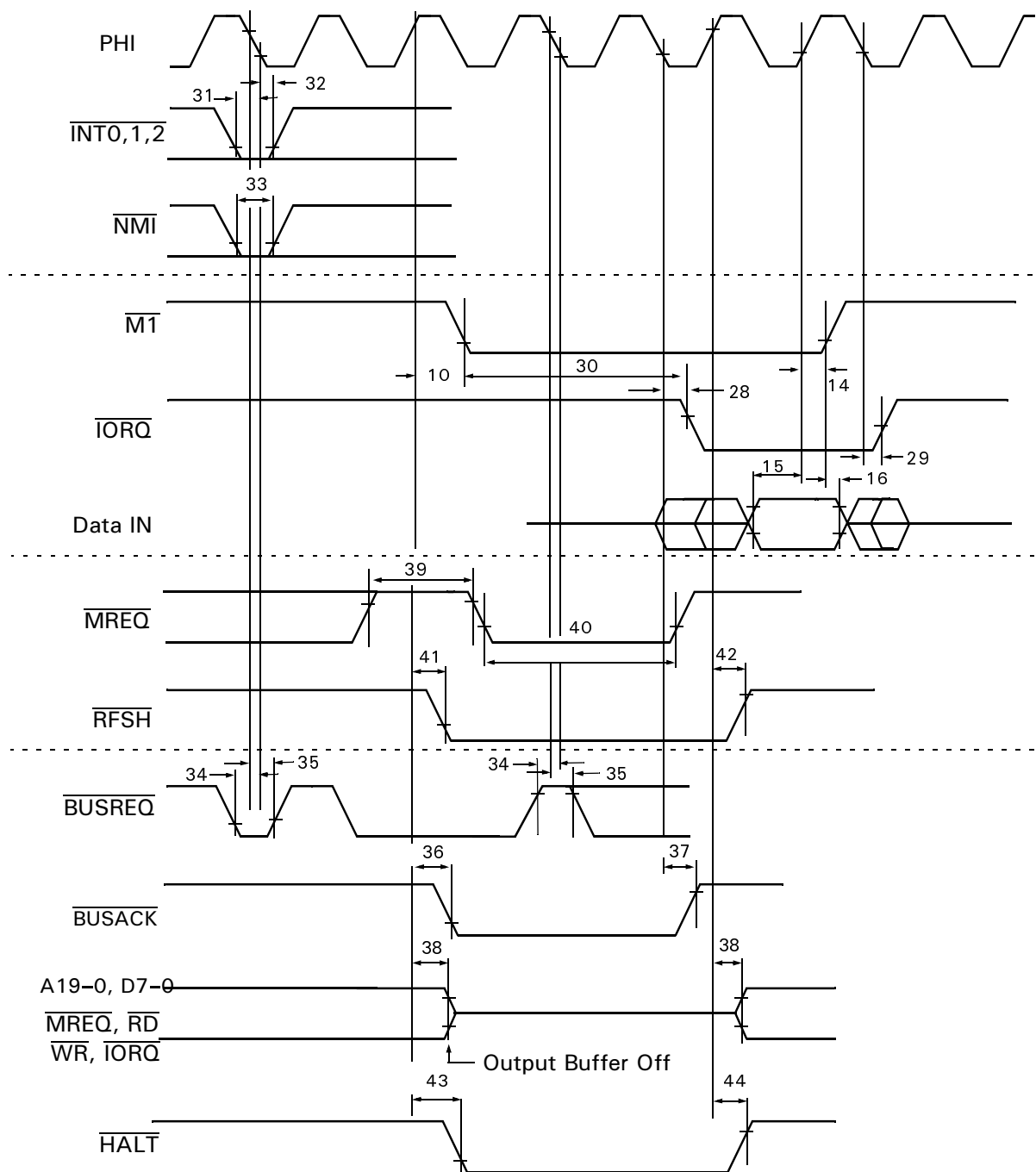
If CCR6 is set to 1 before the SLP instruction places the MPU in STANDBY mode, the value of the CCR3 bit determines the length of the delay before the oscillator restarts and stabilizes when it leaves STANDBY mode due to an external interrupt request. When CCR3 is 0, the Z8S180/Z8L180 waits  $2^{17}$  (131,072) clock cycles. When CCR3 is 1, it waits 64 clock cycles. This state is called QUICK RECOVERY mode. The same delay applies to grant-

## DC CHARACTERISTICS—Z8S180

Table 6. Z8S180 DC Characteristics  
 $V_{DD} = 5V \pm 10\%$ ;  $V_{SS} = 0V$ 

Symbol	Item	Condition	Min	Typ	Max	Unit
$V_{IH1}$	Input H Voltage $\overline{RESET}$ , $\overline{EXTAL}$ , $\overline{NMI}$		$V_{DD} - 0.6$	—	$V_{DD} + 0.3$	V
$V_{IH2}$	Input H Voltage Except $\overline{RESET}$ , $\overline{EXTAL}$ , $\overline{NMI}$		2.0	—	$V_{DD} + 0.3$	V
$V_{IH3}$	Input H Voltage CKS, CKA0, CKA1		2.4	—	$V_{DD} + 0.3$	V
$V_{IL1}$	Input L Voltage $\overline{RESET}$ , $\overline{EXTAL}$ , $\overline{NMI}$		-0.3	—	0.6	V
$V_{IL2}$	Input L Voltage Except $\overline{RESET}$ , $\overline{EXTAL}$ , $\overline{NMI}$		-0.3	—	0.8	V
$V_{OH}$	Outputs H Voltage All outputs	$I_{OH} = -200 \mu A$	2.4	—	—	V
		$I_{OH} = -20 \mu A$	$V_{DD} - 1.2$	—	—	
$V_{OL}$	Outputs L Voltage All outputs	$I_{OL} = 2.2 \text{ mA}$	—	—	0.45	V
$I_{IL}$	Input Leakage Current All Inputs Except XTAL, $\overline{EXTAL}$	$V_{IN} = 0.5 \sim V_{DD} - 0.5$	—	—	1.0	$\mu A$
$I_{TL}$	Three State Leakage Current	$V_{IN} = 0.5 \sim V_{DD} - 0.5$	—	—	1.0	$\mu A$
$I_{DD}^1$	Power Dissipation (Normal Operation)	F = 10 MHz	—	25	60	mA
		20		30	50	
		33		60	100	
	Power Dissipation (SYSTEM STOP mode)	F = 10 MHz	—	2	5	
		20		3	6	
		33		5	9	
$C_P$	Pin Capacitance	$V_{IN} = 0_V$ , $f = 1 \text{ MHz}$ $T_A = 25^\circ C$	—	—	12	pF

**Note:**1.  $V_{IHmin} = V_{DD} - 1.0V$ ,  $V_{ILmax} = 0.8V$  (All output terminals are at NO LOAD.)  $V_{DD} = 5.0V$ .



**Figure 21. CPU Timing**  
( $\overline{\text{INT0}}$  Acknowledge Cycle, Refresh Cycle, BUS RELEASE Mode,  
HALT Mode, SLEEP Mode, SYSTEM STOP Mode)

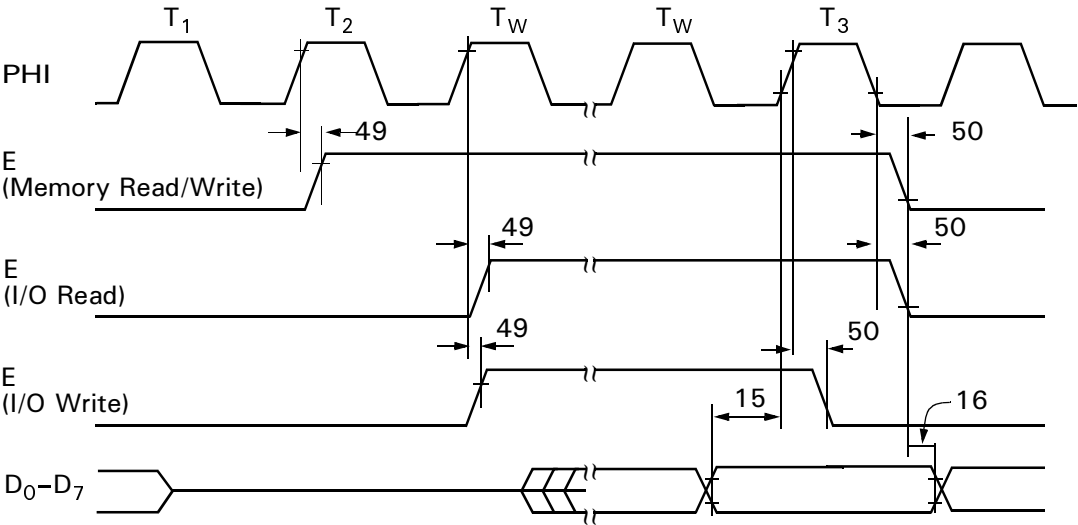


Figure 24. E Clock Timing  
(Memory Read/Write Cycle, I/O Read/Write Cycle)

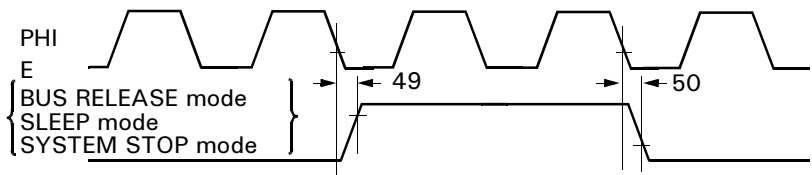


Figure 25. E Clock Timing  
(BUS RELEASE Mode, SLEEP Mode, SYSTEM STOP Mode)

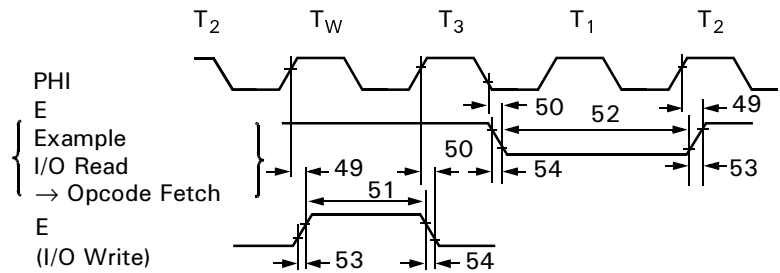


Figure 26. E Clock Timing  
(Minimum Timing Example of  $\text{P}_{\text{WEL}}$  and  $\text{P}_{\text{WEH}}$ )

TIMING DIAGRAMS (Continued)

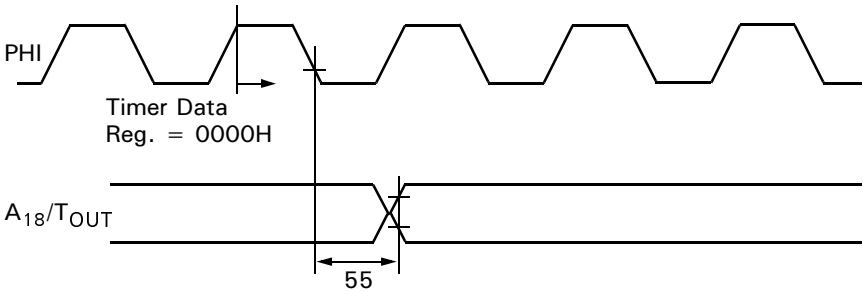


Figure 27. Timer Output Timing

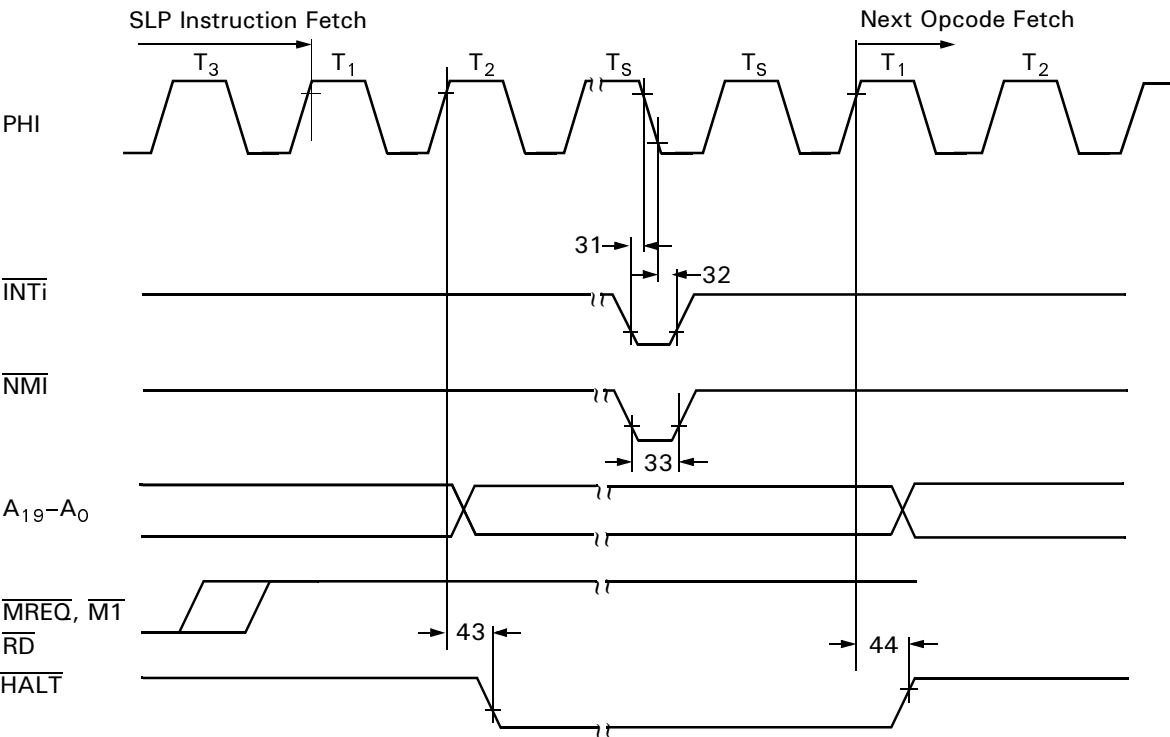


Figure 28. SLP Execution Cycle

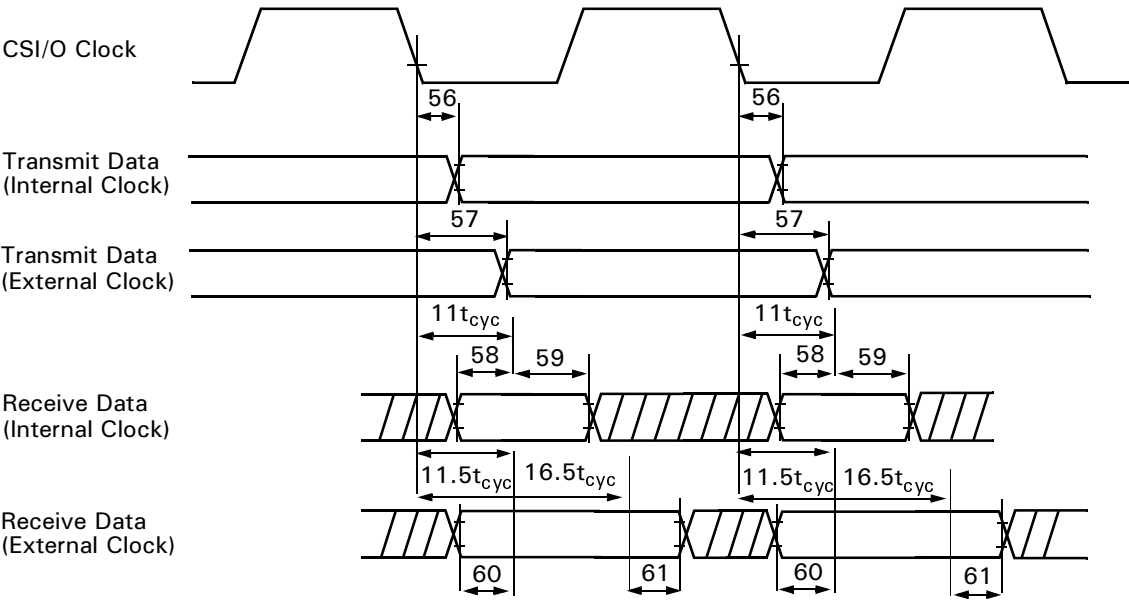


Figure 29. CSI/O Receive/Transmit Timing



Figure 30. Rise Time and Fall Times

ASCI REGISTER DESCRIPTION

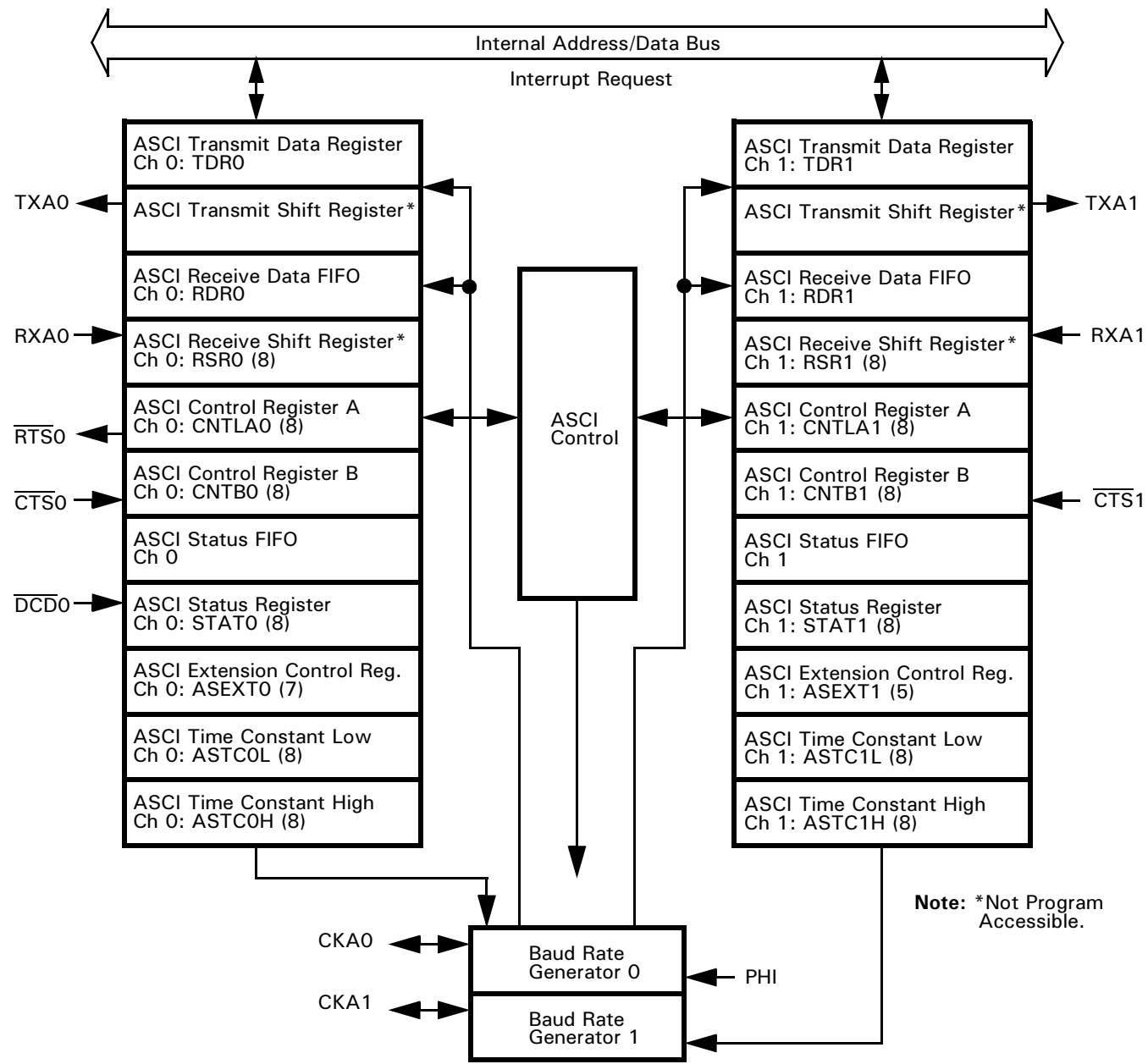


Figure 32. ASCI Block Diagram

**ASCI Transmit Shift Register 0,1.** When the ASCI Transmit Shift Register (TSR) receives data from the ASCI Transmit Data Register (TDR), the data is shifted out to the TXA pin. When transmission is completed, the next byte (if available) is automatically loaded from TDR into TSR and the next transmission starts. If no data is available for trans-

mission, TSR idles by outputting a continuous High level. This register is not program-accessible

**ASCI Transmit Data Register 0,1 (TDR0, 1: I/O address = 06H, 07H).** Data written to the ASCI Transmit Data Register is transferred to the TSR as soon as TSR is empty. Data can be written while TSR is shifting out the previous byte of data. Thus, the ASCI transmitter is double buffered.

ASCI0 requests an interrupt when  $\overline{\text{DCD0}}$  goes High. RIE is cleared to 0 by RESET.

**$\overline{\text{DCD0}}$ : Data Carrier Detect (Bit 2 STAT0).** This bit is set to 1 when the pin is High. It is cleared to 0 on the first READ of STAT0 following the pin's transition from High to Low and during RESET. When bit 6 of the ASEXTO register is 0 to select auto-enabling, and the pin is negated (High), the receiver is reset and its operation is inhibited.

**$\overline{\text{CTS1E}}$ : Clear To Send (Bit 2 STAT1).** Channel 1 features an external  $\overline{\text{CTS1}}$  input, which is multiplexed with the receive data pin RSX for the CSI/O. Setting this bit to 1 selects the CTS1 function; clearing the bit to 0 selects the RXS function.

**TDRE: Transmit Data Register Empty (Bit 1).** TDRE = 1 indicates that the TDR is empty and the next transmit data byte is written to TDR. After the byte is written to TDR, TDRE is cleared to 0 until the ASCI transfers the byte from TDR to the TSR and then TDRE is again set to 1. TDRE is set to 1 in IOSTOP mode and during RESET. On ASCI0, if the  $\overline{\text{CTS0}}$  pin is auto-enabled in the ASEXTO register and the pin is High, TDRE is reset to 0.

**TIE: Transmit Interrupt Enable (Bit 0).** TIE should be set to 1 to enable ASCI transmit interrupt requests. If TIE = 1, an interrupt is requested when TDRE = 1. TIE is cleared to 0 during RESET.

ASCI TRANSMIT DATA REGISTERS

Register addresses 06H and 07H hold the ASCI transmit data for channel 0 and channel 1, respectively.

ASCI Transmit Data Registers Channel 0

Mnemonic TDR0  
Address 06H

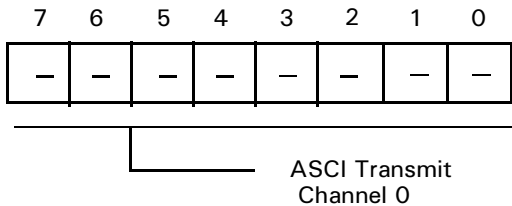


Figure 36. ASCII Register

ASCI Transmit Data Registers Channel 1

Mnemonic TDR1  
Address 07H

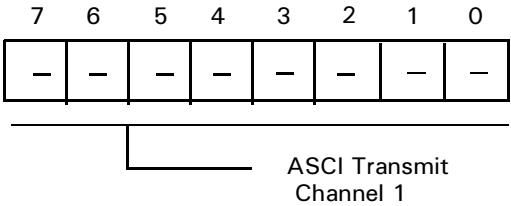


Figure 37. ASCII Register

ASCII RECEIVE REGISTER

Register addresses 08H and 09H hold the ASCII receive data for channel 0 and channel 1, respectively.

ASCII Receive Register Channel 0

Mnemonic RDR0  
Address 08H

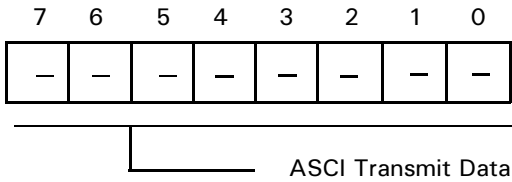


Figure 38. ASCII Receive Register Channel 0

ASCII Receive Register Channel 1

Mnemonic RDR1  
Address 09H

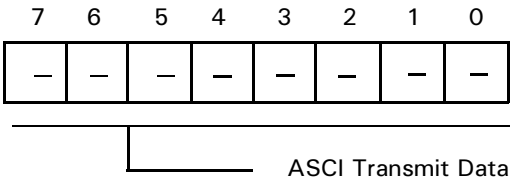


Figure 39. ASCII Receive Register Channel 1

CSI/O CONTROL/STATUS REGISTER

The CSI/O Control/Status Register (CNTR) is used to monitor CSI/O status, enable and disable the CSI/O, enable and

disable interrupt generation, and select the data clock speed and source.

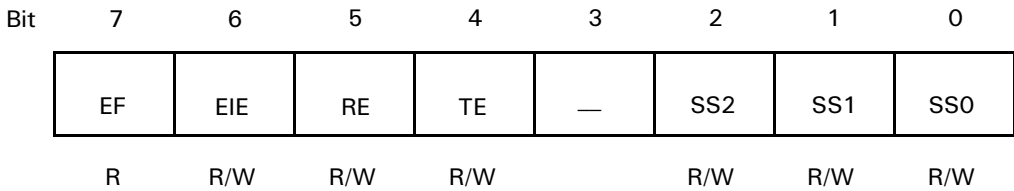


Figure 40. CSI/O Control Register (CNTR: I/O Address = 000AH)

**EF: End Flag (Bit 7).** EF is set to 1 by the CSI/O to indicate completion of an 8-bit data transmit or receive operation. If End Interrupt Enable (EIE) bit = 1 when EF is set to 1, a CPU interrupt request is generated. Program access of TRDR only occurs if EF = 1. The CSI/O clears EF to 0 when TRDR is read or written. EF is cleared to 0 during RESET and IOSTOP mode.

**EIE: End Interrupt Enable (Bit 6).** EIE is set to 1 to generate a CPU interrupt request. The interrupt request is inhibited if EIE is reset to 0. EIE is cleared to 0 during RESET.

**RE: Receive Enable (Bit 5).** A CSI/O receive operation is started by setting RE to 1. When RE is set to 1, the data clock is enabled. In internal clock mode, the data clock is output from the CKS pin. In external clock mode, the clock is input on the CKS pin. In either case, data is shifted in on the RXS

pin in synchronization with the (internal or external) data clock. After receiving 8 bits of data, the CSI/O automatically clears RE to 0, EF is set to 1, and an interrupt (if enabled by EIE = 1) is generated. RE and TE are never both set to 1 at the same time. RE is cleared to 0 during RESET and IOSTOP mode.

**TE: Transmit Enable (Bit 4).** A CSI/O transmit operation is started by setting TE to 1. When TE is set to 1, the data clock is enabled. When in internal clock mode, the data clock is output from the CKS pin. In external clock mode, the clock is input on the CKS pin. In either case, data is shifted out on the TXS pin synchronous with the (internal or external) data clock. After transmitting 8 bits of data, the CSI/O automatically clears TE to 0, sets EF to 1, and requests an interrupt if enabled by EIE = 1. TE and RE are

never both set to 1 at the same time. TE is cleared to 0 during RESET and IOSTOP mode.

**SS2, 1, 0: Speed Select 2, 1, 0 (Bits 2–0).** SS2, SS1 and SS0 select the CSI/O transmit/receive clock source and speed. SS2, SS1 and SS0 are all set to 1 during RESET. Table 11 indicates CSI/O Baud Rate Selection.

Table 11. CSI/O Baud Rate Selection

SS2	SS1	SS0	Divide Ratio
0	0	0	÷20
0	0	1	÷40
0	1	0	÷80
0	1	1	÷160
1	0	0	÷320
1	0	1	÷640
1	1	0	÷1280
1	1	1	External Clock Input (Less Than ÷20)

After RESET, the CKS pin is configured as an external clock input (SS2, SS1, SS0 = 1). Changing these values causes CKS to become an output pin and the selected clock is output when transmit or receive operations are enabled.

CSI/O Transmit/Receive Data Register

Mnemonic TRDR  
Address 0BH

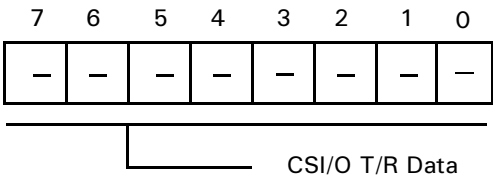


Figure 41. CSI/O Transmit/Receive Data Register

Timer Data Register Channel 0 Low

Mnemonic TMDR0L  
Address 0CH

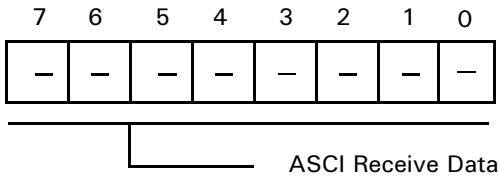


Figure 42. Timer Register Channel 0 Low

Timer Data Register Channel 0H

Mnemonic TMDR0H  
Address 0DH

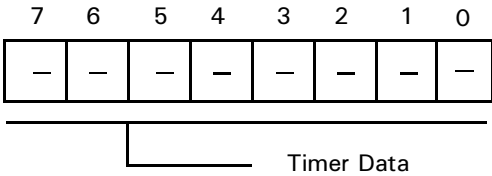


Figure 43. Timer Data Register Channel 0 High

Timer Reload Register Channel 0 Low

Mnemonic RLDR0L  
Address 0EH

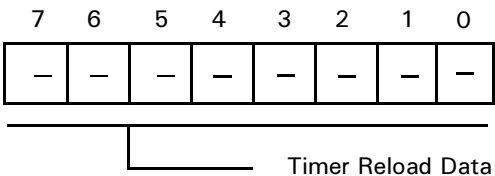


Figure 44. Timer Reload Register Low

Timer Reload Register Channel 0 High

Mnemonic RLDR0H  
Address 0FH

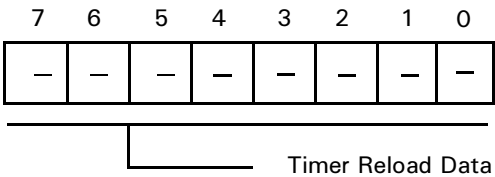


Figure 45. Timer Reload Register Channel 0 High

ASCI TIME CONSTANT REGISTERS

If the SS2–0 bits of the CNTLB register are not 111, and the BRG mode bit in the ASEX register is 1, the ASCI divides the PHI clock by two times the registers’ 16-bit value, plus two. As a result, the clock is presented to the transmitter and receiver for division by 1, 16, or 64, and is output on the CKA pin.

If the SS2–0 bits in an ASCI CNTLB register are not 111, and the BRG mode bit in its Extension Control Register is 1, its *new* baud rate generator divides PHI for serial clocking, as follows:

$$\text{bits/second} = f_{\text{PHI}} / (2 * (\text{TC} + 2) \times \text{sampling rate})$$

where TC is the 16-bit value programmed into the ASCI Time Constant High and Low registers. If the ASCI multiplexed CKA pin is selected for the CKA function, it outputs the clock before the final division by the sampling rate, as follows:

$$f_{\text{CKAout}} = f_{\text{PHI}} / (2 * (\text{TC} + 2))$$

Find the TC value for a particular serial bit rate as follows:

$$\text{TC} = (f_{\text{PHI}} / (2 \times \text{bits/second} \times \text{sampling rate})) - 2$$

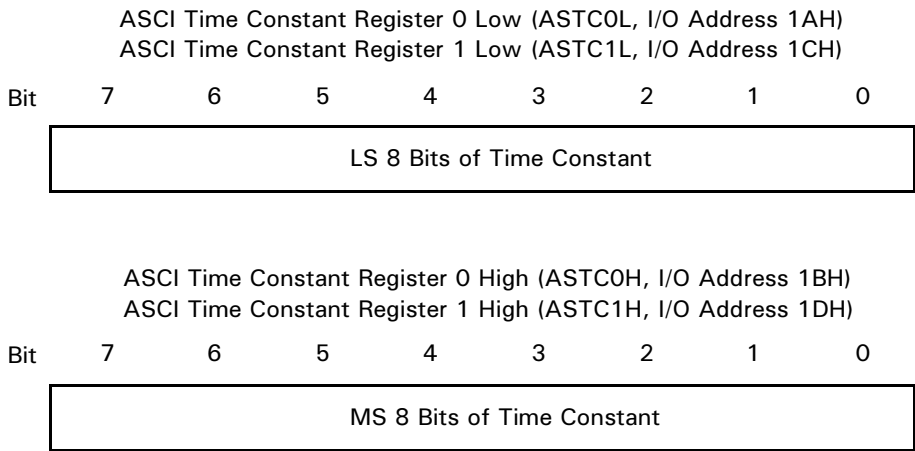


Figure 53. ASCI Time Constant Registers

DMA DESTINATION ADDRESS REGISTER CHANNEL 0

The DMA Destination Address Register Channel 0 specifies the physical destination address for channel 0 transfers. The register contains 20 bits and can specify up to 1024-KB memory addresses or up to 64-KB I/O addresses. Channel 0 destination can be memory, I/O, or memory mapped I/O. For I/O, the MS bits of this register identify the Request Handshake signal for channel 0.

DMA Destination Address Register Channel 0 Low

Mnemonic DAR0L  
Address 23H

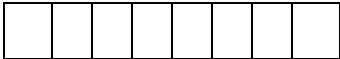


Figure 58. DMA Destination Address Register Channel 0 Low

DMA Destination Address Register Channel 0 High

Mnemonic DAR0H  
Address 24H

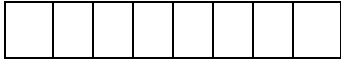


Figure 59. DMA Destination Address Register Channel 0 High

DMA Destination Address Register Channel 0B

Mnemonic DAR0B  
Address 25H

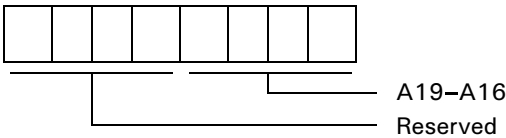


Figure 60. DMA Destination Address Register Channel 0B

If the DMA destination is in I/O space, bits 1–0 of this register select the DMA request signal for DMA0, as follows:

Bit 1 (A17)	Bit 0 (A16)	DMA Transfer Request
0	0	DREQ0 (external)
0	1	TDR0 (ASCI0)
1	0	TDR1 (ASCI1)
1	1	Not Used

DMA STATUS REGISTER

The DMA Status Register (DSTAT) is used to enable and disable DMA transfer and DMA termination interrupts.

DSTAT also indicates DMA transfer status, Completed or In Progress.

DMA Status Register

Mnemonic DSTAT  
Address 30H

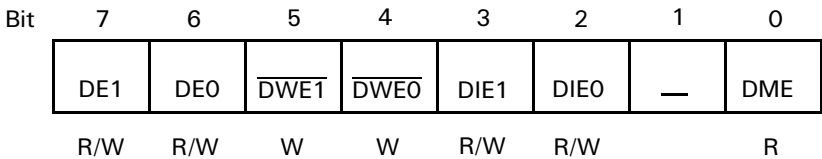


Figure 71. DMA Status Register (DSTAT: I/O Address = 30H)

**DE1: DMA Enable Channel 1 (Bit 7).** When DE1 = 1 and DME = 1, channel 1 DMA is enabled. When a DMA transfer terminates (BCR1 = 0), DE1 is reset to 0 by the DMAC. When DE1 = 0 and the DMA interrupt is enabled (DIE1 = 1), a DMA interrupt request is made to the CPU.

To perform a software WRITE to DE1,  $\overline{\text{DWE1}}$  should be written with a 0 during the same register WRITE access. Writing DE1 to 0 disables channel 1 DMA, but DMA is restartable. Writing DE1 to 1 enables channel 1 DMA and automatically sets DMA Main Enable (DME) to 1. DE1 is cleared to 0 during RESET.

**DE0: DMA Enable Channel 0 (Bit 6).** When DE0 = 1 and DME = 1, channel 0 DMA is enabled. When a DMA transfer terminates (BCR0 = 0), DE0 is reset to 0 by the DMAC. When DE0 = 0 and the DMA interrupt is enabled (DIE0 = 1), a DMA interrupt request is made to the CPU.

To perform a software WRITE to DE0,  $\overline{\text{DWE0}}$  should be written with 0 during the same register WRITE access. Writing DE0 to 0 disables channel 0 DMA. Writing DE0 to 1 enables channel 0 DMA and automatically sets DMA Main Enable (DME) to 1. DE0 is cleared to 0 during RESET.

**$\overline{\text{DWE1}}$ : DE1 Bit Write Enable (Bit 5).** When performing any software WRITE to DE1, this bit should be written with 0 during the same access.  $\overline{\text{DWE1}}$  always reads as 1.

**$\overline{\text{DWE0}}$ : DE0 Bit Write Enable (Bit 4).** When performing any software WRITE to DE0, this bit should be written with 0 during the same access.  $\overline{\text{DWE0}}$  always reads as 1.

**DIE1: DMA Interrupt Enable Channel 1 (Bit 3).** When DIE0 is set to 1, the termination channel 1 DMA transfer (indicated when DE1 = 0) causes a CPU interrupt request to be generated. When DIE0 = 0, the channel 0 DMA termination interrupt is disabled. DIE0 is cleared to 0 during RESET.

**DIE0: DMA Interrupt Enable Channel 0 (Bit 2).** When DIE0 is set to 1, the termination channel 0 of DMA transfer (indicated when DE0 = 0) causes a CPU interrupt request to be generated. When DIE0 = 0, the channel 0 DMA termination interrupt is disabled. DIE0 is cleared to 0 during RESET.

**DME: DMA Main Enable (Bit 0).** A DMA operation is only enabled when its DE bit (DE0 for channel 0, DE1 for channel 1) and the DME bit is set to 1.

When  $\overline{\text{NMI}}$  occurs, DME is reset to 0, thus disabling DMA activity during the  $\overline{\text{NMI}}$  interrupt service routine. To restart DMA, DE– and/or DE1 should be written with a 1 (even if the contents are already 1). This condition automatically sets DME to 1, allowing DMA operations to continue.

**Note:** DME cannot be directly written. The bit is cleared to 0 by  $\overline{\text{NMI}}$  or indirectly set to 1 by setting DE0 and/or DE1 to 1. DME is cleared to 0 during RESET.

MMU COMMON BASE REGISTER

The Common Base Register (CBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical address for Common Area 1 accesses. All bits of CBR are reset to 0 during RESET.

MMU Common Base Register

Mnemonic CBR  
Address 38H

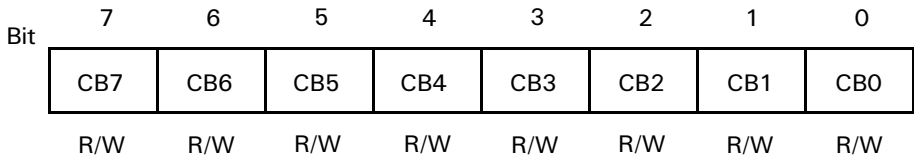


Figure 78. MMU Common Base Register (CBR: I/O Address = 38H)

MMU BANK BASE REGISTER

The Bank Base Register (BBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical address for Bank Area accesses. All bits of BBR are reset to 0 during RESET.

MMU Bank Base Register

Mnemonic BBR  
Address 39H

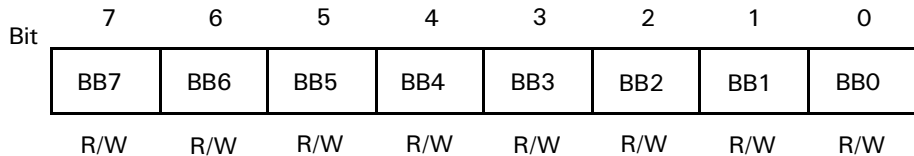


Figure 79. MMU Bank Base Register (BBR: I/O Address = 39H)

MMU COMMON/BANK AREA REGISTER

The Common/Bank Area Register (CBAR) specifies boundaries within the Z8S180/Z8L180 64-KB logical address space for up to three areas; Common Area), Bank Area and Common Area 1.

MMU Common/Bank Area Register

Mnemonic CBAR  
Address 3AH

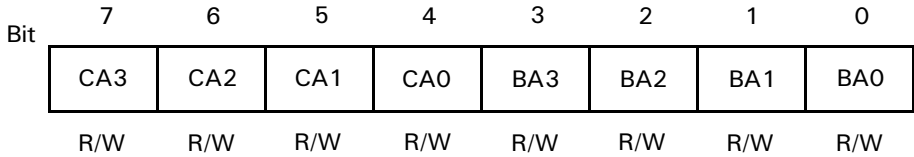


Figure 80. MMU Common/Bank Area Register (CBAR: I/O Address = 3AH)