**Welcome to E-XFL.COM**

## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z8S180 |
| Number of Cores/Bus Width | 1 Core, 8-Bit |
| Speed | 33MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 5.0V |
| Operating Temperature | -40°C ~ 100°C (TA) |
| Security Features | - |
| Package / Case | 68-LCC (J-Lead) |
| Supplier Device Package | 68-PLCC |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8s18033vec |

## GENERAL DESCRIPTION (Continued)

Power connections follow the conventional descriptions below:

| Connection | Circuit | Device |
|---|---|---|
| Power | $V_{CC}$ | $V_{DD}$ |
| Ground | GND | $V_{SS}$ |

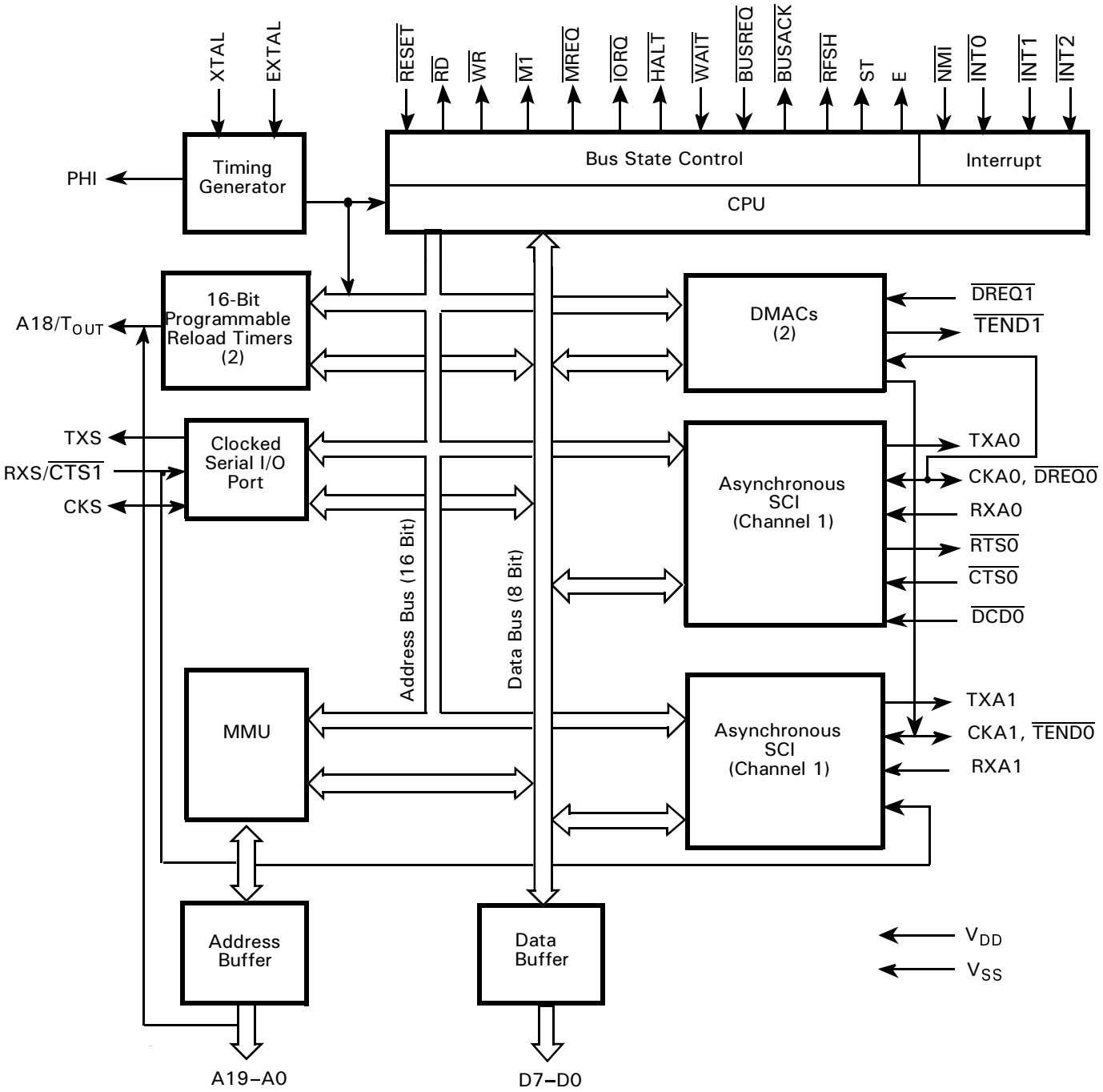



**Figure 1. Z8S180/Z8L180 Functional Block Diagram**

## PIN IDENTIFICATION

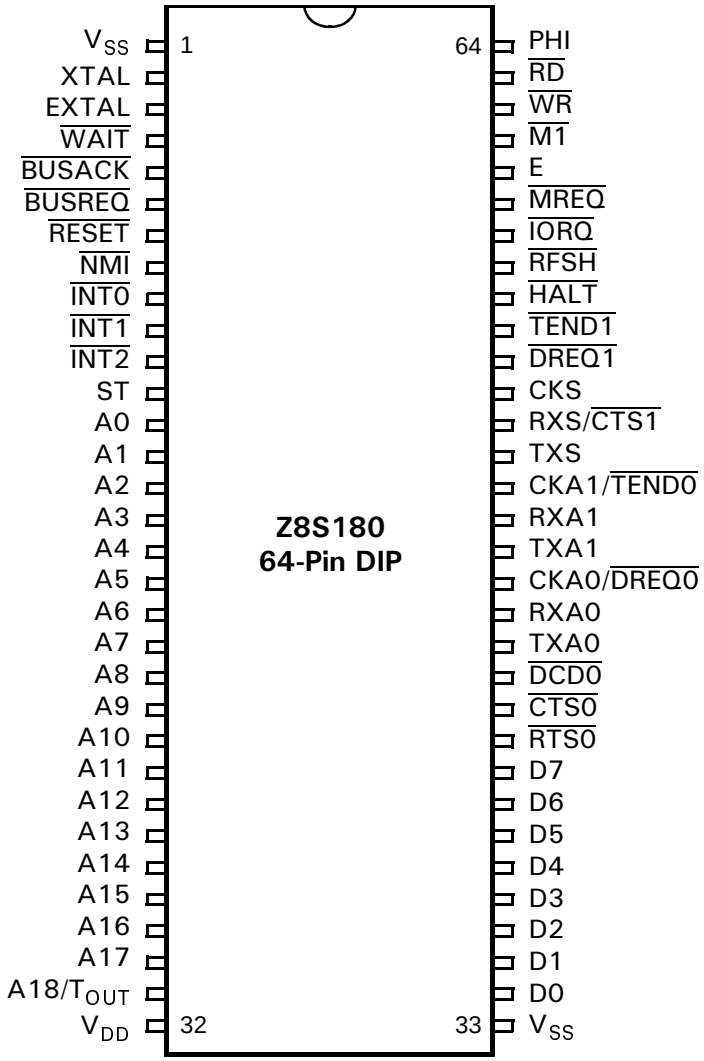



**Figure 2. Z8S180 64-Pin DIP Pin Configuration**

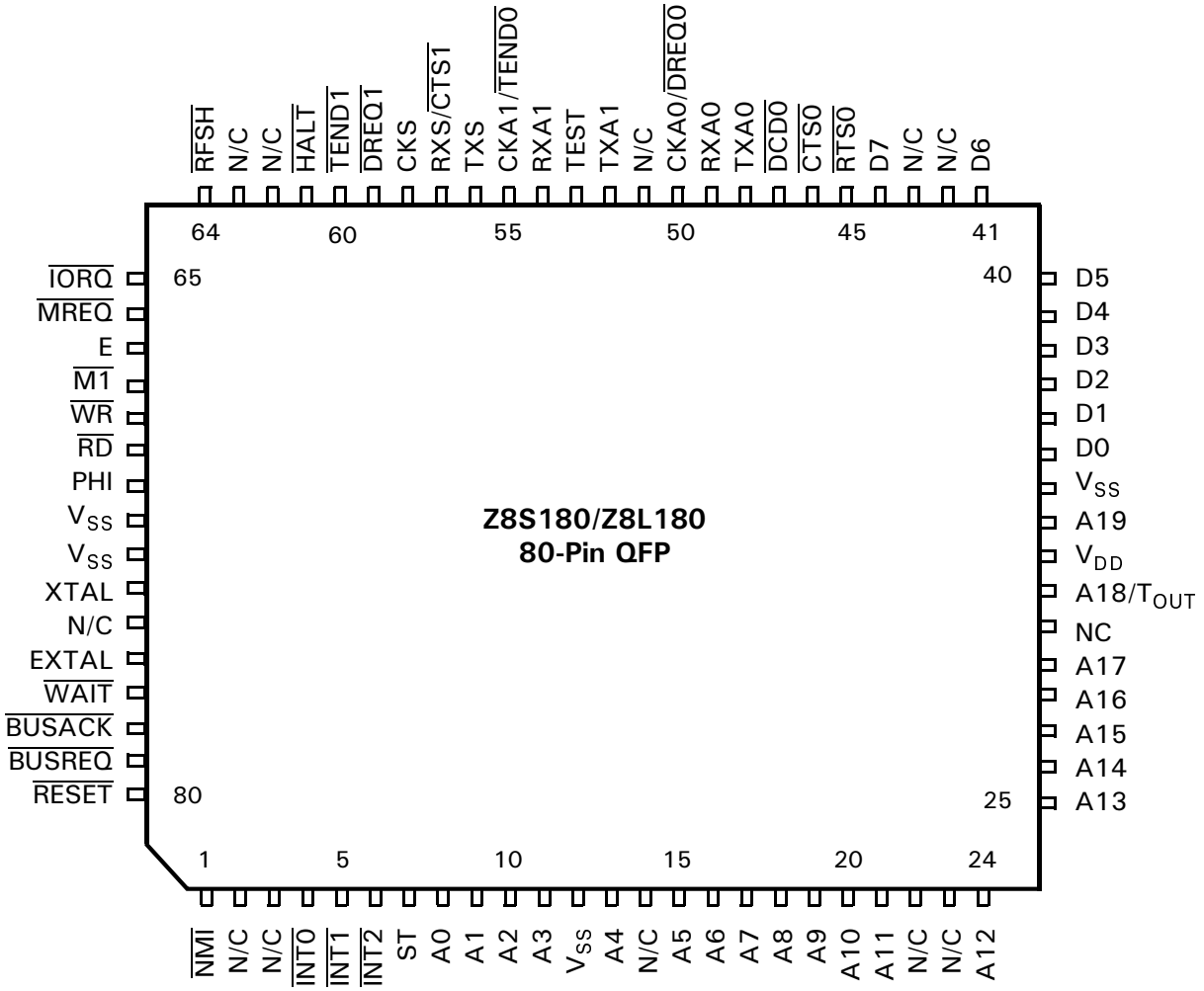



**Figure 4. Z8S180/Z8L180 80-Pin QFP Pin Configuration**

**Table 1. Z8S180/Z8L180 Pin Identification**

| Pin Number and Package Type | | | Default | Secondary | |
|---|---|---|---|---|---|
| QFP | PLCC | DIP | Function | Function | Control |
| 1 | 9 | 8 | $\overline{NMI}$ | | |
| 2 | | | NC | | |
| 3 | | | NC | | |
| 4 | 10 | 9 | $\overline{INT0}$ | | |
| 5 | 11 | 10 | $\overline{INT1}$ | | |
| 6 | 12 | 11 | $\overline{INT2}$ | | |
| 7 | 13 | 12 | ST | | |
| 8 | 14 | 13 | A0 | | |
| 9 | 15 | 14 | A1 | | |
| 10 | 16 | 15 | A2 | | |
| 11 | 17 | 16 | A3 | | |
| 12 | 18 | | $V_{SS}$ | | |

## PIN IDENTIFICATION (Continued)

**Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes**

| Pin Number and Package Type | | | | | Pin Status | | |
|---|---|---|---|---|---|---|---|
| QFP | PLCC | DIP | Default Function | Secondary Function | RESET | BUSACK | SLEEP |
| 1 | 9 | 8 | $\overline{NMI}$ | | IN | IN | IN |
| 2 | | | NC | | | | |
| 3 | | | NC | | | | |
| 4 | 10 | 9 | $\overline{INT0}$ | | IN | IN | IN |
| 5 | 11 | 10 | $\overline{INT1}$ | | IN | IN | IN |
| 6 | 12 | 11 | $\overline{INT2}$ | | IN | IN | IN |
| 7 | 13 | 12 | ST | | High | High | High |
| 8 | 14 | 13 | A0 | | 3T | 3T | High |
| 9 | 15 | 14 | A1 | | 3T | 3T | High |
| 10 | 16 | 15 | A2 | | 3T | 3T | High |
| 11 | 17 | 16 | A3 | | 3T | 3T | High |
| 12 | 18 | | $V_{SS}$ | | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ |
| 13 | 19 | 17 | A4 | | 3T | 3T | High |
| 14 | | | NC | | | | |
| 15 | 20 | 18 | A5 | | 3T | 3T | High |
| 16 | 21 | 19 | A6 | | 3T | 3T | High |
| 17 | 22 | 20 | A7 | | 3T | 3T | High |
| 18 | 23 | 21 | A8 | | 3T | 3T | High |
| 19 | 24 | 22 | A9 | | 3T | 3T | High |
| 20 | 25 | 23 | A10 | | 3T | 3T | High |
| 21 | 26 | 24 | A11 | | 3T | 3T | High |
| 22 | | | NC | | | | |
| 23 | | | NC | | | | |
| 24 | 27 | 25 | A12 | | 3T | 3T | High |
| 25 | 28 | 26 | A13 | | 3T | 3T | High |
| 26 | 29 | 27 | A14 | | 3T | 3T | High |
| 27 | 30 | 28 | A15 | | 3T | 3T | High |
| 28 | 31 | 29 | A16 | | 3T | 3T | High |
| 29 | 32 | 30 | A17 | | 3T | 3T | High |
| 30 | | | NC | | | | |
| 31 | 33 | 31 | A18 | | 3T | 3T | High |
| | | | $T_{OUT}$ | | N/A | OUT | OUT |
| 32 | 34 | 32 | $V_{DD}$ | | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ |
| 33 | 35 | | A19 | | 3T | 3T | High |
| 34 | 36 | 33 | $V_{SS}$ | | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ |
| 35 | 37 | 34 | D0 | | 3T | 3T | 3T |
| 36 | 38 | 35 | D1 | | 3T | 3T | 3T |
| 37 | 39 | 36 | D2 | | 3T | 3T | 3T |
| 38 | 40 | 37 | D3 | | 3T | 3T | 3T |

**Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)**

| Pin Number and Package Type | | | | | Pin Status | | |
|---|---|---|---|---|---|---|---|
| QFP | PLCC | DIP | Default Function | Secondary Function | RESET | BUSACK | SLEEP |
| 39 | 41 | 38 | D4 | | 3T | 3T | 3T |
| 40 | 42 | 39 | D5 | | 3T | 3T | 3T |
| 41 | 43 | 40 | D6 | | 3T | 3T | 3T |
| 42 | | | NC | | | | |
| 43 | | | NC | | | | |
| 44 | 44 | 41 | D7 | | 3T | 3T | 3T |
| 45 | 45 | 42 | $\overline{RTS0}$ | | High | OUT | High |
| 46 | 46 | 43 | $\overline{CTS0}$ | | IN | OUT | IN |
| 47 | 47 | 44 | $\overline{DCD0}$ | | IN | IN | IN |
| 48 | 48 | 45 | TXA0 | | High | OUT | OUT |
| 49 | 49 | 46 | RXA0 | | IN | IN | IN |
| 50 | 50 | 47 | CKA0 | | 3T | I/O | I/O |
| | | | $\overline{DREQ0}$ | | N/A | IN | IN |
| 51 | | | NC | | | | |
| 52 | 51 | 48 | TXA1 | | High | OUT | OUT |
| 53 | 52 | | TEST | | | | |
| 54 | 53 | 49 | RXA1 | | IN | IN | IN |
| 55 | 54 | 50 | CKA1 | | 3T | I/O | I/O |
| | | | $\overline{TEND0}$ | | N/A | High | High |
| 56 | 55 | 51 | TXS | | High | OUT | OUT |
| 57 | 56 | 52 | RXS | | IN | IN | IN |
| | | | $\overline{CTS1}$ | | N/A | IN | IN |
| 58 | 57 | 53 | CKS | | 3T | I/O | I/O |
| 59 | 58 | 54 | $\overline{DREQ1}$ | | IN | 3T | IN |
| 60 | 59 | 55 | $\overline{TEND1}$ | | High | OUT | High |
| 61 | 60 | 56 | $\overline{HALT}$ | | High | High | Low |
| 62 | | | NC | | | | |
| 63 | | | NC | | | | |
| 64 | 61 | 57 | $\overline{RFSH}$ | | High | OUT | High |
| 65 | 62 | 58 | $\overline{IORQ}$ | | High | 3T | High |
| 66 | 63 | 59 | $\overline{MREQ}$ | | High | 3T | High |
| 67 | 64 | 60 | E | | Low | OUT | OUT |
| 68 | 65 | 61 | $\overline{M1}$ | | High | High | High |
| 69 | 66 | 62 | $\overline{WR}$ | | High | 3T | High |
| 70 | 67 | 63 | $\overline{RD}$ | | High | 3T | High |
| 71 | 68 | 64 | PHI | | OUT | OUT | OUT |
| 72 | 1 | 1 | $V_{SS}$ | | GND | GND | GND |
| 73 | 2 | | $V_{SS}$ | | GND | GND | GND |
| 74 | 3 | 2 | XTAL | | OUT | OUT | OUT |
| 75 | | | NC | | | | |

**ARCHITECTURE** (Continued)

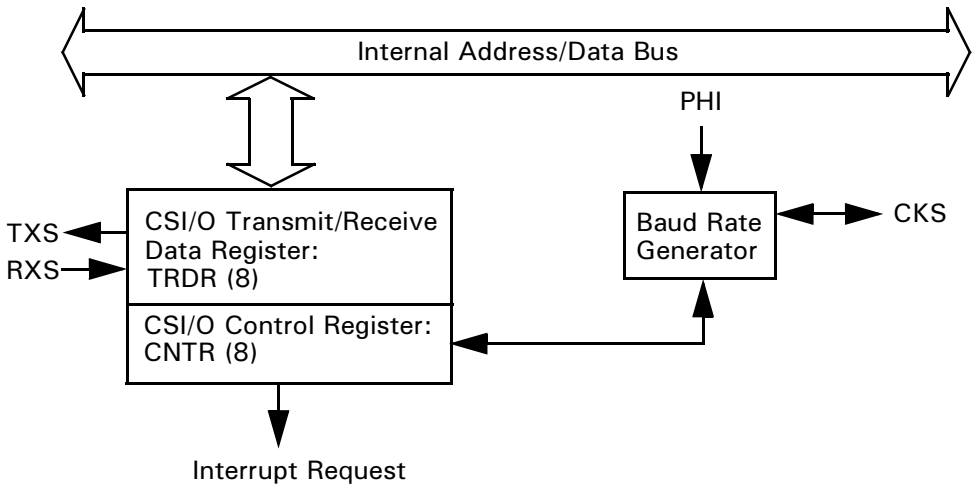



**Figure 7. CSI/O Block Diagram**

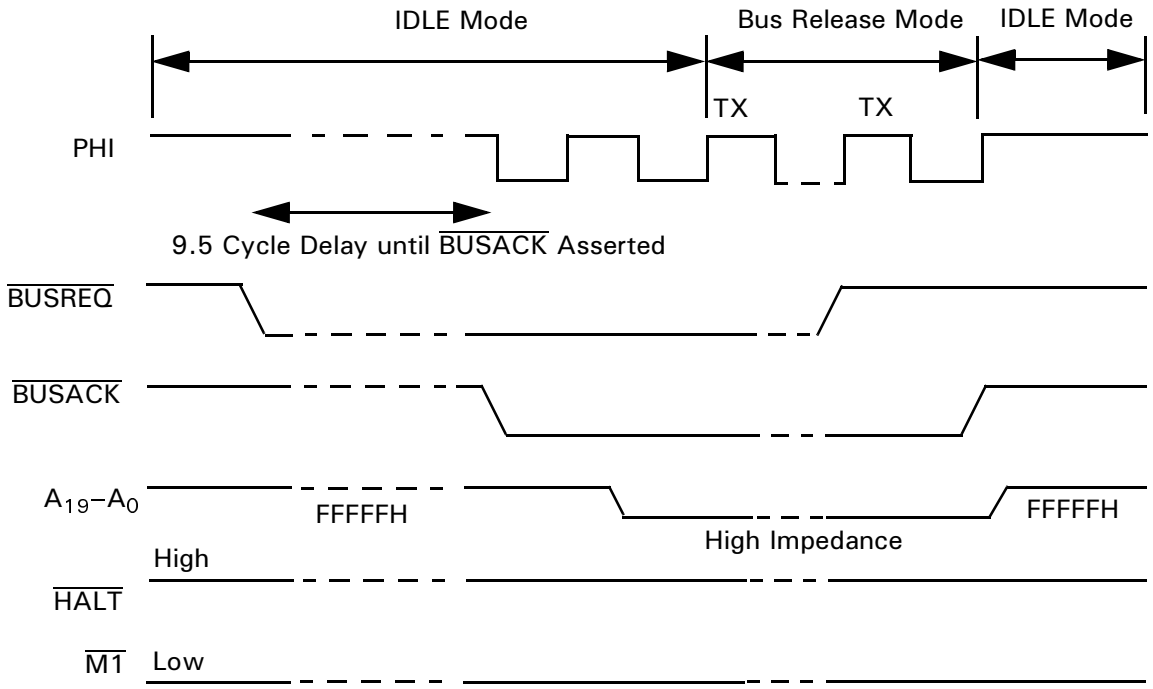



**Figure 16. Bus Granting to External Master in IDLE Mode**

**STANDBY Mode (With or Without QUICK RECOVERY).**

Software can put the Z8S180/Z8L180 into this mode by setting the IOSTOP bit (ICR5) to 1, CCR6 to 1, and executing the SLP instruction. This mode stops the on-chip oscillator and thus draws the least power of any mode, less than 10µA.

As with IDLE mode, the Z8S180/Z8L180 leaves STANDBY mode in response to a Low on $\overline{\text{RESET}}$, on $\overline{\text{NMI}}$, or a Low on $\overline{\text{INT0–2}}$ that is enabled by a 1 in the corresponding bit in the INT/TRAP Control Register. This action grants the bus to an external Master if the BREXT bit in the CPU Control Register (CCR5) is 1. The time required for all of these operations is greatly increased by the necessity for restarting the on-chip oscillator, and ensuring that it stabilizes to square-wave operation.

When an external clock is connected to the EXTAL pin rather than a crystal to the XTAL and EXTAL pins and the external clock runs continuously, there is little necessity to use STANDBY mode because no time is required to restart the oscillator, and other modes restart faster. However, if external logic stops the clock during STANDBY mode (for example, by decoding $\overline{\text{HALT}}$ Low and $\overline{\text{M1}}$ High for several clock cycles), then STANDBY mode can be useful to allow the external clock source to stabilize after it is re-enabled.

When external logic drives $\overline{\text{RESET}}$ Low to bring the device out of STANDBY mode, and a crystal is in use or an external clock source is stopped, the external logic must hold $\overline{\text{RESET}}$ Low until the on-chip oscillator or external clock source is restarted and stabilized.

The clock-stability requirements of the Z8S180/Z8L180 are much less in the divide-by-two mode that is selected by a RESET sequence and controlled by the Clock Divide bit in the CPU Control Register (CCR7). As a result, software performs the following actions:

1. Sets CCR7 to 0 for divide-by-two mode before an SLP instruction and STANDBY mode.
2. Delays setting CCR7 back to 1 for divide-by-one mode as long as possible to allow additional clock stabilization time after a RESET, interrupt, or in-line RESTART after an SLP 01 instruction.

If CCR6 is set to 1 before the SLP instruction places the MPU in STANDBY mode, the value of the CCR3 bit determines the length of the delay before the oscillator restarts and stabilizes when it leaves STANDBY mode due to an external interrupt request. When CCR3 is 0, the Z8S180/Z8L180 waits $2^{17}$ (131,072) clock cycles. When CCR3 is 1, it waits 64 clock cycles. This state is called QUICK RECOVERY mode. The same delay applies to grant-

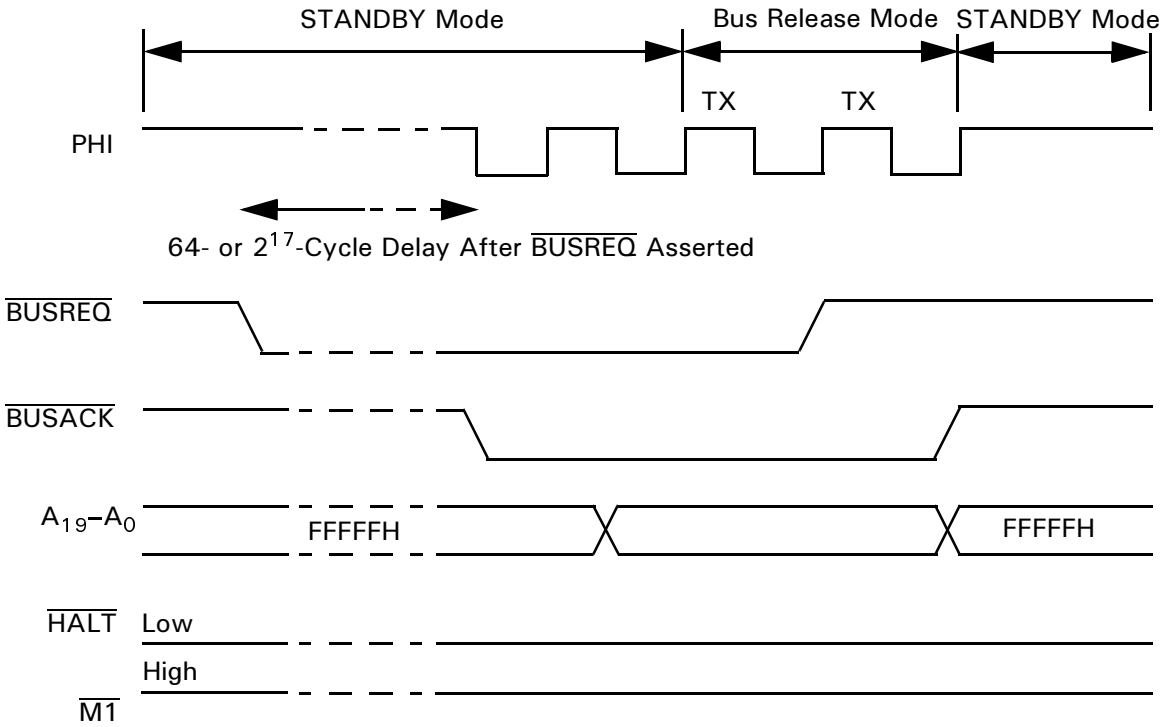



**Figure 18. Bus Granting to External Master During STANDBY Mode**

## STANDARD TEST CONDITIONS

The following standard test conditions apply to DC Characteristics, unless otherwise noted. All voltages are referenced to $V_{SS}$ (0V). Positive current flows into the referenced pin.

All AC parameters assume a load capacitance of 100 pF. Add a 10-ns delay for each 50-pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to $V_{OL}$ MAX or $V_{OL}$ MIN as indicated in Figures 20 through 30 (except for CLOCK, which is referenced to the 10% and 90% points). Ordering Information lists temperature ranges and product numbers. Find package drawings in Package Information.

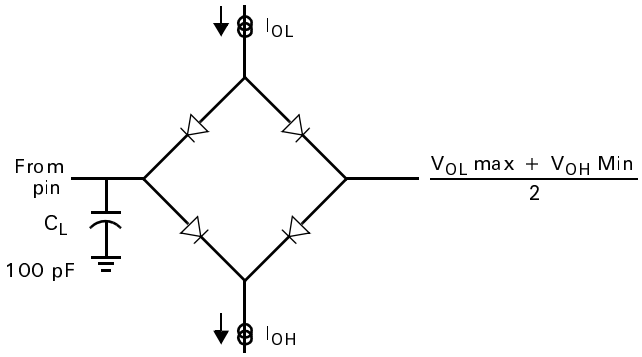



**Figure 19. AC Parameter Test Circuit**

## ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | –0.3 ~ +7.0 | V |
| Input Voltage | $V_{IN}$ | –0.3 ~ $V_{cc}$ +0.3 | V |
| Operating Temperature | $T_{OPR}$ | 0 ~ 70 | °C |
| Extended Temperature | $T_{EXT}$ | –40 ~ 85 | °C |
| Storage Temperature | $T_{STG}$ | –55 ~ +150 | °C |

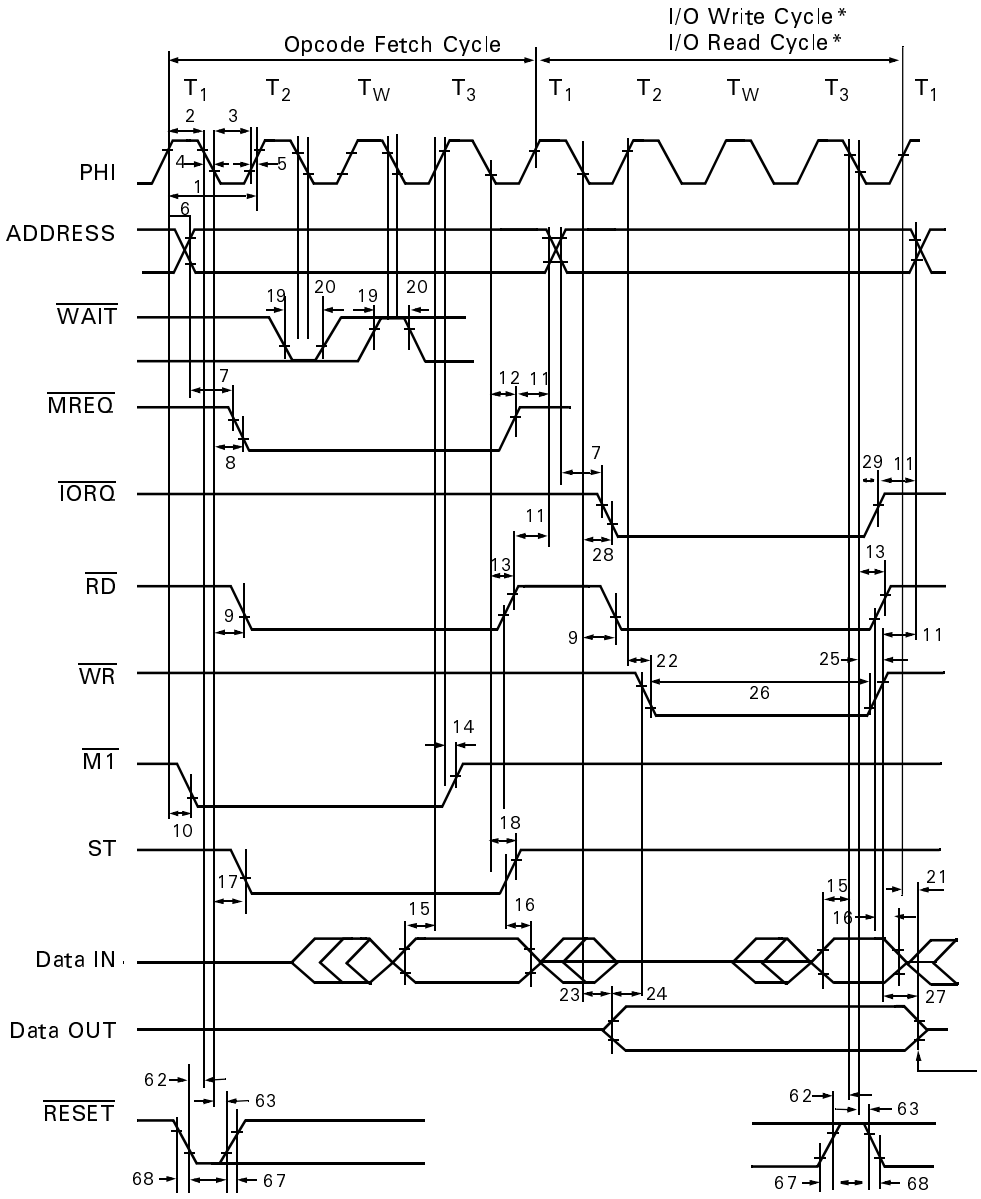
**Note:** Permanent damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability.

## AC CHARACTERISTICS—Z8S180

**Table 8. Z8S180 AC Characteristics**
**$V_{DD}$ = 5V ±10% or $V_{DD}$ = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation**

| | | | Z8S180—20 MHz | | Z8S180—33 MHz | | |
|---|---|---|---|---|---|---|---|
| **Number** | **Symbol** | **Item** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| 1 | $t_{CYC}$ | Clock Cycle Time | 50 | DC | 30 | DC | ns |
| 2 | $t_{CHW}$ | Clock "H" Pulse Width | 15 | — | 10 | — | ns |
| 3 | $t_{CLW}$ | Clock "L" Pulse Width | 15 | — | 10 | — | ns |
| 4 | $t_{CF}$ | Clock Fall Time | — | 10 | — | 5 | ns |
| 5 | $t_{CR}$ | Clock Rise Time | — | 10 | — | 5 | ns |
| 6 | $t_{AD}$ | PHI Rise to Address Valid Delay | — | 30 | — | 15 | ns |
| 7 | $t_{AS}$ | Address Valid to $\overline{MREQ}$ Fall or $\overline{IORQ}$ Fall) | 5 | — | 5 | — | ns |
| 8 | $t_{MED1}$ | PHI Fall to $\overline{MREQ}$ Fall Delay | — | 25 | — | 15 | ns |
| 9 | $t_{RDD1}$ | PHI Fall to $\overline{RD}$ Fall Delay $\overline{IOC}$ = 1 | — | 25 | — | 15 | ns |
| | | PHI Rise to $\overline{RD}$ Rise Delay $\overline{IOC}$ = 0 | — | 25 | — | 15 | |
| 10 | $t_{M1D1}$ | PHI Rise to $\overline{M1}$ Fall Delay | — | 35 | — | 15 | ns |
| 11 | $t_{AH}$ | Address Hold Time from $\overline{MREQ}$, $\overline{IOREQ}$, $\overline{RD}$, $\overline{WR}$ High | 5 | — | 5 | — | ns |
| 12 | $t_{MED2}$ | PHI Fall to $\overline{MREQ}$ Rise Delay | — | 25 | — | 15 | ns |
| 13 | $t_{RDD2}$ | PHI Fall to $\overline{RD}$ Rise Delay | — | 25 | — | 15 | ns |
| 14 | $t_{M1D2}$ | PHI Rise to $\overline{M1}$ Rise Delay | — | 40 | — | 15 | ns |
| 15 | $t_{DRS}$ | Data Read Set-up Time | 10 | — | 5 | — | ns |
| 16 | $t_{DRH}$ | Data Read Hold Time | 0 | — | 0 | — | ns |
| 17 | $t_{STD1}$ | PHI Fall to ST Fall Delay | — | 30 | — | 15 | ns |
| 18 | $t_{STD2}$ | PHI Fall to ST Rise Delay | — | 30 | — | 15 | ns |
| 19 | $t_{WS}$ | $\overline{WAIT}$ Set-up Time to PHI Fall | 15 | — | 10 | — | ns |
| 20 | $t_{WH}$ | $\overline{WAIT}$ Hold Time from PHI Fall | 10 | — | 5 | — | ns |
| 21 | $t_{WDZ}$ | PHI Rise to Data Float Delay | — | 35 | — | 20 | ns |
| 22 | $t_{WRD1}$ | PHI Rise to $\overline{WR}$ Fall Delay | — | 25 | — | 15 | ns |
| 23 | $t_{WDD}$ | PHI Fall to Write Data Delay Time | — | 25 | — | 15 | ns |
| 24 | $t_{WDS}$ | Write Data Set-up Time to $\overline{WR}$ Fall | 10 | — | 10 | — | ns |
| 25 | $t_{WRD2}$ | PHI Fall to $\overline{WR}$ Rise Delay | — | 25 | — | 15 | ns |
| 26 | $t_{WRP}$ | $\overline{WR}$ Pulse Width (Memory Write Cycle) | 80 | — | 45 | — | ns |
| 26a | | $\overline{WR}$ Pulse Width (I/O Write Cycle) | 150 | — | 70 | — | ns |
| 27 | $t_{WDH}$ | Write Data Hold Time from $\overline{WR}$ Rise | 10 | — | 5 | — | ns |
| 28 | $t_{IOD1}$ | PHI Fall to $\overline{IORQ}$ Fall Delay $\overline{IOC}$ = 1 | — | 25 | — | 15 | ns |
| | | PHI Rise to $\overline{IORQ}$ Fall Delay $\overline{IOC}$ = 0 | — | 25 | — | 15 | |
| 29 | $t_{IOD2}$ | PHI Fall to $\overline{IORQ}$ Rise Delay | — | 25 | — | 15 | ns |
| 30 | $t_{IOD3}$ | $\overline{M1}$ Fall to $\overline{IORQ}$ Fall Delay | 125 | — | 80 | — | ns |
| 31 | $t_{INTS}$ | $\overline{INT}$ Set-up Time to PHI Fall | 20 | — | 15 | — | ns |

## TIMING DIAGRAMS




Note: *Memory Read/Write Cycle timing is the same as I/O Read/Write Cycle except there are no automatic wait states ($T_W$), and $\overline{MREQ}$ is active instead of $\overline{IORQ}$.

**Figure 20. CPU Timing**
**(Opcode Fetch Cycle, Memory Read Cycle, Memory Write Cycle, I/O Write Cycle, I/O Read Cycle)**

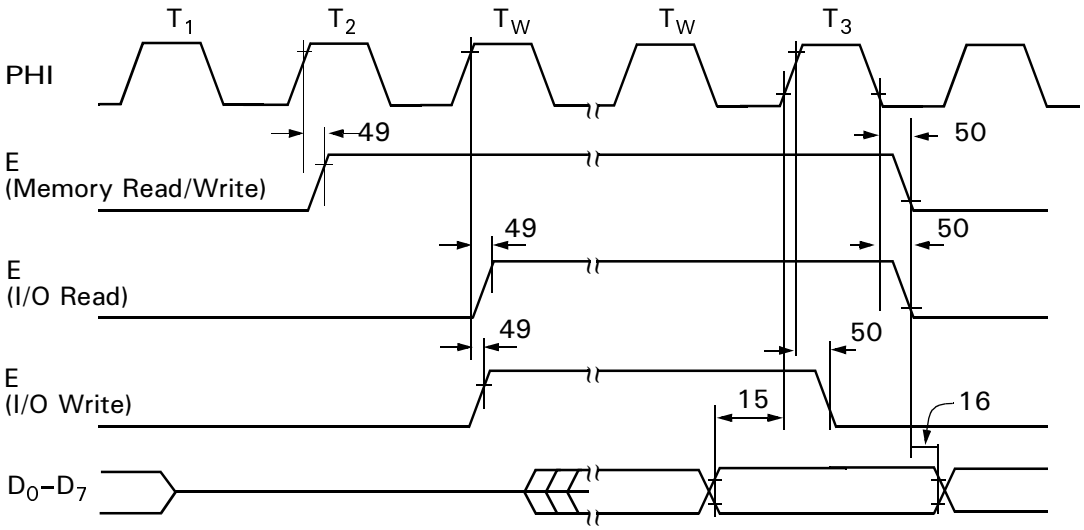



**Figure 24. E Clock Timing**
**(Memory Read/Write Cycle, I/O Read/Write Cycle)**

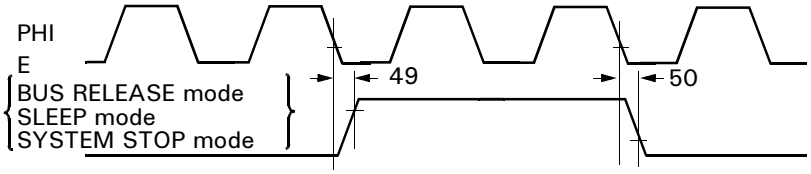



**Figure 25. E Clock Timing**
**(BUS RELEASE Mode, SLEEP Mode, SYSTEM STOP Mode)**

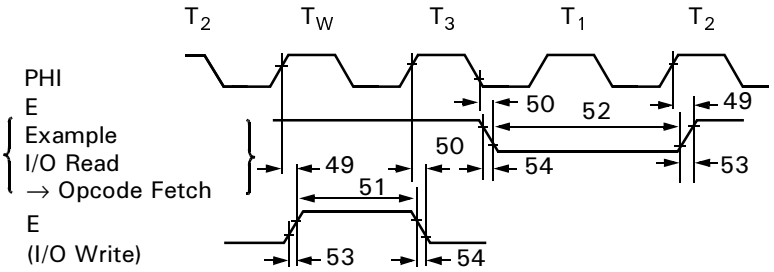



**Figure 26. E Clock Timing**
**(Minimum Timing Example of $P_{WEL}$ and $P_{WEH}$)**

**Bit 2 LNIO.** This bit controls the drive capability of certain external I/O pins of the Z8S180/Z8L180. When this bit is set to 1, the output drive capability of the following pins is reduced to 33 percent of the original drive capability:

| | |
|---|---|
| $\overline{RTS0}$ | TxS |
| CKA1/$\overline{TEND0}$ | CKA0/$\overline{DREQ0}$ |
| TXA0 | TXA1 |
| $\overline{TENDi}$ | CKS |

**Bit 1 LNCPUCTL.** This bit controls the drive capability of the CPU Control pins. When this bit is set to 1, the output drive capability of the following pins is reduced to 33 percent of the original drive capability:

| | |
|---|---|
| $\overline{BUSACK}$ | $\overline{RD}$ |
| $\overline{WR}$ | $\overline{M1}$ |
| $\overline{MREQ}$ | $\overline{IORQ}$ |
| $\overline{RFSH}$ | $\overline{HALT}$ |
| E | TEST |
| ST | |

**Bit 0 LNAD/DATA.** This bit controls the drive capability of the Address/Data bus output drivers. If this bit is set to 1, the output drive capability of the Address and Data bus outputs is reduced to 33 percent of its original drive capability.

## ASCI CHANNEL CONTROL REGISTER B

ASCI Control Register B 0 (CNTLB0: I/O Address = 02H)
ASCI Control Register B 1 (CNTLB1: I/O Address = 03H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | MPBT | MP | $\overline{CTS}$/PS | PEO | DR | SS2 | SS1 | SS0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**Figure 34. ASCI Channel Control Register B**

**MPBT: Multiprocessor Bit Transmit (Bit 7).** When multiprocessor communication format is selected (MP bit = 1), MPBT is used to specify the MPB data bit for transmission. If MPBT = 1, then MPB = 1 is transmitted. If MPBT = 0, then MPB = 0 is transmitted. The MPBT state is undefined during and after RESET.

**MP: Multiprocessor Mode (Bit 6).** When MP is set to 1, the data format is configured for multiprocessor mode based on MOD2 (number of data bits) and MOD0 (number of stop bits) in CNTLA. The format is as follows:

Start bit + 7 or 8 data bits + MPB bit + 1 or 2 stop bits

Multiprocessor (MP = 1) format offers no provision for parity. If MP = 0, the data format is based on MOD0, MOD1, MOD2, and may include parity. The MP bit is cleared to 0 during RESET.

**$\overline{CTS}$/PS: Clear to Send/Prescale (Bit 5).** When read, $\overline{CTS}$/PS reflects the state of the external $\overline{CTS}$ input. If the $\overline{CTS}$ input pin is High, $\overline{CTS}$/PS is read as 1.

**Note:** When the $\overline{CTS}$ input pin is High, the TDRE bit is inhibited (that is, held at 0).

For channel 1, the $\overline{CTS}$ input is multiplexed with RXS pin (Clocked Serial Receive Data). Thus, $\overline{CTS}$/PS is only valid when read if the channel 1 CTS1E bit = 1 and the $\overline{CTS}$ input pin function is selected. The READ data of $\overline{CTS}$/PS is not affected by $\overline{RESET}$.

If the SS2–0 bits in this register are not 111, and the BRG mode bit in the ASEXT register is 0, then writing to this bit sets the prescale (PS) control. Under those circumstances, a 0 indicates a divide-by-10 prescale function while a 1 indicates divide-by-30. The bit resets to 0.

**PEO: Parity Even Odd (Bit 4) .** PEO selects oven or odd parity. PEO does not affect the enabling/disabling of parity (MOD1 bit of CNTLA). If PEO is cleared to 0, even parity is selected. If PEO is set to 1, odd parity is selected. PEO is cleared to 0 during RESET.

**DR: Divide Ratio (Bit 3).** If the X1 bit in the ASEXT register is 0, this bit specifies the divider used to obtain baud rate from the data sampling clock. If DR is reset to 0, divide-by-16 is used, while if DR is set to 1, divide-by-64 is used. DR is cleared to 0 during RESET.

**SS2,1,0: Source/Speed Select 2,1,0 (Bits 2–0).** First, if these bits are 111, as they are after a RESET, the CKA pin is used as a clock input, and is divided by 1, 16, or 64 depending on the DR bit and the X1 bit in the ASEXT register.

If these bits are not 111 and the BRG mode bit is ASEXT is 0, then these bits specify a power-of-two divider for the PHI clock as indicated in Table 10.

Setting or leaving these bits as 111 makes sense for a channel only when its CKA pin is selected for the CKA function. CKAO/CKS offers the CKAO function when bit 4 of the System Configuration Register is 0. $\overline{DCD0}$/CKA1 offers the CKA1 function when bit 0 of the Interrupt Edge register is 1.

**Table 10. Divide Ratio**

| SS2 | SS1 | SS0 | Divide Ratio |
|---|---|---|---|
| 0 | 0 | 0 | ÷1 |
| 0 | 0 | 1 | ÷2 |
| 0 | 1 | 0 | ÷4 |
| 0 | 1 | 1 | ÷8 |
| 1 | 0 | 0 | ÷16 |
| 1 | 0 | 1 | ÷32 |
| 1 | 1 | 0 | ÷64 |
| 1 | 1 | 1 | External Clock |

## TIMER CONTROL REGISTER

The Timer Control Register (TCR) monitors both channels (PRT0, PRT1) TMDR status. It also controls the enabling and disabling of down-counting and interrupts, and controls the output pin A18/$T_{OUT}$ for PRT1.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | TIF1 | TIF0 | TIE1 | TIE0 | TOC1 | TOC0 | TDE1 | TDE0 |
| | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

**Figure 46. Timer Control Register (TCR: I/O Address = 10H)**

**TIF1: Timer Interrupt Flag 1 (Bit 7) .** When TMDR1 decrements to 0, TIF1 is set to 1. This condition generates an interrupt request if enabled by TIE1 = 1. TIF1 is reset to 0 when TCR is read and the higher or lower byte of TMDR1 is read. During RESET, TIF1 is cleared to 0.

**TIF0: Timer Interrupt Flag 0 (Bit 6).** When TMDR0 decrements to 0, TIF0 is set to 1. This condition generates an interrupt request if enabled by TIE0 = 1. TIF0 is reset to 0 when TCR is read and the higher or lower byte of TMDR0 is read. During RESET, TIF0 is cleared to 0.

**TIE1: Timer Interrupt Enable 1 (Bit 5).** When TIE0 is set to 1, TIF1 = 1 generates a CPU interrupt request. When TIE0 is reset to 0, the interrupt request is inhibited. During RESET, TIE0 is cleared to 0.

**TOC1, 0: Timer Output Control (Bits 3, 2).** TOC1 and TOC0 control the output of PRT1 using the multiplexed A18/$T_{OUT}$ pin as indicated in Table 12. During RESET, TOC1 and TOC0 are cleared to 0. If bit 3 of the IAR1B register is 1, the $T_{OUT}$ function is selected. By programming TOC1 and TOC0, the A18/$T_{OUT}$ pin can be forced High, Low, or toggled when TMDR1 decrements to 0.

**Table 12. Timer Output Control**

| TOC1 | TOC0 | Output | |
|---|---|---|---|
| 0 | 0 | Inhibited | The A18/$T_{OUT}$ pin is not affected by the PRT |
| 0 | 1 | Toggled | If bit 3 of IAR1B is 1, the A18/$T_{OUT}$ pin is toggled or set Low or High as indicated |
| 1 | 0 | 0 | |
| 1 | 1 | 1 | |

**TDE1, 0: Timer Down Count Enable (Bits 1, 0).** TDE1 and TDE0 enable and disable down-counting for TMDR1 and TMDR0, respectively. When TDEn (n = 0,1) is set to 1, down-counting is stopped and TMDRn is freely read or written. TDE1 and TDE0 are cleared to 0 during RESET and TMDRn does not decrement until TDEn is set to 1.

## ASCI EXTENSION CONTROL REGISTER CHANNEL 0 AND CHANNEL 1

The ASCI Extension Control Registers (ASEXT0 and ASEXT1) control functions that have been added to the ASCIs in the Z8S180/Z8L180 family. All bits in this register reset to 0.

ASCI Extension Control Register 0 (ASEXT0 I/O Address = 12H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | Reserved | DCD0 Disable | CTS0 Disable | X1 | BRG0 Mode | Break Enable | Break | Send Break |

ASCI Extension Control Register 1 (ASEXT1 I/O Address = 13H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | Reserved | Reserved | Reserved | X1 | BRG1 Mode | Break Enable | Break | Send Break |

**Figure 47. ASCI Extension Control Registers, Channels 0 and 1**

**DCD0 Disable (Bit 6, ASCI0 Only).** If this bit is 0, then the $\overline{\text{DCD0}}$ pin auto-enables the ASCI0 receiver, such that when the pin is negated/High, the Receiver is held in a RESET state. If this bit is 1, the state of the $\overline{\text{DCD}}$-pin has no effect on receiver operation. In either state of this bit, software can read the state of the $\overline{\text{DCD0}}$ pin in the STAT0 register, and the receiver interrupts on a rising edge of $\overline{\text{DCD0}}$.

**CTS0 Disable (Bit 5, ASCI0 Only).** If this bit is 0, then the $\overline{\text{CTS0}}$ pin auto-enables the ASCIO transmitter, in that when the pin is negated/High, the TDRE bit in the STAT0 register is forced to 0. If this bit is 1, the state of the $\overline{\text{CTS0}}$ pin has no effect on the transmitter. Regardless of the state of this bit, software can read the state of the $\overline{\text{CTS0}}$ pin the CNTLB0 register.

**X1 (Bit 4).** If this bit is 1, the clock from the Baud Rate Generator or CKA pin is taken as a 1X-bit clock (sometimes called *isochronous mode*). In this mode, receive data on the RXA pin must be synchronized to the clock on the CKA pin, regardless of whether CKA is an input or an output. If this bit is 0, the clock from the Baud Rate Generator or CKA pin is divided by 16 or 64 per the DR bit in the CNTLB register, to obtain the actual bit rate. In this mode, receive data on the RXA pin is not required to be synchronized to a clock.

**BRG Mode (Bit 3).** If the SS2–0 bits in the CNTLB register are not 111, and this bit is 0, the ASCI Baud Rate Generator divides PHI by 10 or 30, depending on the PS bit in CNTLB, and factored by a power of two (selected by the SS2–0 bits), to obtain the clock that is presented to the transmitter and receiver and output on the CKA pin. If SS2–0 are not 111, and this bit is 1, the Baud Rate Generator divides PHI by twice the sum of the 16-bit value (programmed into the Time Constant registers) and 2. This mode is identical to the operation of the baud rate generator in the ESCC.

**Break Enable (Bit 2).** If this bit is 1, the receiver detects BREAK conditions and report them in bit 1, and the transmitter sends BREAKs under the control of bit 0.

**Break Detect (Bit 1).** The receiver sets this read-only bit to 1 when an all-zero character with a Framing Error becomes the oldest character in the Rx FIFO. The bit is cleared when software writes a 0 to the EFR bit in CNTLA register, also by RESET, by IOSTOP mode, and for ASCI0, if the $\overline{\text{DCD0}}$ pin is auto-enabled and is negated (High).

**Send Break (Bit 0).** If this bit and bit 2 are both 1, the transmitter holds the TXA pin Low to send a BREAK condition. The duration of the BREAK is under software control (one of the PRTs or CTCs can be used to time it). This bit resets to 0, in which state TXA carries the serial output of the transmitter.

## MMU COMMON BASE REGISTER

The Common Base Register (CBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical address for Common Area 1 accesses. All bits of CBR are reset to 0 during RESET.

### MMU Common Base Register

**Mnemonic CBR**
**Address 38H**

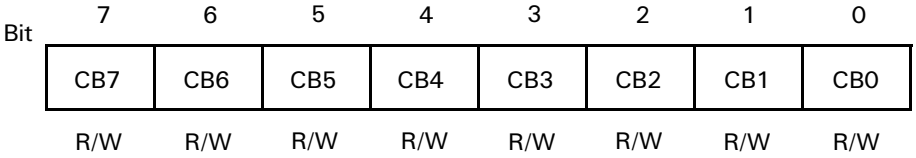



**Figure 78. MMU Common Base Register (CBR: I/O Address = 38H)**

## MMU BANK BASE REGISTER

The Bank Base Register (BBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical address for Bank Area accesses. All bits of BBR are reset to 0 during RESET.

### MMU Bank Base Register

**Mnemonic BBR**
**Address 39H**

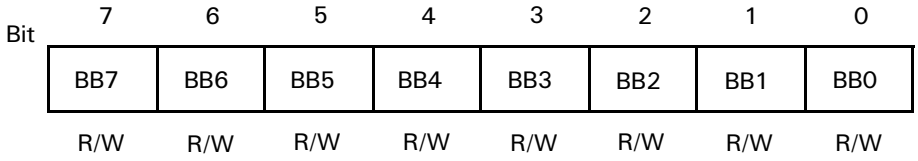



**Figure 79. MMU Bank Base Register (BBR: I/O Address = 39H)**

## MMU COMMON/BANK AREA REGISTER

The Common/Bank Area Register (CBAR) specifies boundaries within the Z8S180/Z8L180 64-KB logical address space for up to three areas; Common Area), Bank Area and Common Area 1.

### MMU Common/Bank Area Register

**Mnemonic CBAR**
**Address 3AH**

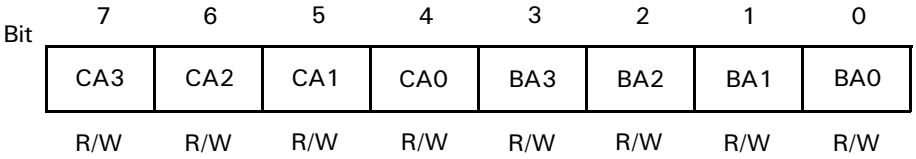



**Figure 80. MMU Common/Bank Area Register (CBAR: I/O Address = 3AH)**

**CA3–CA0:CA (Bits 7–4).** CA specifies the start (Low) address (on 4-KB boundaries) for Common Area 1. This condition also determines the most recent address of the Bank Area. All bits of CA are set to 1 during RESET.

**BA3–BA0 (Bits 3–0).** BA specifies the start (Low) address (on 4-KB boundaries) for the Bank Area. This condition also determines the most recent address of Common Area 0. All bits of BA are set to 1 during RESET.

## OPERATION MODE CONTROL REGISTER

The Z8S180/Z8L180 is descended from two different ancestor processors, ZiLOG's original Z80 and the Hitachi 64180. The Operating Mode Control Register (OMCR) can be programmed to select between certain differences between the Z80 and the 64180.

### Operation Mode Control Register

**Mnemonic OMCR**
**Address 3EH**

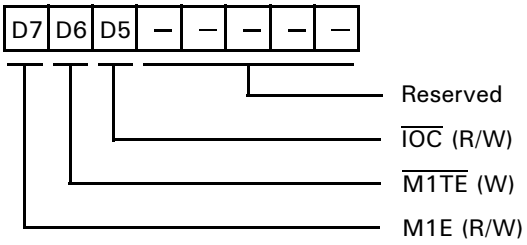



**Figure 81. Operating Control Register (OMCR: I/O Address = 3EH)**

**M1E ($\overline{M1}$ Enable).** This bit controls the $\overline{M1}$ output and is set to a 1 during reset.

When M1E = 1, the $\overline{M1}$ output is asserted Low during the opcode fetch cycle, the $\overline{INT0}$ acknowledge cycle, and the first machine cycle of the $\overline{NMI}$ acknowledge.

On the Z8S180/Z8L180, this choice makes the processor fetch one RETI instruction. When fetching a RETI from zero-wait-state memory, the processor uses three clock machine cycles that are not fully Z80-timing-compatible.

When M1E = 0, the processor does not drive $\overline{M1}$ Low during instruction fetch cycles. After fetching one RETI instruction with normal timing, the processor returns and refetches the instruction using Z80-compatible cycles that drive $\overline{M1}$ Low. This timing compatibility may be required by external Z80 peripherals to properly decode the RETI instruction.

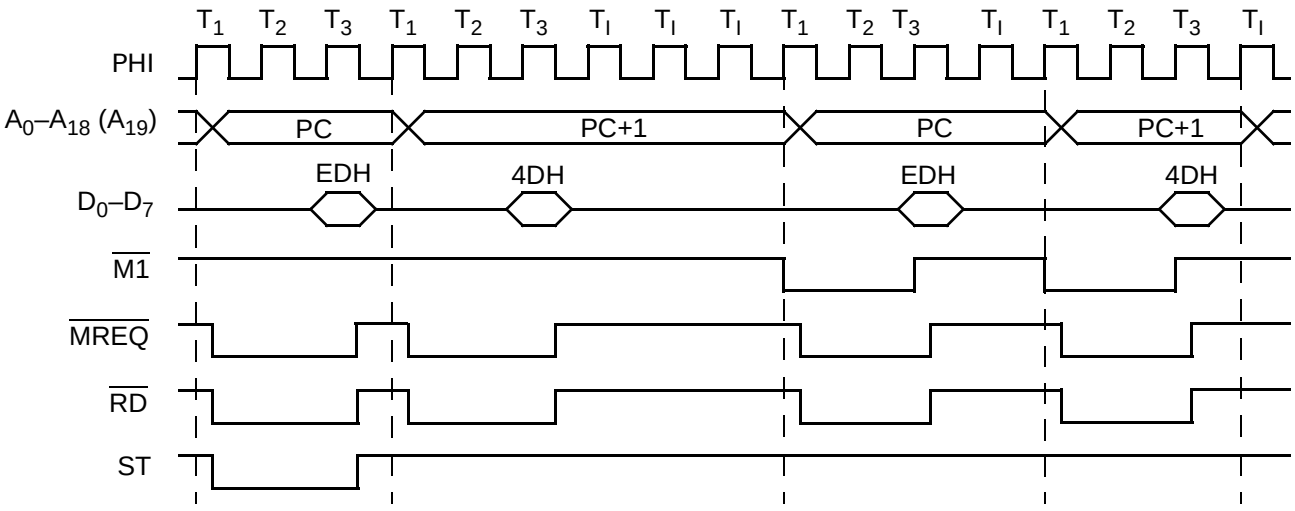



**Figure 82. RETI Instruction Sequence with M1E = 0**

## I/O CONTROL REGISTER

The I/O Control Register (ICR) allows relocation of the internal I/O addresses. ICR also controls the enabling and disabling of IOSTOP mode (Figure 83).

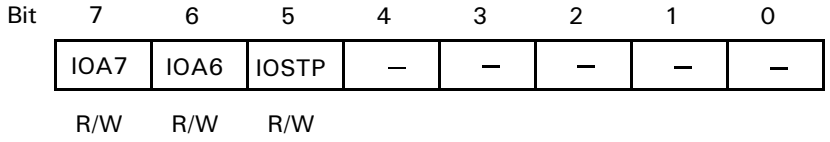



**Figure 83. I/O Control Register (ICR: I/O Address = 3FH)**

**IOA7, 6: I/O Address Relocation (Bits 7,6).** IOA7 and IOA6 relocate internal I/O as indicated in Figure 84.

**Note:** The high-order 8 bits of 16-bit internal I/O address are always 0. IOA7 and IOA6 are cleared to 0 during RESET.

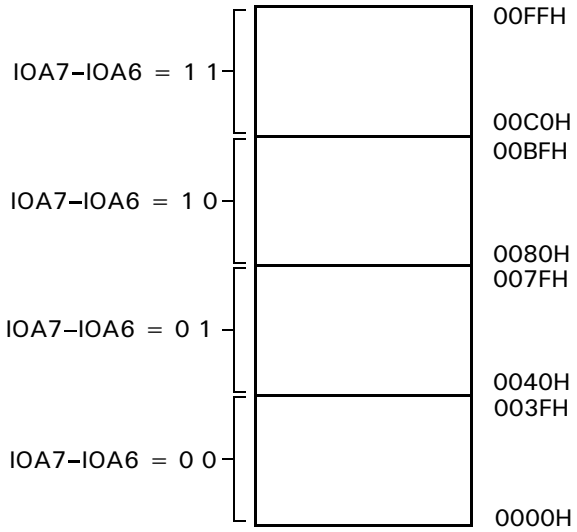



**Figure 84. I/O Address Relocation**

**IOSTP: IOSTOP Mode (Bit 5).** IOSTOP mode is enabled when IOSTP is set to 1. Normal I/O operation resumes when IOSTP is reprogrammed or RESET to 0.

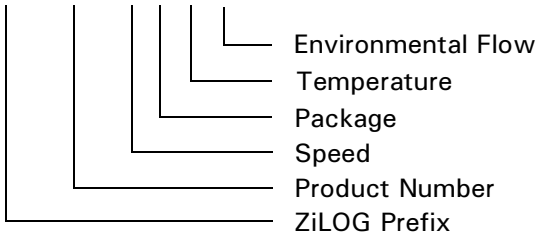
## ORDERING INFORMATION

| Codes | |
|---|---|
| Speed | 10 = 10 MHz |
| | 20 = 20 MHz |
| | 33 = 33 MHz |
| Package | P = 60-Pin Plastic DIP |
| | V = 68-Pin PLCC |
| | F = 80-Pin QFP |
| Temperature | S = 0°C to +70°C |
| | E = –40°C to +85°C |
| Environmental | C = Plastic Standard |

For fast results, contact your local ZiLOG sales office for assistance in ordering the part(s) required.

Example:

Z 8S180 10 P S C is a Z8S180 10-MHz 60-Pin DIP, 0° to +70°C, Plastic Standard Flow




**Pre-Characterization Product**

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or non-conformance with some aspects of the document may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.



ZiLOG, Inc.
910 East Hamilton Avenue, Suite 110
Campbell, CA 95008
Telephone (408) 558-8500
FAX (408) 558-8300
Internet: http://www.zilog.com