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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z8S180 |
| Number of Cores/Bus Width | 1 Core, 8-Bit |
| Speed | 33MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 5.0V |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Security Features | - |
| Package / Case | 68-LCC (J-Lead) |
| Supplier Device Package | 68-PLCC |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8s18033vsg |

## GENERAL DESCRIPTION (Continued)

Power connections follow the conventional descriptions below:

| Connection | Circuit | Device |
|---|---|---|
| Power | $V_{CC}$ | $V_{DD}$ |
| Ground | GND | $V_{SS}$ |

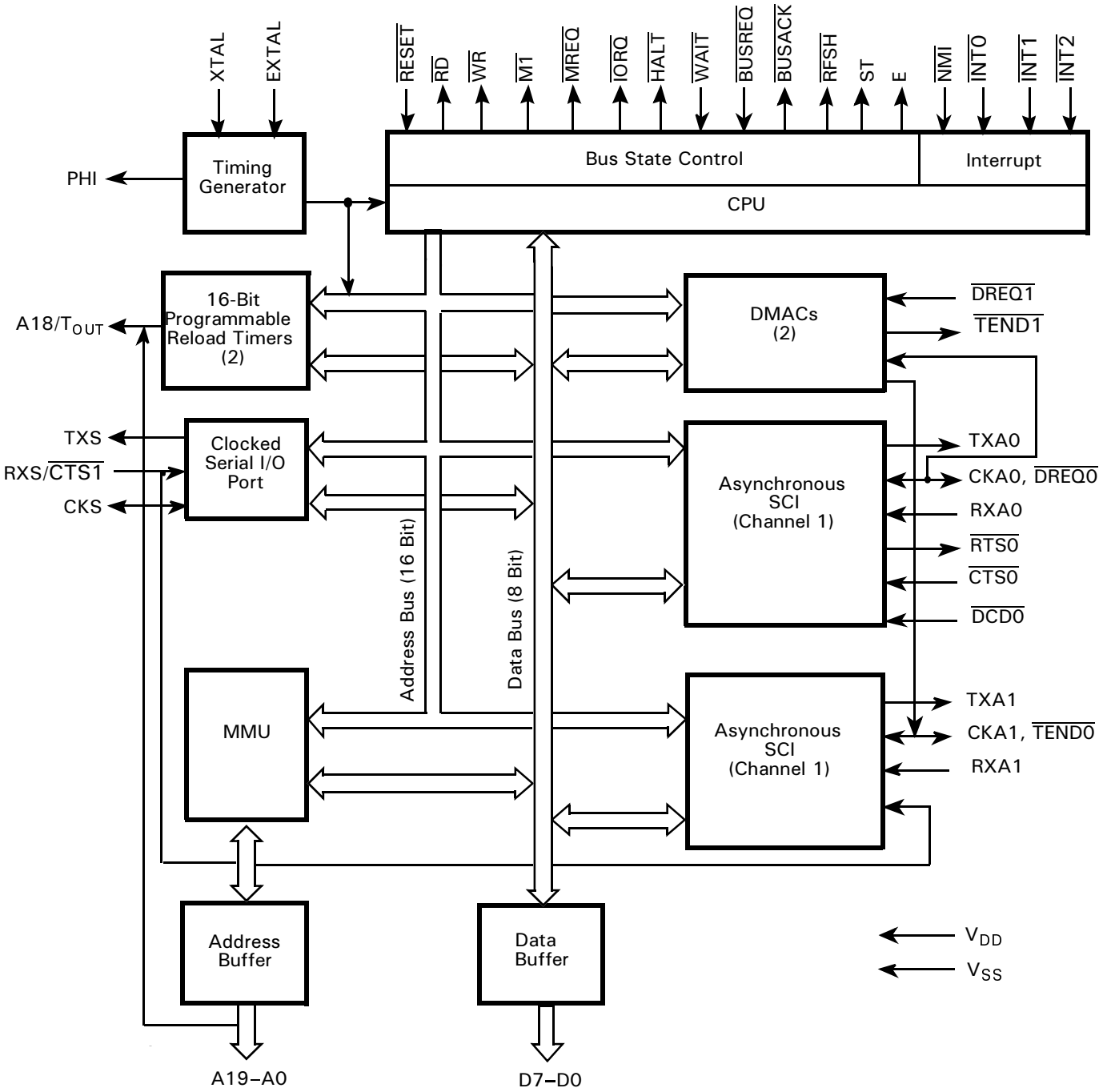



**Figure 1. Z8S180/Z8L180 Functional Block Diagram**

## PIN IDENTIFICATION (Continued)

**Table 2. Pin Status During RESET, BUSACK, and SLEEP Modes (Continued)**

| Pin Number and Package Type | | | | | Pin Status | | |
|---|---|---|---|---|---|---|---|
| QFP | PLCC | DIP | Default Function | Secondary Function | RESET | BUSACK | SLEEP |
| 76 | 4 | 3 | EXTAL | | IN | IN | IN |
| 77 | 5 | 4 | $\overline{\text{WAIT}}$ | | IN | IN | IN |
| 78 | 6 | 5 | $\overline{\text{BUSACK}}$ | | High | OUT | OUT |
| 79 | 7 | 6 | $\overline{\text{BUSREQ}}$ | | IN | IN | IN |
| 80 | 8 | 7 | $\overline{\text{RESET}}$ | | IN | IN | IN |

## OPERATION MODES (Continued)

**Table 5. RETI Control Signal States**

| Machine Cycle | States | Address | Data | $\overline{RD}$ | $\overline{WR}$ | $\overline{MREQ}$ | $\overline{IORQ}$ | $\overline{M1}$ M1E = 1 | $\overline{M1}$ M1E = 0 | $\overline{HALT}$ | ST |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | T1–T3 | 1st Opcode | EDH | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 2 | T1–T3 | 2nd Opcode | 4DH | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| | Ti | NA | 3-state | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Ti | NA | 3-state | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Ti | NA | 3-state | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 3 | T1–T3 | 1st Opcode | EDH | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| | Ti | NA | 3-state | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 4 | T1–T3 | 2nd Opcode | 4DH | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 5 | T1–T3 | SP | Data | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 6 | T1–T3 | SP + 1 | Data | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |

**$\overline{M1TE}$ ($\overline{M1}$ Temporary Enable).** This bit controls the temporary assertion of the $\overline{M1}$ signal. It is always read back as a 1 and is set to 1 during RESET.

When M1E is set to 0 to accommodate certain external Z80 peripheral(s), those same device(s) may require a pulse on $\overline{M1}$ after programming certain of their registers to complete the function being programmed.

For example, when a control word is written to the Z80 PIO to enable interrupts, no enable actually takes place until the PIO sees an active $\overline{M1}$ signal. When $\overline{M1TE}$ = 1, there is no change in the operation of the $\overline{M1}$ signal, and M1E controls its function. When $\overline{M1TE}$ = 0, the $\overline{M1}$ output is asserted during the next opcode fetch cycle regardless of the state programmed into the M1E bit. This condition is only momentary (one time) and it is not necessary to preprogram a 1 to disable the function (see Figure 10).

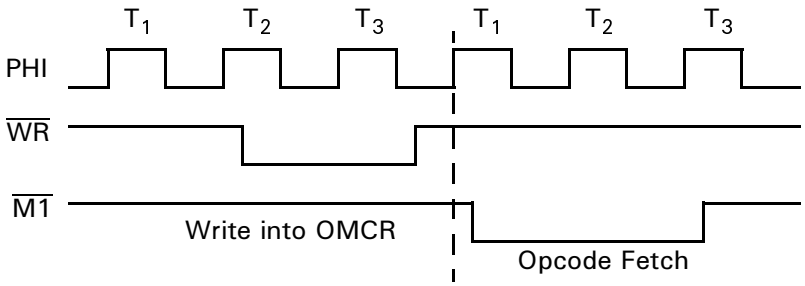



**Figure 10. M1 Temporary Enable Timing**

**IOC (I/O Compatibility).** This bit controls the timing of the $\overline{IORQ}$ and $\overline{RD}$ signals. The bit is set to 1 by RESET.

When $\overline{IOC}$ = 1, the $\overline{IORQ}$ and $\overline{RD}$ signals function the same as the Z64180 (Figure 11).

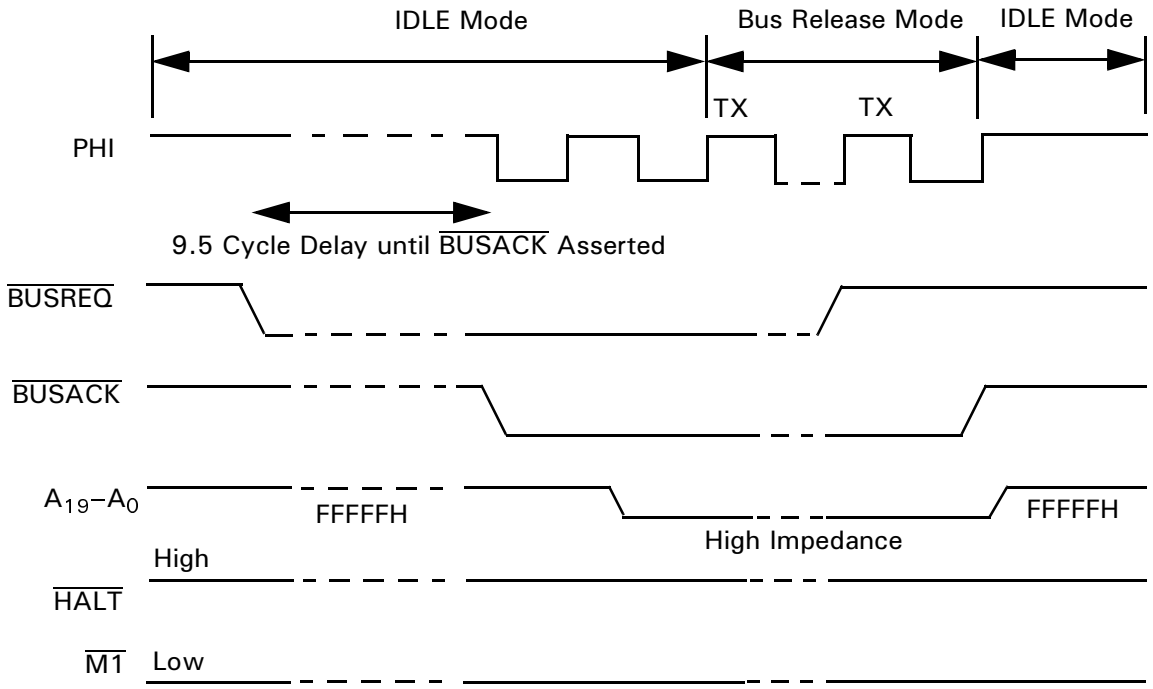



**Figure 16. Bus Granting to External Master in IDLE Mode**

**STANDBY Mode (With or Without QUICK RECOVERY).**

Software can put the Z8S180/Z8L180 into this mode by setting the IOSTOP bit (ICR5) to 1, CCR6 to 1, and executing the SLP instruction. This mode stops the on-chip oscillator and thus draws the least power of any mode, less than 10µA.

As with IDLE mode, the Z8S180/Z8L180 leaves STANDBY mode in response to a Low on $\overline{\text{RESET}}$, on $\overline{\text{NMI}}$, or a Low on $\overline{\text{INT0–2}}$ that is enabled by a 1 in the corresponding bit in the INT/TRAP Control Register. This action grants the bus to an external Master if the BREXT bit in the CPU Control Register (CCR5) is 1. The time required for all of these operations is greatly increased by the necessity for restarting the on-chip oscillator, and ensuring that it stabilizes to square-wave operation.

When an external clock is connected to the EXTAL pin rather than a crystal to the XTAL and EXTAL pins and the external clock runs continuously, there is little necessity to use STANDBY mode because no time is required to restart the oscillator, and other modes restart faster. However, if external logic stops the clock during STANDBY mode (for example, by decoding $\overline{\text{HALT}}$ Low and $\overline{\text{M1}}$ High for several clock cycles), then STANDBY mode can be useful to allow the external clock source to stabilize after it is re-enabled.

When external logic drives $\overline{\text{RESET}}$ Low to bring the device out of STANDBY mode, and a crystal is in use or an external clock source is stopped, the external logic must hold $\overline{\text{RESET}}$ Low until the on-chip oscillator or external clock source is restarted and stabilized.

The clock-stability requirements of the Z8S180/Z8L180 are much less in the divide-by-two mode that is selected by a RESET sequence and controlled by the Clock Divide bit in the CPU Control Register (CCR7). As a result, software performs the following actions:

1. Sets CCR7 to 0 for divide-by-two mode before an SLP instruction and STANDBY mode.
2. Delays setting CCR7 back to 1 for divide-by-one mode as long as possible to allow additional clock stabilization time after a RESET, interrupt, or in-line RESTART after an SLP 01 instruction.

If CCR6 is set to 1 before the SLP instruction places the MPU in STANDBY mode, the value of the CCR3 bit determines the length of the delay before the oscillator restarts and stabilizes when it leaves STANDBY mode due to an external interrupt request. When CCR3 is 0, the Z8S180/Z8L180 waits $2^{17}$ (131,072) clock cycles. When CCR3 is 1, it waits 64 clock cycles. This state is called QUICK RECOVERY mode. The same delay applies to grant-

**Table 7. Z8L180 DC Characteristics**
**$V_{DD}$ = 3.3V ±10%; $V_{SS}$ = 0V**

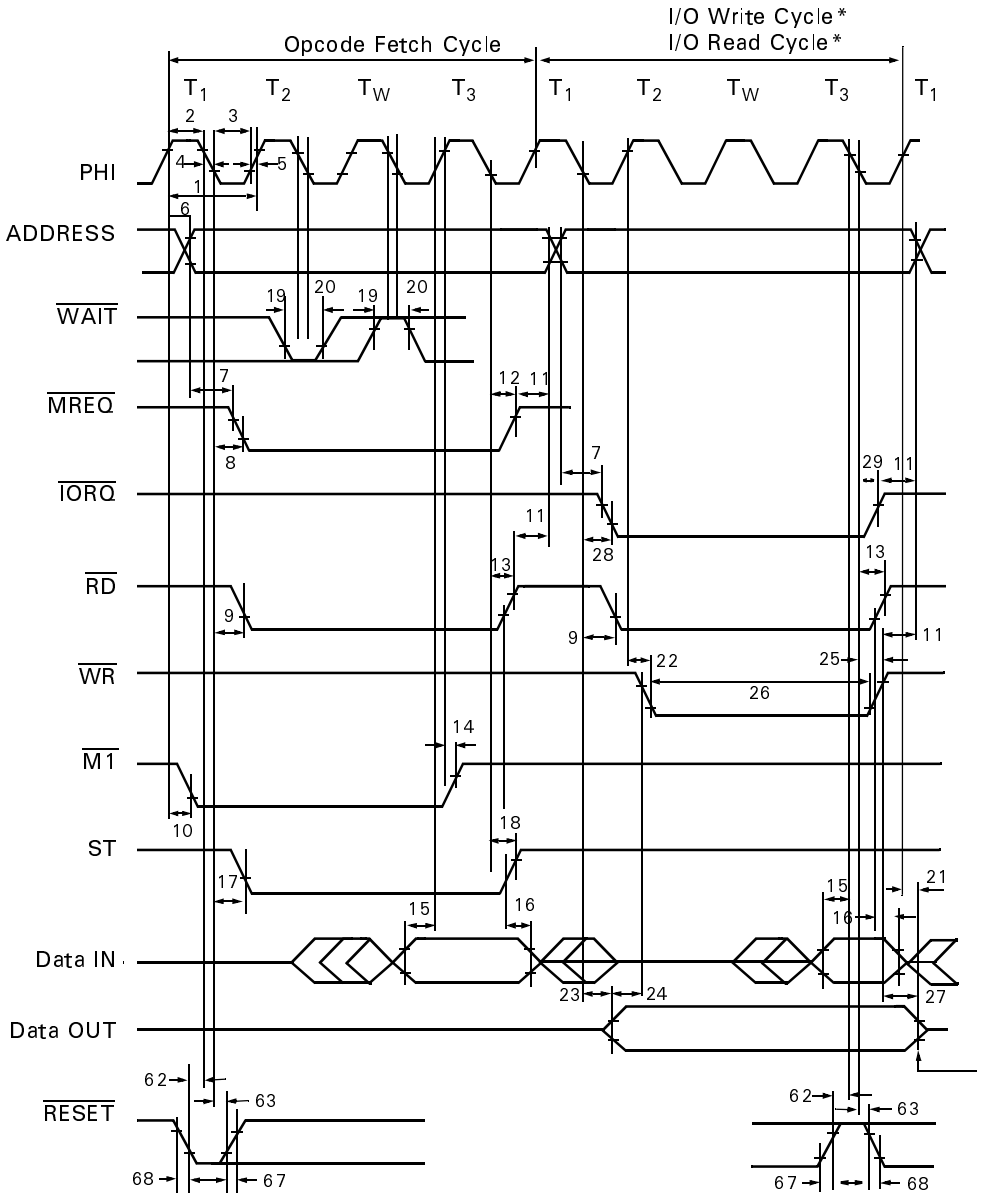
| Symbol | Item | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH1}$ | Input H Voltage<br>$\overline{RESET}$, EXTAL, $\overline{NMI}$ | | $V_{DD}$ –0.6 | | $V_{DD}$ +0.3 | V |
| $V_{IH2}$ | Input H Voltage<br>Except $\overline{RESET}$, EXTAL, $\overline{NMI}$ | | 2.0 | | $V_{DD}$ +0.3 | V |
| $V_{IL1}$ | Input L Voltage<br>RESET, EXTAL, NMI | | –0.3 | | 0.6 | V |
| $V_{IL2}$ | Input L Voltage<br>Except RESET, EXTAL, NMI | | –0.3 | | 0.8 | V |
| $V_{OH}$ | Outputs H Voltage<br>All outputs | $I_{OH}$ = –200 µA | 2.15 | | | V |
| | | $I_{OH}$ = –20 µA | $V_{DD}$ –0.6 | | | V |
| $V_{OL}$ | Outputs L Voltage<br>All Outputs | $I_{OL}$ = 4 mA | | | 0.4 | V |
| $I_{IL}$ | Input Leakage<br>Current All Inputs<br>Except XTAL, EXTAL | $V_{IN}$ = 0.5 ~ $V_{DD}$ –0.5 | | | 1.0 | µA |
| $I_{TL}$ | Three State Leakage<br>Current | $V_{IN}$ = 0.5 ~ $V_{DD}$ –0.5 | | | 1.0 | µA |
| $I_{DD1}$ | Power Dissipation<br>(Normal Operation) | F = 20 MHz | | 30 | 60 | mA |
| | | 4 MHz | | 4 | 10 | |
| | Power Dissipation<br>(SYSTEM STOP mode) | F = 20 MHz | | 5 | 10 | |
| | | 4 MHz | | 2 | 5 | |
| $C_P$ | Pin Capacitance | $V_{IN}$ = 0V, f = 1 MHz<br>$T_A$ = 25° C | | | 12 | pF |

**Note:**
1. $V_{IHmin}$ = $V_{DD}$ –1.0V, $V_{ILmax}$ = 0.6V (All output terminals are at NO LOAD.) $V_{DD}$ = 3.0V.

**Table 8. Z8S180 AC Characteristics (Continued)**
**$V_{DD}$ = 5V ±10% or $V_{DD}$ = 3.3V ±10%; 33-MHz Characteristics Apply Only to 5V Operation**

| | | | Z8S180—20 MHz | | Z8S180—33 MHz | | |
|---|---|---|---|---|---|---|---|
| **Number** | **Symbol** | **Item** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| 63 | $t_{REH}$ | $\overline{RESET}$ Hold Time from PHI Fall | 25 | — | 15 | — | ns |
| 64 | $t_{OSC}$ | Oscillator Stabilization Time | — | 20 | — | 20 | ns |
| 65 | $t_{EXR}$ | External Clock Rise Time (EXTAL) | — | 5 | — | 5 | ns |
| 66 | $t_{EXF}$ | External Clock Fall Time (EXTAL) | — | 5 | — | 5 | ns |
| 67 | $t_{RR}$ | $\overline{RESET}$ Rise Time | — | 50 | — | 50 | ms |
| 68 | $t_{RF}$ | $\overline{RESET}$ Fall Time | — | 50 | — | 50 | ms |
| 69 | $t_{IR}$ | Input Rise Time (except EXTAL, $\overline{RESET}$) | — | 50 | — | 50 | ns |
| 70 | $t_{IF}$ | Input Fall Time (except EXTAL, $\overline{RESET}$) | — | 50 | — | 50 | ns |

## TIMING DIAGRAMS




Note: *Memory Read/Write Cycle timing is the same as I/O Read/Write Cycle except there are no automatic wait states ($T_W$), and $\overline{MREQ}$ is active instead of $\overline{IORQ}$.

**Figure 20. CPU Timing**
**(Opcode Fetch Cycle, Memory Read Cycle, Memory Write Cycle, I/O Write Cycle, I/O Read Cycle)**

## ASCI REGISTER DESCRIPTION

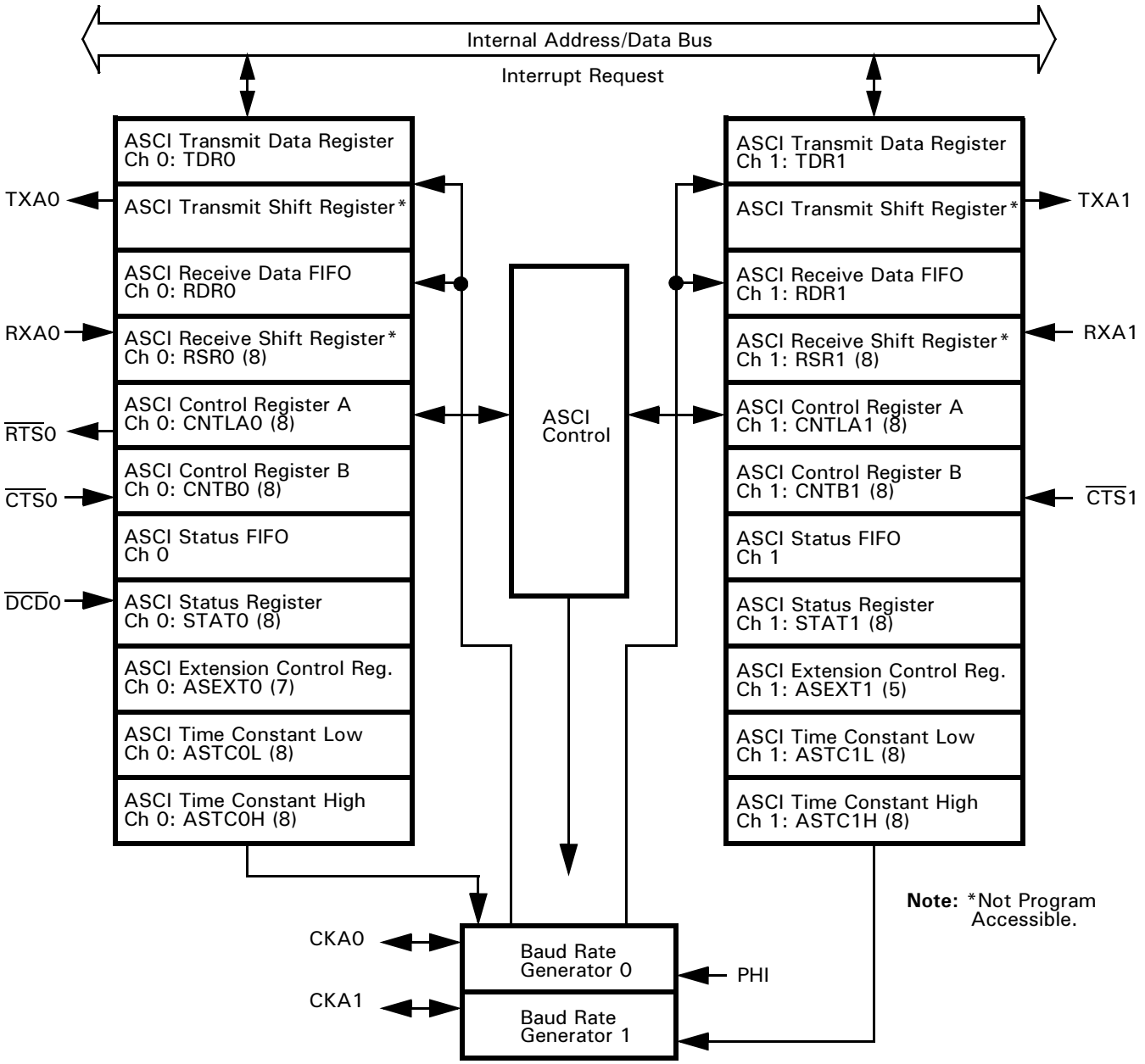



**Figure 32. ASCI Block Diagram**

**ASCI Transmit Shift Register 0,1.** When the ASCI Transmit Shift Register (TSR) receives data from the ASCI Transmit Data Register (TDR), the data is shifted out to the TXA pin. When transmission is completed, the next byte (if available) is automatically loaded from TDR into TSR and the next transmission starts. If no data is available for transmission, TSR idles by outputting a continuous High level. This register is not program-accessible

**ASCI Transmit Data Register 0,1 (TDR0, 1: I/O address = 06H, 07H).** Data written to the ASCI Transmit Data Register is transferred to the TSR as soon as TSR is empty. Data can be written while TSR is shifting out the previous byte of data. Thus, the ASCI transmitter is double buffered.

## ASCI STATUS REGISTER 0,1

Each ASCI channel status register (STAT0,1) allows interrogation of ASCI communication, error and modem control signal status, and the enabling or disabling of ASCI interrupts.

ASCI Status Register 0 (STAT0: I/O Address = 04H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | RDRF | OVRN | PE | FE | RE | $\overline{DCD0}$ | TDRE | TIE |
| | R | R | R | R | R/W | R | R | R/W |

ASCI Status Register 1 (STAT1: I/O Address = 05H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | RDRF | OVRN | PE | FE | RE | CTS1E | TDRE | TIE |
| | R | R | R | R | R/W | R/W | R | R/W |

**Figure 35. ASCI Status Registers**

**RDRF: Receive Data Register Full (Bit 7).** RDRF is set to 1 when an incoming data byte is loaded into an empty Rx FIFO. If a framing or parity error occurs, RDRF is still set and the receive data (which generated the error) is still loaded into the FIFO. RDRF is cleared to 0 by reading RDR and most recently received character in the FIFO from IOSTOP mode, during RESET and for ASCI0 if the $\overline{DCD0}$ input is auto-enabled and is negated (High).

**OVRN: Overrun Error (Bit 6).** An overrun condition occurs if the receiver finishes assembling a character but the Rx FIFO is full so there is no room for the character. However, this status bit is not set until the most recent character received before the overrun becomes the oldest byte in the FIFO. This bit is cleared when software writes a 1 to the EFR bit in the CNTLA register. The bit may also be cleared by RESET in IOSTOP mode or ASCI0 if the $\overline{DCD0}$ pin is auto enabled and is negated (High).

**Note:** When an overrun occurs, the receiver does not place the character in the shift register into the FIFO, nor any subsequent characters, until the most recent good character enters the top of the FIFO so that OVRN is set. Software then writes a 1 to EFR to clear it.

**PE: Parity Error (Bit 5).** A parity error is detected when parity checking is enabled.When the MOD1 bit in the CNTLA register is 1, a character is assembled in which the parity does not match the PEO bit in the CNTLB register. However, this status bit is not set until or unless the error character becomes the oldest one in the Rx FIFO. PE is cleared when software writes a 1 to the EFR bit in the CNTRLA register. PE is also cleared by RESET in IOSTOP mode, or on ASCI0, if the $\overline{DCD0}$ pin is auto-enabled and is negated (High).

**FE: Framing Error (Bit 4).** A framing error is detected when the stop bit of a character is sampled as 0/SPACE. However, this status bit is not set until/unless the error character becomes the oldest one in the Rx FIFO. FE is cleared when software writes a 1 to the EFR bit in the CNTLA register. FE is also cleared by RESET in IOSTOP mode, or on ASCI0, if the $\overline{DCD0}$ pin is auto-enabled and is negated (High).

**REI: Receive Interrupt Enable (Bit 3).** RIE should be set to 1 to enable ASCI receive interrupt requests. When RIE is 1, the Receiver requests an interrupt when a character is received and RDRF is set, but only if neither DMA channel requires its request-routing field to be set to receive data from this ASCI. That is, if SM1–0 are 11 and SAR17–16 are 10, or DIM1 is 1 and IAR17–16 are 10, then ASCI1 does not request an interrupt for RDRF. If RIE is 1, either ASCI requests an interrupt when OVRN, PE or FE is set, and

ASCI0 requests an interrupt when $\overline{DCD0}$ goes High. RIE is cleared to 0 by RESET.

**$\overline{DCD0}$: Data Carrier Detect (Bit 2 STAT0).** This bit is set to 1 when the pin is High. It is cleared to 0 on the first READ of STAT0 following the pin's transition from High to Low and during RESET. When bit 6 of the ASEXT0 register is 0 to select auto-enabling, and the pin is negated (High), the receiver is reset and its operation is inhibited.

**$\overline{CTS1E}$: Clear To Send (Bit 2 STAT1).** Channel 1 features an external $\overline{CTS1}$ input, which is multiplexed with the receive data pin RSX for the CSI/O. Setting this bit to 1 selects the CTS1 function; clearing the bit to 0 selects the RXS function.

**TDRE: Transmit Data Register Empty (Bit 1).** TDRE = 1 indicates that the TDR is empty and the next transmit data byte is written to TDR. After the byte is written to TDR, TDRE is cleared to 0 until the ASCI transfers the byte from TDR to the TSR and then TDRE is again set to 1. TDRE is set to 1 in IOSTOP mode and during RESET. On ASCI0, if the $\overline{CTS0}$ pin is auto-enabled in the ASEXT0 register and the pin is High, TDRE is reset to 0.

**TIE: Transmit Interrupt Enable (Bit 0).** TIE should be set to 1 to enable ASCI transmit interrupt requests. If TIE = 1, an interrupt is requested when TDRE = 1. TIE is cleared to 0 during RESET.

## ASCI TRANSMIT DATA REGISTERS

Register addresses 06H and 07H hold the ASCI transmit data for channel 0 and channel 1, respectively.

### ASCI Transmit Data Registers Channel 0

**Mnemonic TDR0**
**Address 06H**

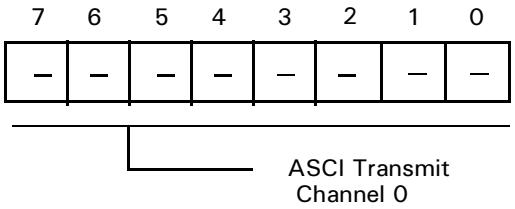



**Figure 36. ASCI Register**

### ASCI Transmit Data Registers Channel 1

**Mnemonic TDR1**
**Address 07H**

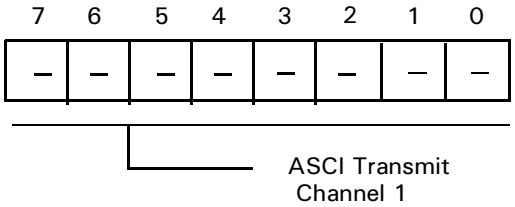



**Figure 37. ASCI Register**

## TIMER CONTROL REGISTER

The Timer Control Register (TCR) monitors both channels (PRT0, PRT1) TMDR status. It also controls the enabling and disabling of down-counting and interrupts, and controls the output pin A18/$T_{OUT}$ for PRT1.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | TIF1 | TIF0 | TIE1 | TIE0 | TOC1 | TOC0 | TDE1 | TDE0 |
| | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

**Figure 46. Timer Control Register (TCR: I/O Address = 10H)**

**TIF1: Timer Interrupt Flag 1 (Bit 7) .** When TMDR1 decrements to 0, TIF1 is set to 1. This condition generates an interrupt request if enabled by TIE1 = 1. TIF1 is reset to 0 when TCR is read and the higher or lower byte of TMDR1 is read. During RESET, TIF1 is cleared to 0.

**TIF0: Timer Interrupt Flag 0 (Bit 6).** When TMDR0 decrements to 0, TIF0 is set to 1. This condition generates an interrupt request if enabled by TIE0 = 1. TIF0 is reset to 0 when TCR is read and the higher or lower byte of TMDR0 is read. During RESET, TIF0 is cleared to 0.

**TIE1: Timer Interrupt Enable 1 (Bit 5).** When TIE0 is set to 1, TIF1 = 1 generates a CPU interrupt request. When TIE0 is reset to 0, the interrupt request is inhibited. During RESET, TIE0 is cleared to 0.

**TOC1, 0: Timer Output Control (Bits 3, 2).** TOC1 and TOC0 control the output of PRT1 using the multiplexed A18/$T_{OUT}$ pin as indicated in Table 12. During RESET, TOC1 and TOC0 are cleared to 0. If bit 3 of the IAR1B register is 1, the $T_{OUT}$ function is selected. By programming TOC1 and TOC0, the A18/$T_{OUT}$ pin can be forced High, Low, or toggled when TMDR1 decrements to 0.

**Table 12. Timer Output Control**

| TOC1 | TOC0 | Output | |
|---|---|---|---|
| 0 | 0 | Inhibited | The A18/$T_{OUT}$ pin is not affected by the PRT |
| 0 | 1 | Toggled | If bit 3 of IAR1B is 1, the A18/$T_{OUT}$ pin is toggled or set Low or High as indicated |
| 1 | 0 | 0 | |
| 1 | 1 | 1 | |

**TDE1, 0: Timer Down Count Enable (Bits 1, 0).** TDE1 and TDE0 enable and disable down-counting for TMDR1 and TMDR0, respectively. When TDEn (n = 0,1) is set to 1, down-counting is stopped and TMDRn is freely read or written. TDE1 and TDE0 are cleared to 0 during RESET and TMDRn does not decrement until TDEn is set to 1.

## ASCI EXTENSION CONTROL REGISTER CHANNEL 0 AND CHANNEL 1

The ASCI Extension Control Registers (ASEXT0 and ASEXT1) control functions that have been added to the ASCIs in the Z8S180/Z8L180 family. All bits in this register reset to 0.

ASCI Extension Control Register 0 (ASEXT0 I/O Address = 12H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | Reserved | DCD0 Disable | CTS0 Disable | X1 | BRG0 Mode | Break Enable | Break | Send Break |

ASCI Extension Control Register 1 (ASEXT1 I/O Address = 13H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | Reserved | Reserved | Reserved | X1 | BRG1 Mode | Break Enable | Break | Send Break |

**Figure 47. ASCI Extension Control Registers, Channels 0 and 1**

**DCD0 Disable (Bit 6, ASCI0 Only).** If this bit is 0, then the $\overline{\text{DCD0}}$ pin auto-enables the ASCI0 receiver, such that when the pin is negated/High, the Receiver is held in a RESET state. If this bit is 1, the state of the $\overline{\text{DCD}}$-pin has no effect on receiver operation. In either state of this bit, software can read the state of the $\overline{\text{DCD0}}$ pin in the STAT0 register, and the receiver interrupts on a rising edge of $\overline{\text{DCD0}}$.

**CTS0 Disable (Bit 5, ASCI0 Only).** If this bit is 0, then the $\overline{\text{CTS0}}$ pin auto-enables the ASCIO transmitter, in that when the pin is negated/High, the TDRE bit in the STAT0 register is forced to 0. If this bit is 1, the state of the $\overline{\text{CTS0}}$ pin has no effect on the transmitter. Regardless of the state of this bit, software can read the state of the $\overline{\text{CTS0}}$ pin the CNTLB0 register.

**X1 (Bit 4).** If this bit is 1, the clock from the Baud Rate Generator or CKA pin is taken as a 1X-bit clock (sometimes called *isochronous mode*). In this mode, receive data on the RXA pin must be synchronized to the clock on the CKA pin, regardless of whether CKA is an input or an output. If this bit is 0, the clock from the Baud Rate Generator or CKA pin is divided by 16 or 64 per the DR bit in the CNTLB register, to obtain the actual bit rate. In this mode, receive data on the RXA pin is not required to be synchronized to a clock.

**BRG Mode (Bit 3).** If the SS2–0 bits in the CNTLB register are not 111, and this bit is 0, the ASCI Baud Rate Generator divides PHI by 10 or 30, depending on the PS bit in CNTLB, and factored by a power of two (selected by the SS2–0 bits), to obtain the clock that is presented to the transmitter and receiver and output on the CKA pin. If SS2–0 are not 111, and this bit is 1, the Baud Rate Generator divides PHI by twice the sum of the 16-bit value (programmed into the Time Constant registers) and 2. This mode is identical to the operation of the baud rate generator in the ESCC.

**Break Enable (Bit 2).** If this bit is 1, the receiver detects BREAK conditions and report them in bit 1, and the transmitter sends BREAKs under the control of bit 0.

**Break Detect (Bit 1).** The receiver sets this read-only bit to 1 when an all-zero character with a Framing Error becomes the oldest character in the Rx FIFO. The bit is cleared when software writes a 0 to the EFR bit in CNTLA register, also by RESET, by IOSTOP mode, and for ASCI0, if the $\overline{\text{DCD0}}$ pin is auto-enabled and is negated (High).

**Send Break (Bit 0).** If this bit and bit 2 are both 1, the transmitter holds the TXA pin Low to send a BREAK condition. The duration of the BREAK is under software control (one of the PRTs or CTCs can be used to time it). This bit resets to 0, in which state TXA carries the serial output of the transmitter.

## ASCI TIME CONSTANT REGISTERS

If the SS2–0 bits of the CNTLB register are not 111, and the BRG mode bit in the ASEXT register is 1, the ASCI divides the PHI clock by two times the registers' 16-bit value, plus two. As a result, the clock is presented to the transmitter and receiver for division by 1, 16, or 64, and is output on the CKA pin.

If the SS2–0 bits in an ASCI CNTLB register are not 111, and the BRG mode bit in its Extension Control Register is 1, its *new* baud rate generator divides PHI for serial clocking, as follows:

$$\text{bits/second} = f_{PHI}/(2*(TC+2) \times \text{sampling rate})$$

where TC is the 16-bit value programmed into the ASCI Time Constant High and Low registers. If the ASCI multiplexed CKA pin is selected for the CKA function, it outputs the clock before the final division by the sampling rate, as follows:

$$f_{CKAout} = f_{PHI}/(2*(TC+2))$$

Find the TC value for a particular serial bit rate as follows:

$$TC = (f_{PHI}/(2 \times \text{bits/second} \times \text{sampling rate})) - 2$$

ASCI Time Constant Register 0 Low (ASTC0L, I/O Address 1AH)
ASCI Time Constant Register 1 Low (ASTC1L, I/O Address 1CH)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | LS 8 Bits of Time Constant | | | | | | | |

ASCI Time Constant Register 0 High (ASTC0H, I/O Address 1BH)
ASCI Time Constant Register 1 High (ASTC1H, I/O Address 1DH)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | MS 8 Bits of Time Constant | | | | | | | |

**Figure 53. ASCI Time Constant Registers**

## CLOCK MULTIPLIER REGISTER

**(Z180 MPU Address 1EH)**

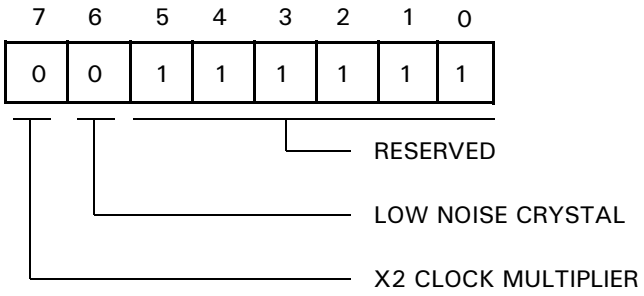



**Figure 54. Clock Multiplier Register**

**Bit 7. X2 Clock Multiplier Mode.** When this bit is set to 1, the programmer can double the internal clock speed from the speed of the external clock. This feature only operates effectively with frequencies of 10–16 MHz (20–32 MHz internal). When this bit is set to 0, the Z8S180/Z8L180 device operates in normal mode. At power-up, this feature is disabled.

**Bit 6. Low Noise Crystal Option.** Setting this bit to 1 enables the low-noise option for the EXTAL and XTAL pins. This option reduces the gain in addition to reducing the output drive capability to 30% of its original drive capability. The Low Noise Crystal Option is recommended in the use of crystals for PCMCIA applications, where the crystal may be driven too hard by the oscillator. Setting this bit to 0 is selected for normal operation of the EXTAL and XTAL pins. The default for this bit is 0.

**Note:** Operating restrictions for device operation are listed below. If a low-noise option is required, and normal device operation is required, use the clock multiplier feature.

**Table 13. Low Noise Option**

| Low Noise ADDR 1E, bit 6 = 1 | Normal ADDR 1E, bit 6 = 0 |
|---|---|
| 20 MHz @ 4.5V, 100°C | 33 MHz @ 4.5V, 100°C |
| 10 MHz @ 3.0V, 100°C | 20 MHz @ 3.0V, 100°C |

## DMA SOURCE ADDRESS REGISTER CHANNEL 0

The DMA Source Address Register Channel 0 specifies the physical source address for channel 0 transfers. The register contains 20 bits and can specify up to 1024 KB memory addresses or up to 64-KB I/O addresses. Channel 0 source can be memory, I/O, or memory mapped I/O. For I/O, bits 17–16 of this register identify the Request Handshake signal.

### DMA Source Address Register, Channel 0 Low

**Mnemonic SAR0L**
**Address 20H**

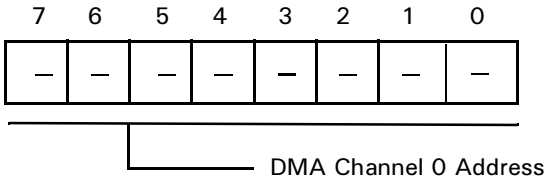



**Figure 55. DMA Source Address Register 0 Low**

### DMA Source Address Register, Channel 0 High

**Mnemonic SAR0H**
**Address 21H**

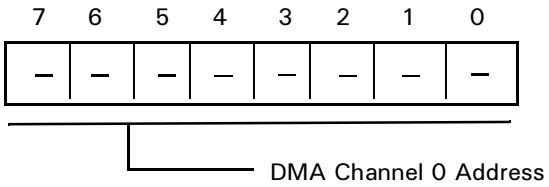



**Figure 56. DMA Source Address Register 0 High**

### DMA Source Address Register Channel 0B

**Mnemonic SAR0B**
**Address 22H**

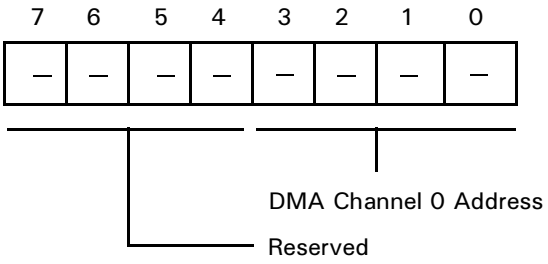



**Figure 57. DMA Source Address Register 0B**

If the source is in I/O space, bits 1–0 of this register select the DMA request signal for DMA0, as follows:

| Bit 1 (A17) | Bit 0 (A16) | DMA Transfer Request |
|---|---|---|
| 0 | 0 | DREQ0 (external) |
| 0 | 1 | RDRF (ASCI0) |
| 1 | 0 | RDRF (ASCI1) |
| 1 | 1 | Reserved |

## INTERRUPT VECTOR LOW REGISTER

Bits 7–5 of the Interrupt Vector Low Register ($I_L$) are used as bits 7–5 of the synthesized interrupt vector during interrupts for the $\overline{INT1}$ and $\overline{INT2}$ pins and for the DMAs, ASCIs, PRTs, and CSI/O. These three bits are cleared to 0 during RESET (Figure 74).

### Interrupt Vector Low Register

**Mnemonic: IL**
**Address 33H**

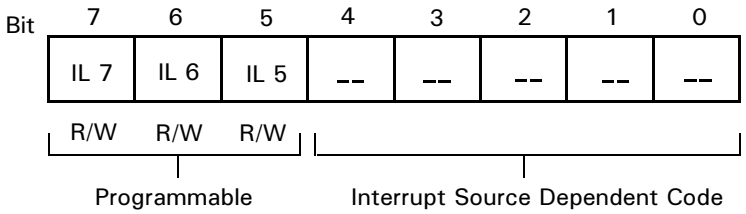


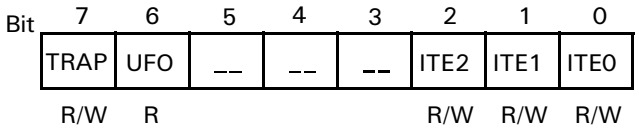

**Figure 74. Interrupt Vector Low Register (IL: I/O Address = 33H)**

## INT/TRAP CONTROL REGISTER

This register is used in handling TRAP interrupts and to enable or disable Maskable Interrupt Level 0 and the $\overline{INT1}$ and $\overline{INT2}$ pins.

### INT/TRAP Control Register

**Mnemonics ITC**
**Address 34H**




**TRAP (Bit 7).** This bit is set to 1 when an undefined opcode is fetched. TRAP can be reset under program control by writing it with a 0; however, TRAP cannot be written with 1 under program control. TRAP is reset to 0 during RESET.

**UFO: Undefined Fetch Object (Bit 6).** When a TRAP interrupt occurs, the contents of UFO allow the starting address of the undefined instruction to be determined. This interrupt is necessary because the TRAP may occur on either the second or third byte of the opcode. UFO allows the stacked PC value to be correctly adjusted. If UFO = 0, the first opcode should be interpreted as the stacked PC-1. If UFO = 1, the first opcode address is stacked PC-2. UFO is Read-Only.

**ITE2, 1, 0: Interrupt Enable 2, 1, 0 (Bits 2–0).** ITE2 and ITE1 enable and disable the external interrupt inputs $\overline{INT2}$ and $\overline{INT1}$, respectively. ITE0 enables and disables interrupts from:

- ESCC
- Bidirectional Centronics controller
- CTCs
- External interrupt input $\overline{INT0}$

A 1 in a bit enables the corresponding interrupt level while a 0 disables it. A RESET sets ITE0 to 1 and clears ITE1 and ITE2 to 0.

**TRAP Interrupt.** The Z8S180/Z8L180 generates a TRAP sequence when an undefined opcode fetch occurs. This feature can be used to increase software reliability, implement an *extended* instruction set, or both. TRAP may occur during opcode fetch cycles and also if an undefined opcode is fetched during the interrupt acknowledge cycle for $\overline{INT0}$ when Mode 0 is used.

When a TRAP sequence occurs, the Z8S180/Z8L180:

1. Sets the TRAP bit in the Interrupt TRAP/Control (ITC) register to 1.
2. Saves the current Program Counter (PC) value, reflecting the location of the undefined opcode, on the stack.
3. Resumes execution at logical address 0.

**Note:** If logical address 0000H is mapped to physical address 00000H, the vector is the same as for RESET. In this case, testing the TRAP bit in ITC reveals whether the restart at physical address 00000H was caused by RESET or TRAP.

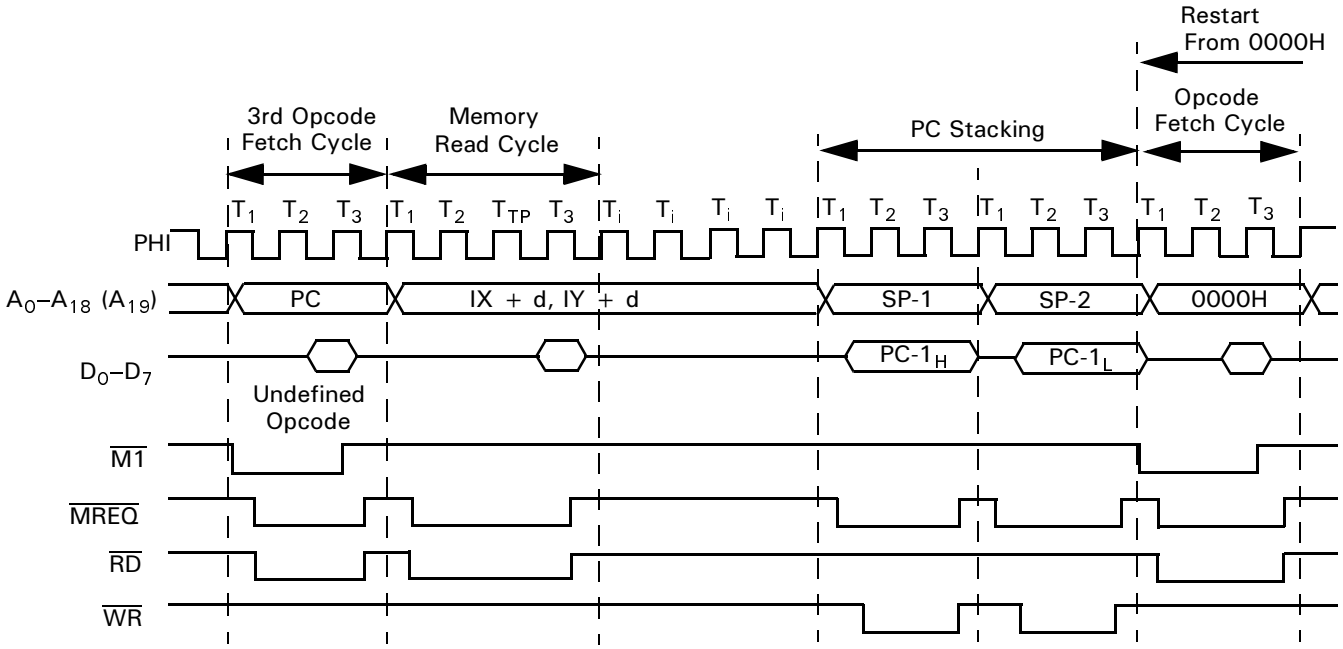



**Figure 76. TRAP Timing—3rd Opcode Undefined**

## MMU COMMON BASE REGISTER

The Common Base Register (CBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical address for Common Area 1 accesses. All bits of CBR are reset to 0 during RESET.

### MMU Common Base Register

**Mnemonic CBR**
**Address 38H**

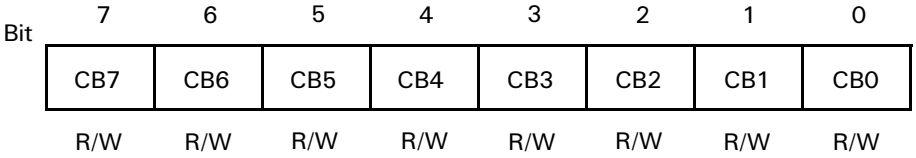



**Figure 78. MMU Common Base Register (CBR: I/O Address = 38H)**

## MMU BANK BASE REGISTER

The Bank Base Register (BBR) specifies the base address (on 4-KB boundaries) used to generate a 20-bit physical address for Bank Area accesses. All bits of BBR are reset to 0 during RESET.

### MMU Bank Base Register

**Mnemonic BBR**
**Address 39H**

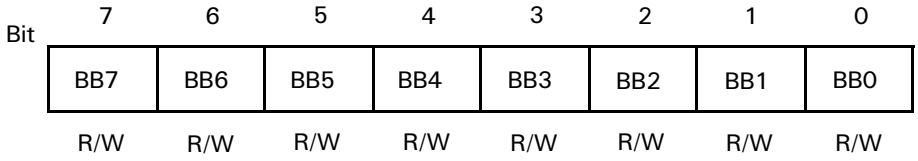



**Figure 79. MMU Bank Base Register (BBR: I/O Address = 39H)**

## MMU COMMON/BANK AREA REGISTER

The Common/Bank Area Register (CBAR) specifies boundaries within the Z8S180/Z8L180 64-KB logical address space for up to three areas; Common Area), Bank Area and Common Area 1.

### MMU Common/Bank Area Register

**Mnemonic CBAR**
**Address 3AH**

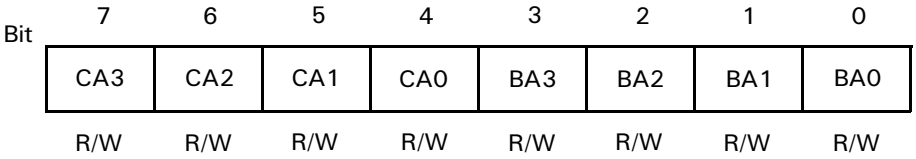
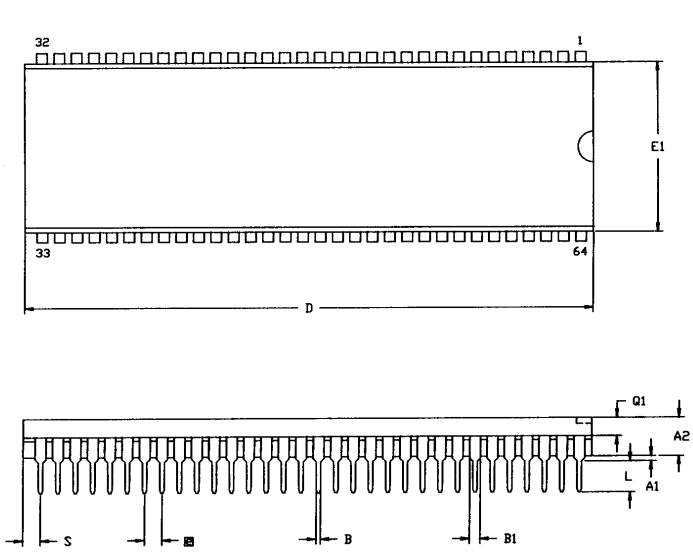



**Figure 80. MMU Common/Bank Area Register (CBAR: I/O Address = 3AH)**

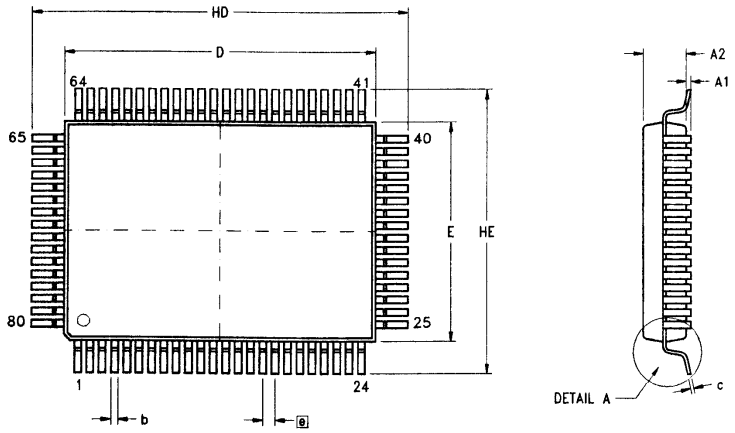
## PACKAGE INFORMATION




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A1 | 0.38 | 1.07 | .015 | .042 |
| A2 | 3.68 | 3.94 | .145 | .155 |
| B | 0.38 | 0.53 | .015 | .021 |
| B1 | 0.94 | 1.09 | .037 | .043 |
| C | 0.23 | 0.38 | .009 | .015 |
| D | 57.40 | 58.17 | 2.260 | 2.290 |
| E | 18.80 | 19.30 | .740 | .760 |
| E1 | 16.76 | 17.27 | .660 | .680 |
| e | 1.78 TYP | | .070 TYP | |
| eA | 19.30 | 20.32 | .760 | .800 |
| L | 3.18 | 3.81 | .125 | .150 |
| Q1 | 1.65 | 1.91 | .065 | .075 |
| S | 1.02 | 1.78 | .040 | .070 |

CONTROLLING DIMENSIONS : INCH

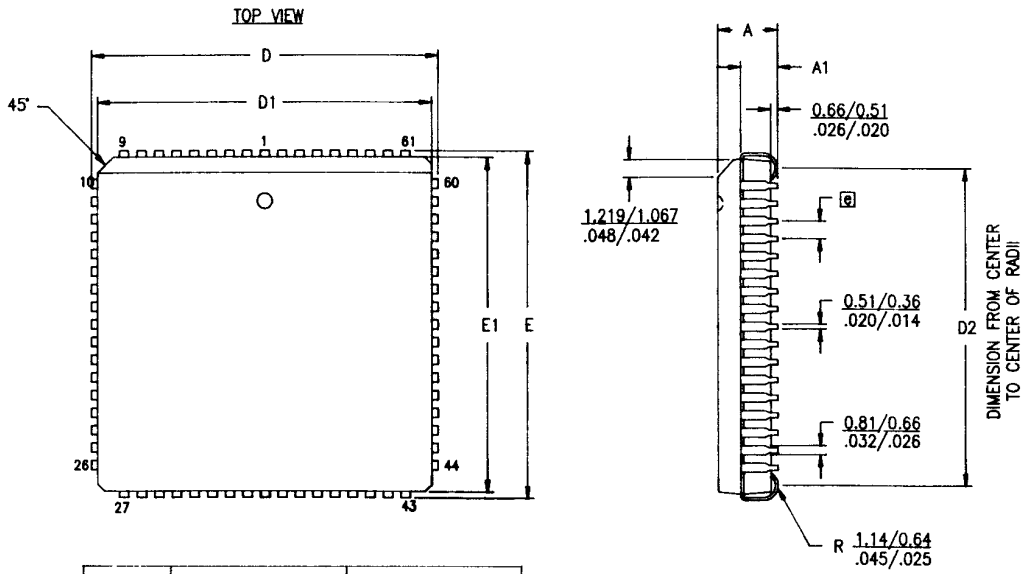
**Figure 85. 64-Pin DIP Package Diagram**




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A1 | 0.10 | 0.30 | .004 | .012 |
| A2 | 2.60 | 2.80 | .102 | .110 |
| b | 0.30 | 0.45 | .012 | .018 |
| c | 0.13 | 0.20 | .005 | .008 |
| HD | 23.70 | 24.15 | .933 | .951 |
| D | 19.90 | 20.10 | .783 | .791 |
| HE | 17.70 | 18.15 | .697 | .715 |
| E | 13.90 | 14.10 | .547 | .555 |
| e | 0.80 TYP | | .0315 TYP | |
| L | 0.70 | 1.10 | .028 | .043 |

NOTES:
1. CONTROLLING DIMENSIONS: MILLIMETER
2. MAX COPLANARITY: .10 / .004

**Figure 86. 80-Pin QFP Package Diagram**




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 4.32 | 4.57 | .170 | .180 |
| A1 | 2.43 | 2.92 | .095 | .115 |
| D/E | 25.02 | 25.40 | .985 | 1.000 |
| D1/E1 | 24.13 | 24.33 | .950 | .958 |
| D2 | 22.86 | 23.62 | .900 | .930 |
| e | 1.27 TYP | | .050 TYP | |

NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN RANGE.
3. DIMENSION : MM / INCH

**Figure 87. 68-Pin PLCC Package Diagram**