



Welcome to [E-XFL.COM](http://E-XFL.COM)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	6
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	16 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f011apb020sc">https://www.e-xfl.com/product-detail/zilog/z8f011apb020sc</a>

## Block Diagram

Figure 1 displays the block diagram of the architecture of the Z8 Encore! XP<sup>®</sup> F082A Series devices.

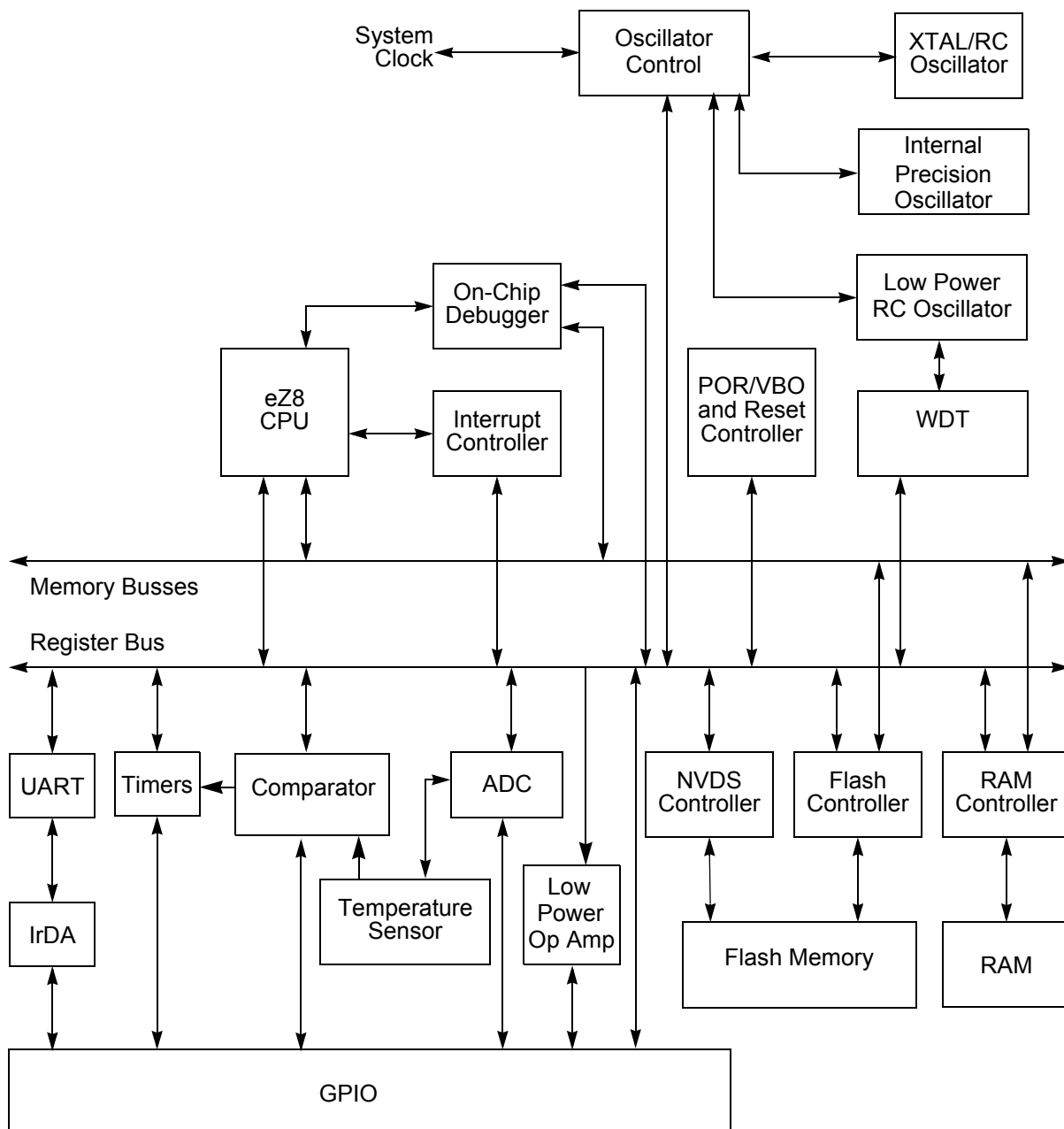


Figure 1. Z8 Encore! XP F082A Series Block Diagram

## **Low-Power Operational Amplifier**

The optional low-power operational amplifier (LPO) is a general-purpose amplifier primarily targeted for current sense applications. The LPO output may be routed internally to the ADC or externally to a pin.

## **Internal Precision Oscillator**

The internal precision oscillator (IPO) is a trimmable clock source that requires no external components.

## **Temperature Sensor**

The optional temperature sensor produces an analog output proportional to the device temperature. This signal can be sent to either the ADC or the analog comparator.

## **Analog Comparator**

The analog comparator compares the signal at an input pin with either an internal programmable voltage reference or a second input pin. The comparator output can be used to drive either an output pin or to generate an interrupt.

## **External Crystal Oscillator**

The crystal oscillator circuit provides highly accurate clock frequencies with the use of an external crystal, ceramic resonator or RC network.

## **Low Voltage Detector**

The low voltage detector (LVD) is able to generate an interrupt when the supply voltage drops below a user-programmable level. The LVD is available on 8-pin devices only.

## **On-Chip Debugger**

The Z8 Encore! XP<sup>®</sup> F082A Series products feature an integrated on-chip debugger (OCD) accessed via a single-pin interface. The OCD provides a rich-set of debugging capabilities, such as reading and writing registers, programming Flash memory, setting breakpoints, and executing code.

The pin configurations listed are preliminary and subject to change based on manufacturing limitations.

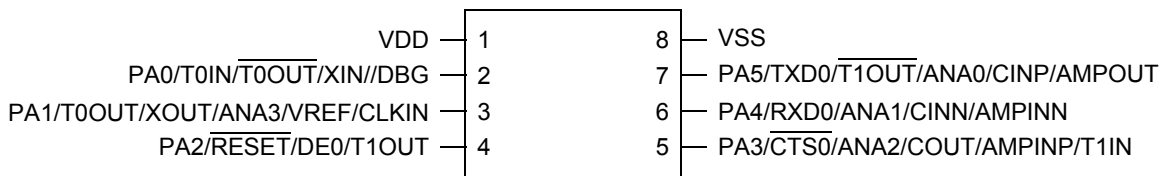


Figure 2. Z8F08xA, Z8F04xA, Z8F02xA, and Z8F01xA in 8-Pin SOIC, QFN/MLF-S, or PDIP Package

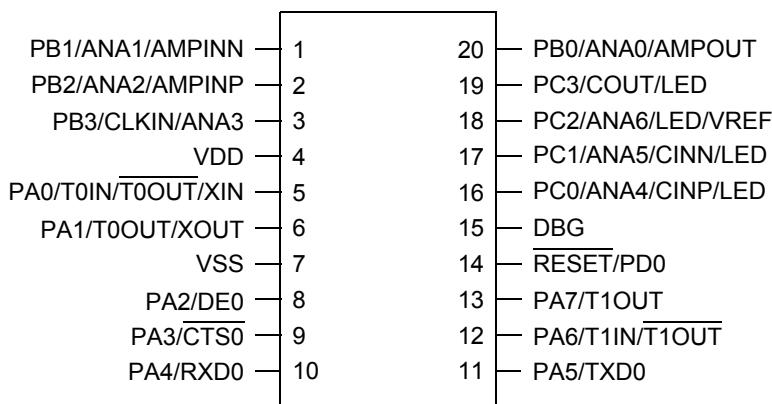


Figure 3. Z8F08xA, Z8F04xA, Z8F02xA, and Z8F01xA in 20-Pin SOIC, SSOP or PDIP Package

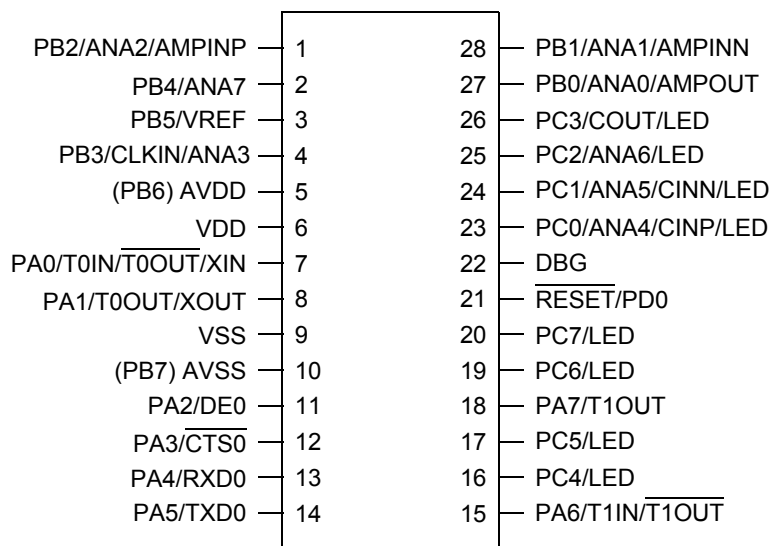


Figure 4. Z8F08xA, Z8F04xA, Z8F02xA, and Z8F01xA in 28-Pin SOIC, SSOP or PDIP Package

# Address Space

The eZ8 CPU can access the following three distinct address spaces:

1. The Register File contains addresses for the general-purpose registers and the eZ8 CPU, peripheral, and general-purpose I/O port control registers.
2. The Program Memory contains addresses for all memory locations having executable code and/or data.
3. The Data Memory contains addresses for all memory locations that contain data only.

These three address spaces are covered briefly in the following subsections. For more information on eZ8 CPU and its address space, refer to *eZ8 CPU Core User Manual (UM0128)* available for download at [www.zilog.com](http://www.zilog.com).

## Register File

The Register File address space in the Z8 Encore!<sup>®</sup> MCU is 4 KB (4096 bytes). The Register File is composed of two sections: control registers and general-purpose registers. When instructions are executed, registers defined as sources are read, and registers defined as destinations are written. The architecture of the eZ8 CPU allows all general-purpose registers to function as accumulators, address pointers, index registers, stack areas, or scratch pad memory.

The upper 256 bytes of the 4 KB Register File address space are reserved for control of the eZ8 CPU, the on-chip peripherals, and the I/O ports. These registers are located at addresses from F00H to FFFH. Some of the addresses within the 256 B control register section are reserved (unavailable). Reading from a reserved Register File address returns an undefined value. Writing to reserved Register File addresses is not recommended and can produce unpredictable results.

The on-chip RAM always begins at address 000H in the Register File address space. The Z8 Encore! XP<sup>®</sup> F082A Series devices contain 256 B to 1 KB of on-chip RAM. Reading from Register File addresses outside the available RAM addresses (and not within the control register address space) returns an undefined value. Writing to these Register File addresses produces no effect.

## Program Memory

The eZ8 CPU supports 64 KB of Program Memory address space. The Z8 Encore! XP F082A Series devices contain 1 KB to 8 KB of on-chip Flash memory in the Program Memory address space, depending on the device. Reading from Program Memory

*initiate Stop Mode Recovery without being written to the Port Input Data register or without initiating an interrupt (if enabled for that pin).*

## Stop Mode Recovery Using the External $\overline{\text{RESET}}$ Pin

When the Z8 Encore! XP F082A Series device is in STOP mode and the external  $\overline{\text{RESET}}$  pin is driven Low, a system reset occurs. Because of a glitch filter operating on the  $\overline{\text{RESET}}$  pin, the Low pulse must be greater than the minimum width specified, or it is ignored. See [Electrical Characteristics](#) on page 221 for details.

## Low Voltage Detection

In addition to the Voltage Brownout (VBO) Reset described above, it is also possible to generate an interrupt when the supply voltage drops below a user-selected value. For details about configuring the Low Voltage Detection (LVD) and the threshold levels available, see [Trim Bit Address 0003H](#) on page 159. The LVD function is available on the 8-pin product versions only.

When the supply voltage drops below the LVD threshold, the LVD bit of the Reset Status (RSTSTAT) register is set to one. This bit remains one until the low-voltage condition goes away. Reading or writing this bit does not clear it. The LVD circuit can also generate an interrupt when so enabled, see [Interrupt Vectors and Priority](#) on page 58. The LVD bit is NOT latched, so enabling the interrupt is the only way to guarantee detection of a transient low voltage event.

The LVD functionality depends on circuitry shared with the VBO block; therefore, disabling the VBO also disables the LVD.

## Reset Register Definitions

The following sections define the Reset registers.

### Reset Status Register

The Reset Status (RSTSTAT) register is a read-only register that indicates the source of the most recent Reset event, indicates a Stop Mode Recovery event, and indicates a Watchdog Timer time-out. Reading this register resets the upper four bits to 0.

This register shares its address with the Watchdog Timer control register, which is write-only (see [Table 11](#) on page 31).

function). (Push-pull output)

1 = The source current for the associated pin is disabled (open-drain mode).

### Port A–D High Drive Enable Sub-Registers

The Port A–D High Drive Enable sub-register (Table 22) is accessed through the Port A–D Control register by writing 04H to the Port A–D Address register. Setting the bits in the Port A–D High Drive Enable sub-registers to 1 configures the specified port pins for high current output drive operation. The Port A–D High Drive Enable sub-register affects the pins directly and, as a result, alternate functions are also affected.

**Table 22. Port A–D High Drive Enable Sub-Registers (PxHDE)**

BITS	7	6	5	4	3	2	1	0
FIELD	PHDE7	PHDE6	PHDE5	PHDE4	PHDE3	PHDE2	PHDE1	PHDE0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	If 04H in Port A–D Address Register, accessible through the Port A–D Control Register							

PHDE[7:0]—Port High Drive Enabled

0 = The Port pin is configured for standard output current drive.

1 = The Port pin is configured for high output current drive.

### Port A–D Stop Mode Recovery Source Enable Sub-Registers

The Port A–D Stop Mode Recovery Source Enable sub-register (Table 23) is accessed through the Port A–D Control register by writing 05H to the Port A–D Address register. Setting the bits in the Port A–D Stop Mode Recovery Source Enable sub-registers to 1 configures the specified Port pins as a Stop Mode Recovery source. During STOP mode, any logic transition on a Port pin enabled as a Stop Mode Recovery source initiates Stop Mode Recovery.

**Table 23. Port A–D Stop Mode Recovery Source Enable Sub-Registers (PxSMRE)**

BITS	7	6	5	4	3	2	1	0
FIELD	PSMRE7	PSMRE6	PSMRE5	PSMRE4	PSMRE3	PSMRE2	PSMRE1	PSMRE0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	If 05H in Port A–D Address Register, accessible through the Port A–D Control Register							

PSMRE[7:0]—Port Stop Mode Recovery Source Enabled

0 = The Port pin is not configured as a Stop Mode Recovery source. Transitions on this pin

Watchdog Timer Reload Registers results in a one-second timeout at room temperature and 3.3 V supply voltage.

Timeouts other than one second may be obtained by scaling the calibration values up or down as required.

► **Note:** *The Watchdog Timer accuracy still degrades as temperature and supply voltage vary. See [Table 133](#) on page 230 for details.*

## Watchdog Timer Control Register Definitions

### Watchdog Timer Control Register

The Watchdog Timer Control (WDTCTL) register is a write-only control register. Writing the 55H, AAH unlock sequence to the WDTCTL register address unlocks the three Watchdog Timer Reload Byte registers (WDTU, WDTL, and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL register address produce no effect on the bits in the WDTCTL register. The locking mechanism prevents spurious writes to the Reload registers.

This register address is shared with the read-only Reset Status register.

**Table 57. Watchdog Timer Control Register (WDTCTL)**

BITS	7	6	5	4	3	2	1	0
FIELD	WDTUNLK							
RESET	X	X	X	X	X	X	X	X
R/W	W	W	W	W	W	W	W	W
ADDR	FF0H							
X = Undefined.								

WDTUNLK—Watchdog Timer Unlock

The software must write the correct unlocking sequence to this register before it is allowed to modify the contents of the Watchdog Timer reload registers.

### Watchdog Timer Reload Upper, High and Low Byte Registers

The Watchdog Timer Reload Upper, High and Low Byte (WDTU, WDTL, and WDTL) registers ([Table 58](#) through [Table 60](#)) form the 24-bit reload value that is loaded into the Watchdog Timer when a WDT instruction executes. The 24-bit reload value is {WDTU[7:0], WDTL[7:0], WDTL[7:0]}. Writing to these registers sets the appropriate Reload Value. Reading from these registers returns the current Watchdog Timer count value.





configuration bits. In general, the address compare feature reduces the load on the CPU, because it does not require access to the UART when it receives data directed to other devices on the multi-node network. The following three MULTIPROCESSOR modes are available in hardware:

1. Interrupt on all address bytes.
2. Interrupt on matched address bytes and correctly framed data bytes.
3. Interrupt only on correctly framed data bytes.

These modes are selected with MPMD [1 : 0] in the UART Control 1 Register. For all multiprocessor modes, bit MPEN of the UART Control 1 Register must be set to 1.

The first scheme is enabled by writing 01b to MPMD[1:0]. In this mode, all incoming address bytes cause an interrupt, while data bytes never cause an interrupt. The interrupt service routine must manually check the address byte that caused triggered the interrupt. If it matches the UART address, the software clears MPMD[0]. Each new incoming byte interrupts the CPU. The software is responsible for determining the end of the frame. It checks for the end-of-frame by reading the MPRX bit of the UART Status 1 Register for each incoming byte. If MPRX=1, a new frame has begun. If the address of this new frame is different from the UART's address, MPMD[0] must be set to 1 causing the UART interrupts to go inactive until the next address byte. If the new frame's address matches the UART's, the data in the new frame is processed as well.

The second scheme requires the following: set MPMD[1:0] to 10B and write the UART's address into the UART Address Compare Register. This mode introduces additional hardware control, interrupting only on frames that match the UART's address. When an incoming address byte does not match the UART's address, it is ignored. All successive data bytes in this frame are also ignored. When a matching address byte occurs, an interrupt is issued and further interrupts now occur on each successive data byte. When the first data byte in the frame is read, the NEWFRM bit of the UART Status 1 Register is asserted. All successive data bytes have NEWFRM=0. When the next address byte occurs, the hardware compares it to the UART's address. If there is a match, the interrupts continues and the NEWFRM bit is set for the first byte of the new frame. If there is no match, the UART ignores all incoming bytes until the next address match.

The third scheme is enabled by setting MPMD[1:0] to 11b and by writing the UART's address into the UART Address Compare Register. This mode is identical to the second scheme, except that there are no interrupts on address bytes. The first data byte of each frame remains accompanied by a NEWFRM assertion.

## External Driver Enable

The UART provides a Driver Enable (DE) signal for off-chip bus transceivers. This feature reduces the software overhead associated with using a GPIO pin to control the transceiver when communicating on a multi-transceiver bus, such as RS-485.

0 = No framing error occurred.

1 = A framing error occurred.

**BRKD**—Break Detect

This bit indicates that a break occurred. If the data bits, parity/multiprocessor bit, and Stop bit(s) are all 0s this bit is set to 1. Reading the UART Receive Data register clears this bit.

0 = No break occurred.

1 = A break occurred.

**TDRE**—Transmitter Data Register Empty

This bit indicates that the UART Transmit Data register is empty and ready for additional data. Writing to the UART Transmit Data register resets this bit.

0 = Do not write to the UART Transmit Data register.

1 = The UART Transmit Data register is ready to receive an additional byte to be transmitted.

**TXE**—Transmitter Empty

This bit indicates that the transmit shift register is empty and character transmission is finished.

0 = Data is currently transmitting.

1 = Transmission is complete.

**CTS**— $\overline{\text{CTS}}$  signal

When this bit is read it returns the level of the  $\overline{\text{CTS}}$  signal. This signal is active Low.

## UART Status 1 Register

This register contains multiprocessor control and status bits.

**Table 64. UART Status 1 Register (U0STAT1)**

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved						NEWFRM	MPRX
RESET	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R	R
ADDR	F44H							

Reserved—Must be 0.

**NEWFRM**—Status bit denoting the start of a new frame. Reading the UART Receive Data register resets this bit to 0.

0 = The current byte is not the first data byte of a new frame.

1 = The current byte is the first data byte of a new frame.

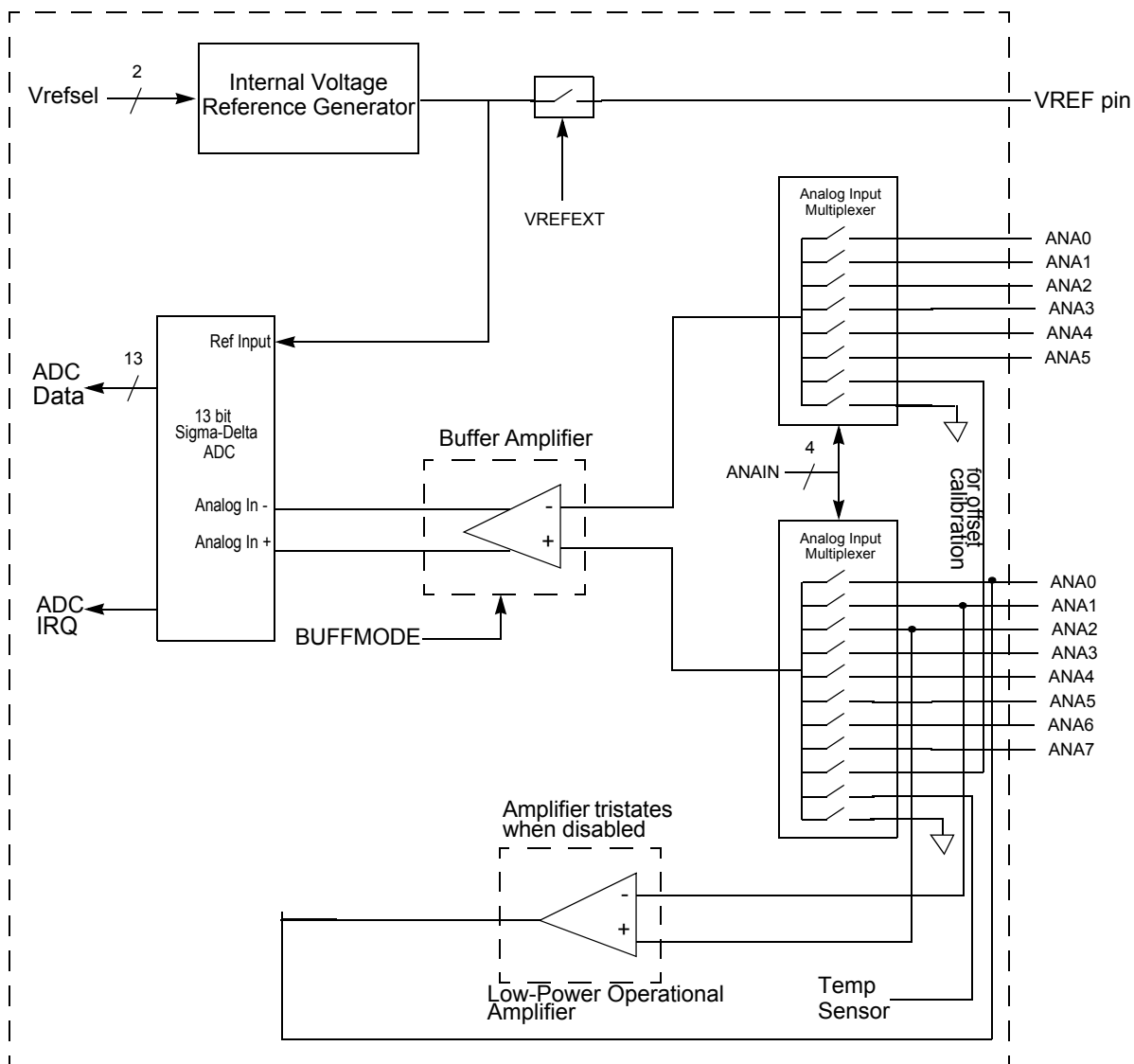


Figure 19. Analog-to-Digital Converter Block Diagram

## Operation

### Data Format

In both SINGLE-ENDED and DIFFERENTIAL modes, the effective output of the ADC is an 11-bit, signed, two's complement digital value. In DIFFERENTIAL mode, the ADC

## ADC Control/Status Register 1

The ADC Control/Status Register 1 (ADCCTL1) configures the input buffer stage, enables the threshold interrupts and contains the status of both threshold triggers. It is also used to select the voltage reference configuration.

**Table 72. ADC Control/Status Register 1 (ADCCTL1)**

BITS	7	6	5	4	3	2	1	0
FIELD	REFSELH	Reserved				BUFMODE[2:0]		
RESET	1	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F71H							

REFSELH—Voltage Reference Level Select High Bit; in conjunction with the Low bit (REFSELL) in [ADC Control Register 0](#), this determines the level of the internal voltage reference; the following details the effects of {REFSELH, REFSELL}; this reference is independent of the Comparator reference.

00= Internal Reference Disabled, reference comes from external pin

01= Internal Reference set to 1.0 V

10= Internal Reference set to 2.0 V (default)

11= Reserved

BUFMODE[2:0] - Input Buffer Mode Select

000 = Single-ended, unbuffered input

001 = Single-ended, buffered input with unity gain

010 = Reserved

011 = Reserved

100 = Differential, unbuffered input

101 = Differential, buffered input with unity gain

110 = Reserved

111 = Reserved

## ADC Data High Byte Register

The ADC Data High Byte (ADCD\_H) register contains the upper eight bits of the ADC output. The output is an 13-bit two's complement value. During a single-shot conversion, this value is invalid. Access to the ADC Data High Byte register is read-only. Reading the ADC Data High Byte register latches data in the ADC Low Bits register.

Assuming a compensated ADC measurement, the following equation defines the relationship between the ADC reading and the die temperature:

$$T = (25/128) \times (\text{ADC} - \text{TSCAL}[11:2]) + 30$$

where, T is the temperature in C; ADC is the 10-bit compensated ADC value; and TSCAL is the temperature sensor calibration value, ignoring the two least significant bits of the 12-bit value.

See [Temperature Sensor Calibration Data](#) on page 164 for the location of TSCAL.

## Calibration

The temperature sensor undergoes calibration during the manufacturing process and is maximally accurate at 30 °C. Accuracy decreases as measured temperatures move further from the calibration point.

# Flash Memory

The products in the Z8 Encore! XP<sup>®</sup> F082A Series feature a non-volatile Flash memory of 8 KB (8192), 4 KB (4096), 2 KB (2048 bytes), or 1 KB (1024) with read/write/erase capability. The Flash Memory can be programmed and erased in-circuit by user code or through the On-Chip Debugger. The features include:

- User controlled read and write protect capability
- Sector-based write protection scheme
- Additional protection schemes against accidental program and erasure

## Architecture

The Flash memory array is arranged in pages with 512 bytes per page. The 512 byte page is the minimum Flash block size that can be erased. Each page is divided into 8 rows of 64 bytes.

For program or data protection, the Flash memory is also divided into sectors. In the Z8 Encore! XP F082A Series, these sectors are either 1024 bytes (in the 8 KB devices) or 512 bytes (all other memory sizes) in size. Page and sector sizes are not generally equal.

The first 2 bytes of the Flash Program memory are used as Flash Option Bits. For more information about their operation, see [Flash Option Bits](#) on page 153.

[Table 76](#) describes the Flash memory configuration for each device in the Z8 Encore! XP F082A Series. [Figure 21](#) displays the Flash memory arrangement.

**Table 76. Z8 Encore! XP F082A Series Flash Memory Configurations**

Part Number	Flash Size KB (Bytes)	Flash Pages	Program Memory Addresses	Flash Sector Size (Bytes)
Z8F08xA	8 (8192)	16	0000H–1FFFH	1024
Z8F04xA	4 (4096)	8	0000H–0FFFH	512
Z8F02xA	2 (2048)	4	0000H–07FFH	512
Z8F01xA	1 (1024)	2	0000H–03FFH	512

## Option Bit Types

### User Option Bits

The user option bits are contained in the first two bytes of program memory. User access to these bits has been provided because these locations contain application-specific device configurations. The information contained here is lost when page 0 of the program memory is erased.

### Trim Option Bits

The trim option bits are contained in the information page of the Flash memory. These bits are factory programmed values required to optimize the operation of onboard analog circuitry and cannot be permanently altered. Program Memory may be erased without endangering these values. It is possible to alter working values of these bits by accessing the Trim Bit Address and Data Registers, but these working values are lost after a power loss or any other reset event.

There are 32 bytes of trim data. To modify one of these values the user code must first write a value between 00H and 1FH into the Trim Bit Address Register. The next write to the Trim Bit Data register changes the working value of the target trim data byte.

Reading the trim data requires the user code to write a value between 00H and 1FH into the Trim Bit Address Register. The next read from the Trim Bit Data register returns the working value of the target trim data byte.

► **Note:** *The trim address range is from information address 20-3F only. The remainder of the information page is not accessible through the trim bit address and data registers.*

### Calibration Option Bits

The calibration option bits are also contained in the information page. These bits are factory programmed values intended for use in software correcting the device's analog performance. To read these values, the user code must employ the LDC instruction to access the information area of the address space as defined in [See Flash Information Area](#) on page 17.

### Serialization Bits

As an optional feature, Zilog<sup>®</sup> is able to provide factory-programmed serialization. For serialized products, the individual devices are programmed with unique serial numbers. These serial numbers are binary values, four bytes in length. The numbers increase in size with each device, but gaps in the serial sequence may exist.

These serial numbers are stored in the Flash information page (see [Reading the Flash Information Page](#) on page 155 and [Serialization Data](#) on page 165 for more details) and are unaffected by mass erasure of the device's Flash memory.



**DBGACK—Debug Acknowledge**

This bit enables the debug acknowledge feature. If this bit is set to 1, the OCD sends a Debug Acknowledge character (FFH) to the host when a Breakpoint occurs.

0 = Debug Acknowledge is disabled.

1 = Debug Acknowledge is enabled.

Reserved—Must be 0.

**RST—Reset**

Setting this bit to 1 resets the Z8F04xA family device. The device goes through a normal Power-On Reset sequence with the exception that the On-Chip Debugger is not reset. This bit is automatically cleared to 0 at the end of reset.

0 = No effect.

1 = Reset the Flash Read Protect Option Bit device.

## OCD Status Register

The OCD Status register reports status information about the current state of the debugger and the system.

**Table 107. OCD Status Register (OCDSTAT)**

BITS	7	6	5	4	3	2	1	0
FIELD	DBG	HALT	FRPENB	Reserved				
RESET	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

**DBG—Debug Status**

0 = NORMAL mode

1 = DEBUG mode

**HALT—HALT Mode**

0 = Not in HALT mode

1 = In HALT mode

**FRPENB—Flash Read Protect Option Bit Enable**

0 = FRP bit enabled, that allows disabling of many OCD commands

1 = FRP bit has no effect

Reserved—Must be 0

**Table 128. Power Consumption (Continued)**

$V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$						
Maximum <sup>2</sup> Maximum <sup>3</sup>						
Symbol	Parameter	Typical <sup>1</sup>	Std Temp	Ext Temp	Units	Conditions
$I_{DD}$ LPO	Low-Power Operational Amplifier Supply Current	3	5	5	$\mu\text{A}$	Driving a high-impedance load
$I_{DD}$ TS	Temperature Sensor Supply Current	60			$\mu\text{A}$	See <a href="#">Notes 4</a>
$I_{DD}$ BG	Band Gap Supply Current	320	480	500	$\mu\text{A}$	For 20-/28-pin devices
						For 8-pin devices

**Notes**

1. Typical conditions are defined as  $V_{DD} = 3.3 \text{ V}$  and  $+30 \text{ }^{\circ}\text{C}$ .
2. Standard temperature is defined as  $T_A = 0 \text{ }^{\circ}\text{C}$  to  $+70 \text{ }^{\circ}\text{C}$ ; these values not tested in production for worst case behavior, but are derived from product characterization and provided for design guidance only.
3. Extended temperature is defined as  $T_A = -40 \text{ }^{\circ}\text{C}$  to  $+105 \text{ }^{\circ}\text{C}$ ; these values not tested in production for worst case behavior, but are derived from product characterization and provided for design guidance only.
4. For this block to operate, the bandgap circuit is automatically turned on and must be added to the total supply current. This bandgap current is only added once, regardless of how many peripherals are using it.

**Table 132. Flash Memory Electrical Characteristics and Timing**

$V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$ $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$ (unless otherwise stated)					
Parameter	Minimum	Typical	Maximum	Units	Notes
Flash Byte Read Time	100	–	–	ns	
Flash Byte Program Time	20	–	40	$\mu\text{s}$	
Flash Page Erase Time	10	–	–	ms	
Flash Mass Erase Time	200	–	–	ms	
Writes to Single Address Before Next Erase	–	–	2		
Flash Row Program Time	–	–	8	ms	Cumulative program time for single row cannot exceed limit before next erase. This parameter is only an issue when bypassing the Flash Controller.
Data Retention	100	–	–	years	25 $^{\circ}\text{C}$
Endurance	10,000	–	–	cycles	Program/erase cycles

**Table 133. Watchdog Timer Electrical Characteristics and Timing**

V <sub>DD</sub> = 2.7 V to 3.6 V T <sub>A</sub> = -40 °C to +105 °C (unless otherwise stated)						
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions
F <sub>WDT</sub>	WDT Oscillator Frequency		10		kHz	
F <sub>WDT</sub>	WDT Oscillator Error			±50	%	
T <sub>WDT<sub>CAL</sub></sub>	WDT Calibrated Timeout	0.98	1	1.02	s	V <sub>DD</sub> = 3.3 V; T <sub>A</sub> = 30 °C
		0.70	1	1.30	s	V <sub>DD</sub> = 2.7 V to 3.6 V T <sub>A</sub> = 0 °C to 70 °C
		0.50	1	1.50	s	V <sub>DD</sub> = 2.7 V to 3.6 V T <sub>A</sub> = -40 °C to +105 °C

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
<b>Z8 Encore! XP<sup>®</sup> F082A Series with 1 KB Flash</b>											
<b>Standard Temperature: 0 °C to 70 °C</b>											
Z8F011APB020SC	1 KB	256 B	16 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F011AQB020SC	1 KB	256 B	16 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F011ASB020SC	1 KB	256 B	16 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F011ASH020SC	1 KB	256 B	16 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F011AHH020SC	1 KB	256 B	16 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F011APH020SC	1 KB	256 B	16 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F011ASJ020SC	1 KB	256 B	16 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F011AHJ020SC	1 KB	256 B	16 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F011APJ020SC	1 KB	256 B	16 B	25	19	2	0	1	1	0	PDIP 28-pin package
<b>Extended Temperature: -40 °C to 105 °C</b>											
Z8F011APB020EC	1 KB	256 B	16 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F011AQB020EC	1 KB	256 B	16 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F011ASB020EC	1 KB	256 B	16 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F011ASH020EC	1 KB	256 B	16 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F011AHH020EC	1 KB	256 B	16 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F011APH020EC	1 KB	256 B	16 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F011ASJ020EC	1 KB	256 B	16 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F011AHJ020EC	1 KB	256 B	16 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F011APJ020EC	1 KB	256 B	16 B	25	19	2	0	1	1	0	PDIP 28-pin package
Replace C with G for Lead-Free Packaging											

## **Customer Support**

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at <http://www.zilog.com/kb>.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at <http://support.zilog.com>.