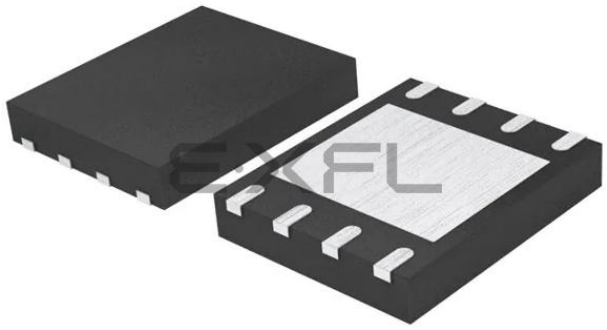

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | eZ8 |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | IrDA, UART/USART |
| Peripherals | Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT |
| Number of I/O | 6 |
| Program Memory Size | 1KB (1K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 16 x 8 |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 8-VDFN Exposed Pad |
| Supplier Device Package | 8-QFN (5x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8f011aqb020sc |

# Register Map

Table 7 provides the address map for the Register File of the Z8 Encore! XP® F082A Series devices. Not all devices and package styles in the Z8 Encore! XP F082A Series support the ADC, or all of the GPIO Ports. Consider registers for unimplemented peripherals as Reserved.

**Table 7. Register File Address Map**

| Address (Hex) | Register Description | Mnemonic | Reset (Hex) | Page No |
|---|---|---|---|---|
| **General-Purpose RAM** | | | | |
| **Z8F082A/Z8F081A Devices** | | | | |
| 000–3FF | General-Purpose Register File RAM | — | XX | |
| 400–EFF | Reserved | — | XX | |
| **Z8F042A/Z8F041A Devices** | | | | |
| 000–3FF | General-Purpose Register File RAM | — | XX | |
| 400–EFF | Reserved | — | XX | |
| **Z8F022A/Z8F021A Devices** | | | | |
| 000–1FF | General-Purpose Register File RAM | — | XX | |
| 200–EFF | Reserved | — | XX | |
| **Z8F012A/Z8F011A Devices** | | | | |
| 000–0FF | General-Purpose Register File RAM | — | XX | |
| 100–EFF | Reserved | — | XX | |
| **Timer 0** | | | | |
| F00 | Timer 0 High Byte | T0H | 00 | 87 |
| F01 | Timer 0 Low Byte | T0L | 01 | 87 |
| F02 | Timer 0 Reload High Byte | T0RH | FF | 88 |
| F03 | Timer 0 Reload Low Byte | T0RL | FF | 88 |
| F04 | Timer 0 PWM High Byte | T0PWMH | 00 | 88 |
| F05 | Timer 0 PWM Low Byte | T0PWML | 00 | 89 |
| F06 | Timer 0 Control 0 | T0CTL0 | 00 | 83 |
| F07 | Timer 0 Control 1 | T0CTL1 | 00 | 84 |
| **Timer 1** | | | | |
| F08 | Timer 1 High Byte | T1H | 00 | 87 |
| F09 | Timer 1 Low Byte | T1L | 01 | 87 |
| F0A | Timer 1 Reload High Byte | T1RH | FF | 88 |

XX=Undefined

**Table 8. Reset and Stop Mode Recovery Characteristics and Latency**

| | Reset Characteristics and Latency | | |
|---|---|---|---|
| **Reset Type** | **Control Registers** | **eZ8 CPU** | **Reset Latency (Delay)** |
| System Reset | Reset (as applicable) | Reset | 66 Internal Precision Oscillator Cycles |
| System Reset with Crystal Oscillator Enabled | Reset (as applicable) | Reset | 5000 Internal Precision Oscillator Cycles |
| Stop Mode Recovery | Unaffected, except WDT_CTL and OSC_CTL registers | Reset | 66 Internal Precision Oscillator Cycles + IPO startup time |
| Stop Mode Recovery with Crystal Oscillator Enabled | Unaffected, except WDT_CTL and OSC_CTL registers | Reset | 5000 Internal Precision Oscillator Cycles |

During a System Reset or Stop Mode Recovery, the Internal Precision Oscillator requires 4 µs to start up. Then the Z8 Encore! XP F082A Series device is held in Reset for 66 cycles of the Internal Precision Oscillator. If the crystal oscillator is enabled in the Flash option bits, this reset period is increased to 5000 IPO cycles. When a reset occurs because of a low voltage condition or Power-On Reset (POR), this delay is measured from the time that the supply voltage first exceeds the POR level. If the external pin reset remains asserted at the end of the reset period, the device remains in reset until the pin is deasserted.

At the beginning of Reset, all GPIO pins are configured as inputs with pull-up resistor disabled, except PD0 (or PA2 on 8-pin devices) which is shared with the reset pin. On reset, the PD0 is configured as a bidirectional open-drain reset. The pin is internally driven low during port reset, after which the user code may reconfigure this pin as a general purpose output.

During Reset, the eZ8 CPU and on-chip peripherals are idle; however, the on-chip crystal oscillator and Watchdog Timer oscillator continue to run.

Upon Reset, control registers within the Register File that have a defined Reset value are loaded with their reset values. Other control registers (including the Stack Pointer, Register Pointer, and Flags) and general-purpose RAM are undefined following Reset. The eZ8 CPU fetches the Reset vector at Program Memory addresses 0002H and 0003H and loads that value into the Program Counter. Program execution begins at the Reset vector address.

As the control registers are re-initialized by a system reset, the system clock after reset is always the IPO. The software must reconfigure the oscillator control block, such that the correct system clock source is enabled and selected.

and as long as four. A reset pulse three clock cycles in duration might trigger a reset; a pulse four cycles in duration always triggers a reset.

While the $\overline{\text{RESET}}$ input pin is asserted Low, the Z8 Encore! XP® F082A Series devices remain in the Reset state. If the $\overline{\text{RESET}}$ pin is held Low beyond the System Reset time-out, the device exits the Reset state on the system clock rising edge following $\overline{\text{RESET}}$ pin deassertion. Following a System Reset initiated by the external $\overline{\text{RESET}}$ pin, the EXT status bit in the Reset Status (RSTSTAT) register is set to 1.

### External Reset Indicator

During System Reset or when enabled by the GPIO logic (see Port A–D Control Registers on page 46), the $\overline{\text{RESET}}$ pin functions as an open-drain (active Low) reset mode indicator in addition to the input functionality. This reset output feature allows a Z8 Encore! XP F082A Series device to reset other components to which it is connected, even if that reset is caused by internal sources such as POR, VBO or WDT events.

After an internal reset event occurs, the internal circuitry begins driving the $\overline{\text{RESET}}$ pin Low. The $\overline{\text{RESET}}$ pin is held Low by the internal circuitry until the appropriate delay listed in Table 8 has elapsed.

### On-Chip Debugger Initiated Reset

A Power-On Reset can be initiated using the On-Chip Debugger by setting the RST bit in the OCD Control register. The On-Chip Debugger block is not reset but the rest of the chip goes through a normal system reset. The RST bit automatically clears during the system reset. Following the system reset the POR bit in the Reset Status (RSTSTAT) register is set.

## Stop Mode Recovery

STOP mode is entered by execution of a STOP instruction by the eZ8 CPU. See Low-Power Modes on page 33 for detailed STOP mode information. During Stop Mode Recovery (SMR), the CPU is held in reset for 66 IPO cycles if the crystal oscillator is disabled or 5000 cycles if it is enabled. The SMR delay (see Table 131 on page 229) $T_{SMR}$, also includes the time required to start up the IPO.

Stop Mode Recovery does not affect on-chip registers other than the Watchdog Timer Control register (WDTCTL) and the Oscillator Control register (OSCCTL). After any Stop Mode Recovery, the IPO is enabled and selected as the system clock. If another system clock source is required, the Stop Mode Recovery code must reconfigure the oscillator control block such that the correct system clock source is enabled and selected.

The eZ8 CPU fetches the Reset vector at Program Memory addresses 0002H and 0003H and loads that value into the Program Counter. Program execution begins at the Reset

operational amplifier (LPO) is OFF. To use the LPO, clear the LPO bit, turning it ON. Clearing this bit might interfere with normal ADC measurements on ANA0 (the LPO output). This bit enables the amplifier even in STOP mode. If the amplifier is not required in STOP mode, disable it. Failure to perform this results in STOP mode currents greater than specified.

**Note:** *This register is only reset during a POR sequence. Other system reset events do not affect it.*

**Table 12. Power Control Register 0 (PWRCTL0)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | LPO | Reserved | | VBO | TEMP | ADC | COMP | Reserved |
| RESET | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| ADDR | F80H | | | | | | | |

LPO—Low-Power Operational Amplifier Disable
0 = LPO is enabled (this applies even in STOP mode).
1 = LPO is disabled.

Reserved—Must be 0.

VBO—Voltage Brownout Detector Disable
This bit and the VBO_AO Flash option bit must both enable the VBO for the VBO to be active.
0 = VBO Enabled
1 = VBO Disabled

TEMP—Temperature Sensor Disable
0 = Temperature Sensor Enabled
1 = Temperature Sensor Disabled

ADC—Analog-to-Digital Converter Disable
0 = Analog-to-Digital Converter Enabled
1 = Analog-to-Digital Converter Disabled

COMP—Comparator Disable
0 = Comparator is Enabled
1 = Comparator is Disabled

Reserved—Must be 0.

**Note:** *Asserting any power control bit disables the targeted block, regardless of any enable bits contained in the target block's control registers.*

**Table 31. LED Drive Level Low Register (LEDLVLL)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | LEDLVLL[7:0] | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| ADDR | F84H | | | | | | | |

LEDLVLL[7:0]—LED Level Low Bit
{LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin.
00 = 3 mA
01 = 7 mA
10 = 13 mA
11 = 20 mA

# Interrupt Controller

The interrupt controller on the Z8 Encore! XP F082A Series products prioritizes the interrupt requests from the on-chip peripherals and the GPIO port pins. The features of interrupt controller include:

- 20 possible interrupt sources with 18 unique interrupt vectors:
  - Twelve GPIO port pin interrupt sources (two interrupt vectors are shared).
  - Eight on-chip peripheral interrupt sources (two interrupt vectors are shared).
- Flexible GPIO interrupts:
  - Eight selectable rising and falling edge GPIO interrupts.
  - Four dual-edge interrupts.
- Three levels of individually programmable interrupt priority.
- Watchdog Timer and LVD can be configured to generate an interrupt.
- Supports vectored as well as polled interrupts

Interrupt requests (IRQs) allow peripheral devices to suspend CPU operation in an orderly manner and force the CPU to start an interrupt service routine (ISR). Usually this interrupt service routine is involved with the exchange of data, status information, or control information between the CPU and the interrupting peripheral. When the service routine is completed, the CPU returns to the operation from which it was interrupted.

The eZ8 CPU supports both vectored and polled interrupt handling. For polled interrupts, the interrupt controller has no effect on operation. For more information on interrupt servicing by the eZ8 CPU, refer to *eZ8 CPU Core User Manual (UM0128)* available for download at www.zilog.com.

## Interrupt Vector Listing

Table 32 on page 56 lists all of the interrupts available in order of priority. The interrupt vector is stored with the most-significant byte (MSB) at the even Program Memory address and the least-significant byte (LSB) at the following odd Program Memory address.

**Note:** *Some port interrupts are not available on the 8- and 20-pin packages. The ADC interrupt is unavailable on devices not containing an ADC.*

**Caution:** *The following coding style that clears bits in the Interrupt Request registers is not recommended. All incoming interrupts received between execution of the first* `LDX` *command and the final LDX command are lost.*

**Poor coding style that can result in lost interrupt requests:**

```
LDX r0, IRQ0
AND r0, MASK
LDX IRQ0, r0
```

**Caution:** *To avoid missing interrupts, use the following coding style to clear bits in the Interrupt Request 0 register:*

**Good coding style that avoids lost interrupt requests:**

```
ANDX IRQ0, MASK
```

## Software Interrupt Assertion

Program code can generate interrupts directly. Writing a 1 to the correct bit in the Interrupt Request register triggers an interrupt (assuming that interrupt is enabled). When the interrupt request is acknowledged by the eZ8 CPU, the bit in the Interrupt Request register is automatically cleared to 0.

**Caution:** *The following coding style used to generate software interrupts by setting bits in the Interrupt Request registers is not recommended. All incoming interrupts received between execution of the first LDX command and the final LDX command are lost.*

**Poor coding style that can result in lost interrupt requests:**

```
LDX r0, IRQ0
OR r0, MASK
LDX IRQ0, r0
```

**Caution:** *To avoid missing interrupts, use the following coding style to set bits in the Interrupt Request registers:*

**Good coding style that avoids lost interrupt requests:**

```
ORX IRQ0, MASK
```

## Watchdog Timer Interrupt Assertion

The Watchdog Timer interrupt behavior is different from interrupts generated by other sources. The Watchdog Timer continues to assert an interrupt as long as the timeout condition continues. As it operates on a different (and usually slower) clock domain than the rest of the device, the Watchdog Timer continues to assert this interrupt for many system clocks until the counter rolls over.

## IRQ2 Enable High and Low Bit Registers

Table 42 describes the priority control for IRQ2. The IRQ2 Enable High and Low Bit registers (Table 43 and Table 44) form a priority encoded enabling for interrupts in the Interrupt Request 2 register.

### Table 42. IRQ2 Enable and Priority Encoding

| IRQ2ENH[*x*] | IRQ2ENL[*x*] | Priority | Description |
|---|---|---|---|
| 0 | 0 | Disabled | Disabled |
| 0 | 1 | Level 1 | Low |
| 1 | 0 | Level 2 | Medium |
| 1 | 1 | Level 3 | High |

where *x* indicates the register bits from 0–7.

### Table 43. IRQ2 Enable High Bit Register (IRQ2ENH)

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | Reserved | | | | C3ENH | C2ENH | C1ENH | C0ENH |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| ADDR | FC7H | | | | | | | |

Reserved—Must be 0.

C3ENH—Port C3 Interrupt Request Enable High Bit
C2ENH—Port C2 Interrupt Request Enable High Bit
C1ENH—Port C1 Interrupt Request Enable High Bit
C0ENH—Port C0 Interrupt Request Enable High Bit

### Table 44. IRQ2 Enable Low Bit Register (IRQ2ENL)

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | Reserved | | | | C3ENL | C2ENL | C1ENL | C0ENL |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| ADDR | FC8H | | | | | | | |

- Set the prescale value.
- If using the Timer Output alternate function, set the initial output level (High or Low).

2. Write to the Timer High and Low Byte registers to set the starting count value (usually 0001H). This action only affects the first pass in CONTINUOUS mode. After the first timer Reload in CONTINUOUS mode, counting always begins at the reset value of 0001H.
3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
4. Enable the timer interrupt (if appropriate) and set the timer interrupt priority by writing to the relevant interrupt registers.
5. Configure the associated GPIO port pin (if using the Timer Output function) for the Timer Output alternate function.
6. Write to the Timer Control register to enable the timer and initiate counting.

In CONTINUOUS mode, the system clock always provides the timer input. The timer period is given by the following equation:

$$\text{CONTINUOUS Mode Time-Out Period (s)} = \frac{\text{Reload Value} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, use the ONE-SHOT mode equation to determine the first time-out period.

### COUNTER Mode

In COUNTER mode, the timer counts input transitions from a GPIO port pin. The timer input is taken from the GPIO Port pin Timer Input alternate function. The TPOL bit in the Timer Control Register selects whether the count occurs on the rising edge or the falling edge of the Timer Input signal. In COUNTER mode, the prescaler is disabled.

**Caution:** *The input frequency of the Timer Input signal must not exceed one-fourth the system clock frequency. Further, the high or low state of the input signal pulse must be no less than twice the system clock period. A shorter pulse may not be captured.*

Upon reaching the Reload value stored in the Timer Reload High and Low Byte registers, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer Reload.

0001H and counting resumes. The INPCAP bit in TxCTL0 register is cleared to indicate the timer interrupt is not caused by an input capture event.

Follow the steps below for configuring a timer for CAPTURE RESTART mode and initiating the count:

1. Write to the Timer Control register to:
   - Disable the timer.
   - Configure the timer for CAPTURE RESTART mode by writing the TMODE bits in the TxCTL1 register and the TMODEHI bit in TxCTL0 register.
   - Set the prescale value.
   - Set the Capture edge (rising or falling) for the Timer Input.
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
4. Clear the Timer PWM High and Low Byte registers to 0000H. This allows the software to determine if interrupts were generated by either a capture event or a reload. If the PWM High and Low Byte registers still contain 0000H after the interrupt, the interrupt was generated by a Reload.
5. Enable the timer interrupt, if appropriate, and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input capture and reload events. If appropriate, configure the timer interrupt to be generated only at the input capture event or the reload event by setting TICONFIG field of the TxCTL0 register.
6. Configure the associated GPIO port pin for the Timer Input alternate function.
7. Write to the Timer Control register to enable the timer and initiate counting.

In CAPTURE mode, the elapsed time from timer start to Capture event can be calculated using the following equation:

$$\text{Capture Elapsed Time (s)} = \frac{(\text{Capture Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

### COMPARE Mode

In COMPARE mode, the timer counts up to the 16-bit maximum Compare value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the Compare value, the timer generates an interrupt and counting continues (the timer value is not reset to 0001H). Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) upon Compare.

If the Timer reaches FFFFH, the timer rolls over to 0000H and continue counting.

**Caution:** *The 24-bit WDT Reload Value must not be set to a value less than* 000004H.

**Table 58. Watchdog Timer Reload Upper Byte Register (WDTU)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | WDTU | | | | | | | |
| RESET | 00H | | | | | | | |
| R/W | R/W* | | | | | | | |
| ADDR | FF1H | | | | | | | |
| R/W* - Read returns the current WDT count value. Write sets the appropriate Reload Value. | | | | | | | | |

WDTU—WDT Reload Upper Byte
Most-significant byte (MSB), Bits[23:16], of the 24-bit WDT reload value.

**Table 59. Watchdog Timer Reload High Byte Register (WDTH)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | WDTH | | | | | | | |
| RESET | 04H | | | | | | | |
| R/W | R/W* | | | | | | | |
| ADDR | FF2H | | | | | | | |
| R/W* - Read returns the current WDT count value. Write sets the appropriate Reload Value. | | | | | | | | |

WDTH—WDT Reload High Byte
Middle byte, Bits[15:8], of the 24-bit WDT reload value.

**Table 60. Watchdog Timer Reload Low Byte Register (WDTL)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | WDTL | | | | | | | |
| RESET | 00H | | | | | | | |
| R/W | R/W* | | | | | | | |
| ADDR | FF3H | | | | | | | |
| R/W* - Read returns the current WDT count value. Write sets the appropriate Reload Value. | | | | | | | | |

WDTL—WDT Reload Low

Least significant byte (LSB), Bits[7:0], of the 24-bit WDT reload value.

### Factory Calibration

Devices that have been factory calibrated contain 30 bytes of calibration data in the Flash option bit space. This data consists of 3 bytes for each input mode, one for offset and two for gain correction. For a list of input modes for which calibration data exists, see Zilog Calibration Data on page 161.

### User Calibration

If you have precision references available, its own external calibration can be performed using any input modes. This calibration data takes into account buffer offset and non-linearity, so it is recommended that this calibration be performed separately for each of the ADC input modes planned for use.

### Manual Offset Calibration

When uncalibrated, the ADC has significant offset (see Table 135 on page 231). Subsequently, manual offset calibration capability is built into the block. When the ADC Control Register 0 sets the input mode (ANAIN[2:0]) to MANUAL OFFSET CALIBRATION mode, the differential inputs to the ADC are shorted together by an internal switch. Reading the ADC value at this point produces 0 in an ideal system. The value actually read is the ADC offset. This value can be stored in non-volatile memory (see Non-Volatile Data Storage on page 169) and accessed by user code to compensate for the input offset error. There is no provision for manual gain calibration.

### Software Compensation Procedure Using Factory Calibration Data

The value read from the ADC high and low byte registers is uncompensated. The user mode software must apply gain and offset correction to this uncompensated value for maximum accuracy. The following equation yields the compensated value:

$$ADC_{comp} = (ADC_{uncomp} - OFFCAL) + ((ADC_{uncomp} - OFFCAL) \times GAINCAL) / 2^{16}$$

where GAINCAL is the gain calibration value, OFFCAL is the offset calibration value and $ADC_{uncomp}$ is the uncompensated value read from the ADC. All values are in two's complement format.

**Note:** *The offset compensation is performed first, followed by the gain compensation. One bit of resolution is lost because of rounding on both the offset and gain computations. As a result the ADC registers read back 13 bits: 1 sign bit, two calibration bits lost to rounding and 10 data bits.*

*Also note that in the second term, the multiplication must be performed before the division by $2^{16}$. Otherwise, the second term incorrectly evaluates to zero.*

# Low Power Operational Amplifier

## Overview

The LPO is a general-purpose low power operational amplifier. Each of the three ports of the amplifier is accessible from the package pins. The LPO contains only one pin configuration: ANA0 is the output/feedback node, ANA1 is the inverting input and ANA2 is the non-inverting input.

## Operation

To use the LPO, it must be enabled in the Power Control Register 0 (PWRCTL0). The default state of the LPO is OFF. To use the LPO, the LPO bit must be cleared, turning it ON (Power Control Register 0 (PWRCTL0) on page 35). When making normal ADC measurements on ANA0 (measurements not involving the LPO output), the LPO bit must be OFF. Turning the LPO bit ON interferes with normal ADC measurements.

**Warning:** *The LPO bit enables the amplifier even in STOP mode. If the amplifier is not required in STOP mode, disable it. Failing to perform this results in STOP mode currents higher than necessary.*

As with other ADC measurements, any pins used for analog purposes must be configured as such in the GPIO registers (see Port A–D Alternate Function Sub-Registers on page 47).

LPO output measurements are made on ANA0, as selected by the ANAIN[3:0] bits of ADC Control Register 0. It is also possible to make single-ended measurements on ANA1 and ANA2 while the amplifier is enabled, which is often useful for determining offset conditions. Differential measurements between ANA0 and ANA2 may be useful for noise cancellation purposes.

If the LPO output is routed to the ADC, then the BUFFMODE[2:0] bits of ADC Control/Status Register 1 must also be configured for unity-gain buffered operation. Sampling the LPO in an unbuffered mode is not recommended.

When either input is overdriven, the amplifier output saturates at the positive or negative supply voltage. No instability results.

## Option Bit Types

### User Option Bits

The user option bits are contained in the first two bytes of program memory. User access to these bits has been provided because these locations contain application-specific device configurations. The information contained here is lost when page 0 of the program memory is erased.

### Trim Option Bits

The trim option bits are contained in the information page of the Flash memory. These bits are factory programmed values required to optimize the operation of onboard analog circuitry and cannot be permanently altered. Program Memory may be erased without endangering these values. It is possible to alter working values of these bits by accessing the Trim Bit Address and Data Registers, but these working values are lost after a power loss or any other reset event.

There are 32 bytes of trim data. To modify one of these values the user code must first write a value between 00H and 1FH into the Trim Bit Address Register. The next write to the Trim Bit Data register changes the working value of the target trim data byte.

Reading the trim data requires the user code to write a value between 00H and 1FH into the Trim Bit Address Register. The next read from the Trim Bit Data register returns the working value of the target trim data byte.

**Note:** *The trim address range is from information address 20-3F only. The remainder of the information page is not accessible through the trim bit address and data registers.*

### Calibration Option Bits

The calibration option bits are also contained in the information page. These bits are factory programmed values intended for use in software correcting the device's analog performance. To read these values, the user code must employ the LDC instruction to access the information area of the address space as defined in See Flash Information Area on page 17.

### Serialization Bits

As an optional feature, Zilog® is able to provide factory-programmed serialization. For serialized products, the individual devices are programmed with unique serial numbers. These serial numbers are binary values, four bytes in length. The numbers increase in size with each device, but gaps in the serial sequence may exist.

These serial numbers are stored in the Flash information page (see Reading the Flash Information Page on page 155 and Serialization Data on page 165 for more details) and are unaffected by mass erasure of the device's Flash memory.

High. Because of the open-drain nature of the DBG pin, the host can send a Serial Break to the OCD even if the OCD is transmitting a character.

## OCD Unlock Sequence (8-Pin Devices Only)

Because of pin-sharing on the 8-pin device, an unlock sequence must be performed to access the DBG pin. If this sequence is not completed during a system reset, then the PA0/DBG pin functions only as a GPIO pin.

The following sequence unlocks the DBG pin:

1. Hold PA2/$\overline{\text{RESET}}$ Low.
2. Wait 5ms for the internal reset sequence to complete.
3. Send the following bytes serially to the debug pin:

```
DBG ← 80H (autobaud)
DBG ← EBH
DBG ← 5AH
DBG ← 70H
DBG ← CDH (32-bit unlock key)
```

4. Release PA2/$\overline{\text{RESET}}$. The PA0/DBG pin is now identical in function to that of the DBG pin on the 20-/28-pin device. To enter DEBUG mode, re-autobaud and write 80H to the OCD control register (see On-Chip Debugger Commands on page 179).

**Caution:** *Between Step 3 and Step 4, there is an interval during which the 8-pin device is neither in RESET nor DEBUG mode. If a device has been erased or has not yet been programmed, all program memory bytes contain FFH. The CPU interprets this as an illegal instruction, so some irregular behavior can occur before entering DEBUG mode, and the register values after entering DEBUG mode differs from their specified reset values. However, none of these irregularities prevent programming the Flash memory. Before beginning system debug, it is recommended that some legal code be programmed into the 8-pin device, and that a RESET occurs.*

## Breakpoints

Execution Breakpoints are generated using the BRK instruction (opcode 00H). When the eZ8 CPU decodes a BRK instruction, it signals the On-Chip Debugger. If Breakpoints are enabled, the OCD enters DEBUG mode and idles the eZ8 CPU. If Breakpoints are not enabled, the OCD ignores the BRK signal and the BRK instruction operates as an NOP instruction.

# eZ8 CPU Instruction Set

## Assembly Language Programming Introduction

The eZ8 CPU assembly language provides a means for writing an application program without concern for actual memory addresses or machine instruction formats. A program written in assembly language is called a source program. Assembly language allows the use of symbolic addresses to identify memory locations. It also allows mnemonic codes (opcodes and operands) to represent the instructions themselves. The opcodes identify the instruction while the operands represent memory locations, registers, or immediate data values.

Each assembly language program consists of a series of symbolic commands called statements. Each statement can contain labels, operations, operands and comments.

Labels can be assigned to a particular instruction step in a source program. The label identifies that step in the program as an entry point for use by other instructions.

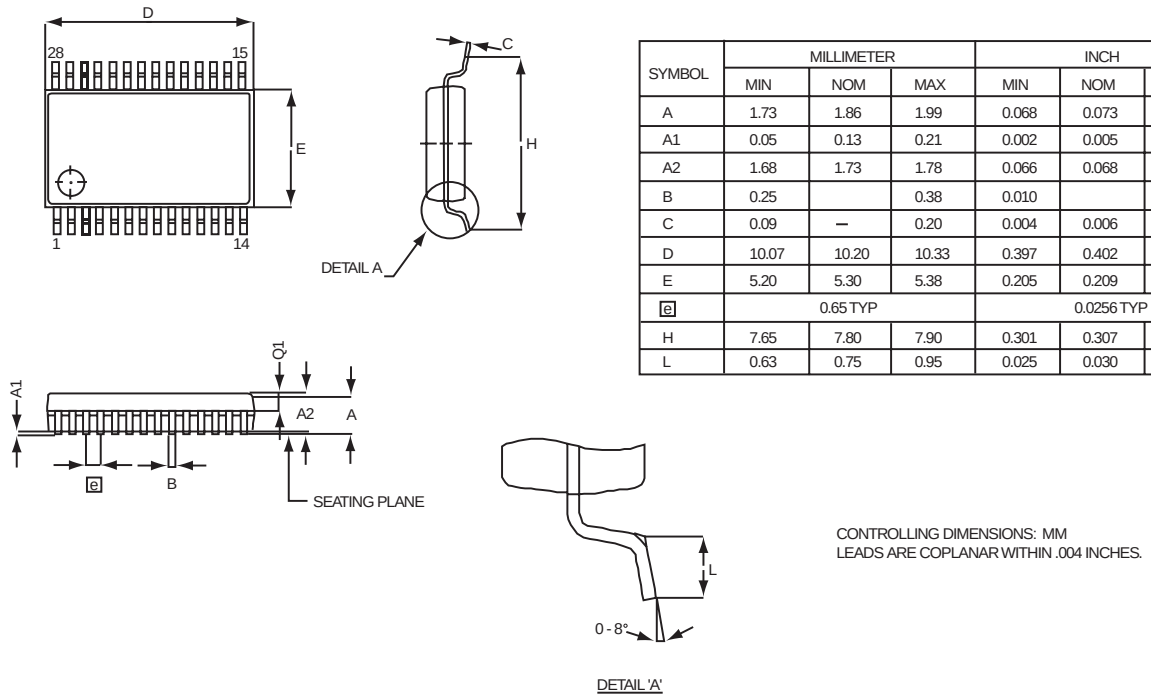
The assembly language also includes assembler directives that supplement the machine instruction. The assembler directives, or pseudo-ops, are not translated into a machine instruction. Rather, the pseudo-ops are interpreted as directives that control or assist the assembly process.

The source program is processed (assembled) by the assembler to obtain a machine language program called the object code. The object code is executed by the eZ8 CPU. An example segment of an assembly language program is detailed in the following example.

### Assembly Language Source Program Example

```
JP START          ; Everything after the semicolon is a comment.
START:            ; A label called 'START'. The first instruction (JP START) in this
                  ; example causes program execution to jump to the point within the
                  ; program where the START label occurs.
LD R4, R7         ; A Load (LD) instruction with two operands. The first operand,
                  ; Working Register R4, is the destination. The second operand,
                  ; Working Register R7, is the source. The contents of R7 is
                  ; written into R4.
LD 234H, #%01     ; Another Load (LD) instruction with two operands.
                  ; The first operand, Extended Mode Register Address 234H,
                  ; identifies the destination. The second operand, Immediate Data
                  ; value 01H, is the source. The value 01H is written into the
                  ; Register at address 234H.
```

Figure 47 displays the 28-pin Small Shrink Outline Package (SSOP) available for the Z8 Encore! XP F082A Series devices.




| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.73 | 1.86 | 1.99 | 0.068 | 0.073 | 0.078 |
| A1 | 0.05 | 0.13 | 0.21 | 0.002 | 0.005 | 0.008 |
| A2 | 1.68 | 1.73 | 1.78 | 0.066 | 0.068 | 0.070 |
| B | 0.25 | | 0.38 | 0.010 | | 0.015 |
| C | 0.09 | – | 0.20 | 0.004 | 0.006 | 0.008 |
| D | 10.07 | 10.20 | 10.33 | 0.397 | 0.402 | 0.407 |
| E | 5.20 | 5.30 | 5.38 | 0.205 | 0.209 | 0.212 |
| e | 0.65 TYP | | | 0.0256 TYP | | |
| H | 7.65 | 7.80 | 7.90 | 0.301 | 0.307 | 0.311 |
| L | 0.63 | 0.75 | 0.95 | 0.025 | 0.030 | 0.037 |

**Figure 47. 28-Pin Small Shrink Outline Package (SSOP)**

| Part Number | Flash | RAM | NVDS | I/O Lines | Interrupts | 16-Bit Timers w/PWM | 10-Bit A/D Channels | UART with IrDA | Comparator | Temperature Sensor | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Z8 Encore! XP® F082A Series Development Kit** | | | | | | | | | | | |
| Z8F08A28100KITG | | | | | | | | | | | Z8 Encore! XP F082A Series 28-Pin Development Kit |
| Z8F04A28100KITG | | | | | | | | | | | Z8 Encore! XP F042A Series 28-Pin Development Kit |
| Z8F04A08100KITG | | | | | | | | | | | Z8 Encore! XP F042A Series 8-Pin Development Kit |
| ZUSBSC00100ZACG | | | | | | | | | | | USB Smart Cable Accessory Kit |
| ZUSBOPTSC01ZACG | | | | | | | | | | | USB Opto-Isolated Smart Cable Accessory Kit |
| ZENETSC0100ZACG | | | | | | | | | | | Ethernet Smart Cable Accessory Kit |

# Index

## Symbols



## Numerics



## A



## B



## C