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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	16 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f011ash020ec00tr



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As used herein

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Overview

Zilog's Z8 Encore![®] MCU family of products are the first in a line of Zilog[®] microcontroller products based upon the 8-bit eZ8 CPU. Zilog's Z8 Encore! XP[®] F082A Series products expand upon Zilog's extensive line of 8-bit microcontrollers. The Flash in-circuit programming capability allows for faster development time and program changes in the field. The new eZ8 CPU is upward compatible with existing Z8[®] instructions. The rich peripheral set of the Z8 Encore! XP F082A Series makes it suitable for a variety of applications including motor control, security systems, home appliances, personal electronic devices, and sensors.

Features

The key features of Z8 Encore! XP F082A Series products include:

- 20 MHz eZ8 CPU
- 1 KB, 2 KB, 4 KB, or 8 KB Flash memory with in-circuit programming capability
- 256 B, 512 B, or 1 KB register RAM
- Up to 128 B non-volatile data storage (NVDS)
- Internal precision oscillator trimmed to $\pm 1\%$ accuracy
- External crystal oscillator, operating up to 20 MHz
- Optional 8-channel, 10-bit analog-to-digital converter (ADC)
- Optional on-chip temperature sensor
- On-chip analog comparator
- Optional on-chip low-power operational amplifier (LPO)
- Full-duplex UART
- The UART baud rate generator (BRG) can be configured and used as a basic 16-bit timer
- Infrared Data Association (IrDA)-compliant infrared encoder/decoders, integrated with UART
- Two enhanced 16-bit timers with capture, compare, and PWM capability
- Watchdog Timer (WDT) with dedicated internal RC oscillator
- Up to 20 vectored interrupts
- 6 to 25 I/O pins depending upon package

Table 2. Signal Descriptions (Continued)

Signal Mnemonic	I/O	Description
Power Supply		
V _{DD}	I	Digital Power Supply.
AV _{DD}	I	Analog Power Supply.
V _{SS}	I	Digital Ground.
AV _{SS}	I	Analog Ground.
Note: The AV _{DD} and AV _{SS} signals are available only in 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.		

Pin Characteristics

Table 3 describes the characteristics for each pin available on the Z8 Encore! XP F082A Series 20- and 28-pin devices. Data in Table 3 is sorted alphabetically by the pin symbol mnemonic.

Table 4 on page 14 provides detailed information about the characteristics for each pin available on the Z8 Encore! XP F082A Series 8-pin devices.

► **Note:** All six I/O pins on the 8-pin packages are 5 V-tolerant (unless the pull-up devices are enabled). The column in Table 3 below describes 5 V-tolerance for the 20- and 28-pin packages only.

Table 3. Pin Characteristics (20- and 28-pin Devices)

Symbol Mnemonic	Direction	Reset Direction	Active Low or Active High	Tristate Output	Internal Pull-up or Pull-down	Schmitt-Trigger Input	Open Drain Output	5 V Tolerance
AVDD	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
AVSS	N/A	N/A	N/A	N/A	N/A	N/A	N/A	NA
DBG	I/O	I	N/A	Yes	Yes	Yes	Yes	No
PA[7:0]	I/O	I	N/A	Yes	Programmable Pull-up	Yes	Yes, Programmable	PA[7:2] unless pullups enabled
PB[7:0]	I/O	I	N/A	Yes	Programmable Pull-up	Yes	Yes, Programmable	PB[7:6] unless pullups enabled

vector address. Following Stop Mode Recovery, the STOP bit in the Reset Status (RSTSTAT) Register is set to 1. Table 10 lists the Stop Mode Recovery sources and resulting actions. The text following provides more detailed information about each of the Stop Mode Recovery sources.

Table 10. Stop Mode Recovery Sources and Resulting Action

Operating Mode	Stop Mode Recovery Source	Action
STOP mode	Watchdog Timer time-out when configured for Reset	Stop Mode Recovery
	Watchdog Timer time-out when configured for interrupt	Stop Mode Recovery followed by interrupt (if interrupts are enabled)
	Data transition on any GPIO Port pin enabled as a Stop Mode Recovery source	Stop Mode Recovery
	Assertion of external $\overline{\text{RESET}}$ Pin	System Reset
	Debug Pin driven Low	System Reset

Stop Mode Recovery Using Watchdog Timer Time-Out

If the Watchdog Timer times out during STOP mode, the device undergoes a Stop Mode Recovery sequence. In the Reset Status (RSTSTAT) register, the WDT and STOP bits are set to 1. If the Watchdog Timer is configured to generate an interrupt upon time-out and the Z8 Encore! XP F082A Series device is configured to respond to interrupts, the eZ8 CPU services the Watchdog Timer interrupt request following the normal Stop Mode Recovery sequence.

Stop Mode Recovery Using a GPIO Port Pin Transition

Each of the GPIO Port pins may be configured as a Stop Mode Recovery input source. On any GPIO pin enabled as a Stop Mode Recovery source, a change in the input pin value (from High to Low or from Low to High) initiates Stop Mode Recovery.

► **Note:** *The SMR pulses shorter than specified does not trigger a recovery (see Table 131 on page 229). When this happens, the STOP bit in the Reset Status (RSTSTAT) register is set to 1.*



Caution: *In STOP mode, the GPIO Port Input Data registers (PxIN) are disabled. The Port Input Data registers record the Port transition only if the signal stays on the Port pin through the end of the Stop Mode Recovery delay. As a result, short pulses on the Port pin can*

General-Purpose Input/Output

The Z8 Encore! XP[®] F082A Series products support a maximum of 25 port pins (Ports A–D) for general-purpose input/output (GPIO) operations. Each port contains control and data registers. The GPIO control registers determine data direction, open-drain, output drive current, programmable pull-ups, Stop Mode Recovery functionality, and alternate pin functions. Each port pin is individually programmable. In addition, the Port C pins are capable of direct LED drive at programmable drive strengths.

GPIO Port Availability By Device

[Table 13](#) lists the port pins available with each device and package type.

Table 13. Port Availability by Device and Package Type

Devices	Package	ADC	Port A	Port B	Port C	Port D	Total I/O
Z8F082ASB, Z8F082APB, Z8F082AQB Z8F042ASB, Z8F042APB, Z8F042AQB Z8F022ASB, Z8F022APB, Z8F022AQB Z8F012ASB, Z8F012APB, Z8F012AQB	8-pin	Yes	[5:0]	No	No	No	6
Z8F081ASB, Z8F081APB, Z8F081AQB Z8F041ASB, Z8F041APB, Z8F041AQB Z8F021ASB, Z8F021APB, Z8F021AQB Z8F011ASB, Z8F011APB, Z8F011AQB	8-pin	No	[5:0]	No	No	No	6
Z8F082APH, Z8F082AHH, Z8F082ASH Z8F042APH, Z8F042AHH, Z8F042ASH Z8F022APH, Z8F022AHH, Z8F022ASH Z8F012APH, Z8F012AHH, Z8F012ASH	20-pin	Yes	[7:0]	[3:0]	[3:0]	[0]	17
Z8F081APH, Z8F081AHH, Z8F081ASH Z8F041APH, Z8F041AHH, Z8F041ASH Z8F021APH, Z8F021AHH, Z8F021ASH Z8F011APH, Z8F011AHH, Z8F011ASH	20-pin	No	[7:0]	[3:0]	[3:0]	[0]	17
Z8F082APJ, Z8F082ASJ, Z8F082AHJ Z8F042APJ, Z8F042ASJ, Z8F042AHJ Z8F022APJ, Z8F022ASJ, Z8F022AHJ Z8F012APJ, Z8F012ASJ, Z8F012AHJ	28-pin	Yes	[7:0]	[5:0]	[7:0]	[0]	23
Z8F081APJ, Z8F081ASJ, Z8F081AHJ Z8F041APJ, Z8F041ASJ, Z8F041AHJ Z8F021APJ, Z8F021ASJ, Z8F021AHJ Z8F011APJ, Z8F011ASJ, Z8F011AHJ	28-pin	No	[7:0]	[7:0]	[7:0]	[0]	25

- Set the prescale value.
 - If using the Timer Output alternate function, set the initial output level (High or Low).
2. Write to the Timer High and Low Byte registers to set the starting count value (usually 0001H). This action only affects the first pass in CONTINUOUS mode. After the first timer Reload in CONTINUOUS mode, counting always begins at the reset value of 0001H.
 3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
 4. Enable the timer interrupt (if appropriate) and set the timer interrupt priority by writing to the relevant interrupt registers.
 5. Configure the associated GPIO port pin (if using the Timer Output function) for the Timer Output alternate function.
 6. Write to the Timer Control register to enable the timer and initiate counting.

In CONTINUOUS mode, the system clock always provides the timer input. The timer period is given by the following equation:

$$\text{CONTINUOUS Mode Time-Out Period (s)} = \frac{\text{Reload Value} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, use the ONE-SHOT mode equation to determine the first time-out period.

COUNTER Mode

In COUNTER mode, the timer counts input transitions from a GPIO port pin. The timer input is taken from the GPIO Port pin Timer Input alternate function. The TPOL bit in the Timer Control Register selects whether the count occurs on the rising edge or the falling edge of the Timer Input signal. In COUNTER mode, the prescaler is disabled.



Caution: *The input frequency of the Timer Input signal must not exceed one-fourth the system clock frequency. Further, the high or low state of the input signal pulse must be no less than twice the system clock period. A shorter pulse may not be captured.*

Upon reaching the Reload value stored in the Timer Reload High and Low Byte registers, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer Reload.

Timer Control Register Definitions

Timer 0–1 Control Registers

Time 0–1 Control Register 0

The Timer Control Register 0 (TxCTL0) and Timer Control Register 1 (TxCTL1) determine the timer operating mode (Table 48). It also includes a programmable PWM dead-band delay, two bits to configure timer interrupt definition, and a status bit to identify if the most recent timer interrupt is caused by an input capture event.

Table 48. Timer 0–1 Control Register 0 (TxCTL0)

BITS	7	6	5	4	3	2	1	0
FIELD	TMODEHI	TICONFIG		Reserved	PWMD			INPCAP
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
ADDR	F06H, F0EH							

TMODEHI—Timer Mode High Bit

This bit along with the TMODE field in TxCTL1 register determines the operating mode of the timer. This is the most significant bit of the Timer mode selection value. See the TxCTL1 register description for details of the full timer mode decoding.

TICONFIG—Timer Interrupt Configuration

This field configures timer interrupt definition.

0x = Timer Interrupt occurs on all defined Reload, Compare and Input Events

10 = Timer Interrupt only on defined Input Capture/Deassertion Events

11 = Timer Interrupt only on defined Reload/Compare Events

Reserved—Must be 0.

PWMD—PWM Delay value

This field is a programmable delay to control the number of system clock cycles delay before the Timer Output and the Timer Output Complement are forced to their active state.

000 = No delay

001 = 2 cycles delay

010 = 4 cycles delay

011 = 8 cycles delay

100 = 16 cycles delay

101 = 32 cycles delay

Universal Asynchronous Receiver/Transmitter

The universal asynchronous receiver/transmitter (UART) is a full-duplex communication channel capable of handling asynchronous data transfers. The UART uses a single 8-bit data mode with selectable parity. Features of the UART include:

- 8-bit asynchronous data transfer.
- Selectable even- and odd-parity generation and checking.
- Option of one or two STOP bits.
- Separate transmit and receive interrupts.
- Framing, parity, overrun and break detection.
- Separate transmit and receive enables.
- 16-bit baud rate generator (BRG).
- Selectable MULTIPROCESSOR (9-bit) mode with three configurable interrupt schemes.
- Baud rate generator (BRG) can be configured and used as a basic 16-bit timer.
- Driver enable (DE) output for external bus transceivers.

Architecture

The UART consists of three primary functional blocks: transmitter, receiver, and baud rate generator. The UART's transmitter and receiver function independently, but employ the same baud rate and data format. [Figure 10](#) on page 98 displays the UART architecture.

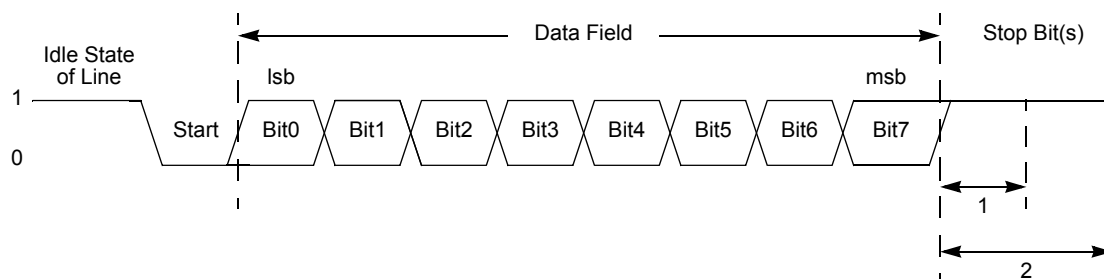


Figure 11. UART Asynchronous Data Format without Parity

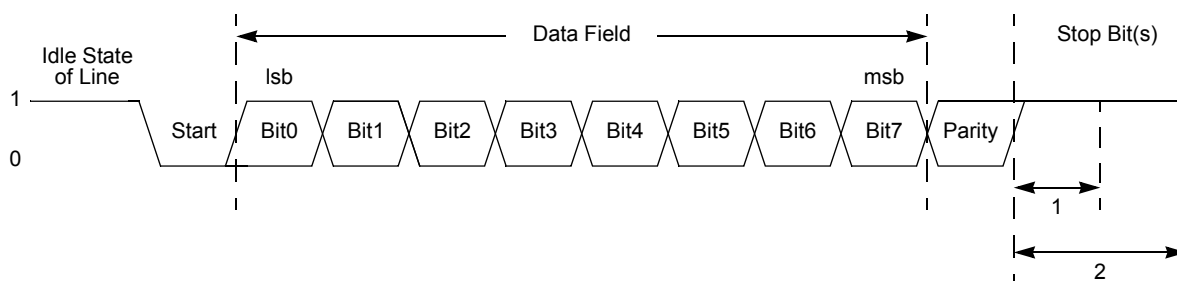


Figure 12. UART Asynchronous Data Format with Parity

Transmitting Data using the Polled Method

Follow the steps below to transmit data using the polled method of operation:

1. Write to the UART Baud Rate High and Low Byte registers to set the required baud rate.
2. Enable the UART pin functions by configuring the associated GPIO Port pins for alternate function operation.
3. Write to the UART Control 1 register, if MULTIPROCESSOR mode is appropriate, to enable MULTIPROCESSOR (9-bit) mode functions.
4. Set the Multiprocessor Mode Select (MPEN) bit to enable MULTIPROCESSOR mode.
5. Write to the UART Control 0 register to:
 - Set the transmit enable bit (TEN) to enable the UART for data transmission.
 - Set the parity enable bit (PEN), if parity is appropriate and MULTIPROCESSOR mode is not enabled, and select either even or odd parity (PSEL).
 - Set or clear the CTSE bit to enable or disable control from the remote receiver using the $\overline{\text{CTS}}$ pin.

Compensation Steps:

1. Correct for Offset

ADC MSB	ADC LSB
---------	---------

-

Offset MSB	Offset LSB
------------	------------

=

#1 MSB	#1 LSB
--------	--------

2. Take absolute value of the offset corrected ADC value *if negative*—the gain correction factor is computed assuming positive numbers, with sign restoration afterward.

#2 MSB	#2 LSB
--------	--------

Also take absolute value of the gain correction word *if negative*.

AGain MSB	AGain LSB
-----------	-----------

3. Multiply by Gain Correction Word. If in DIFFERENTIAL mode, there are two gain correction values: one for positive ADC values, another for negative ADC values. Based on the sign of #2, use the appropriate Gain Correction Word.

#2 MSB	#2 LSB
--------	--------

*

AGain MSB	AGain LSB
-----------	-----------

=

#3	#3	#3	#3
----	----	----	----

4. Round the result and discard the least significant two bytes (this is equivalent to dividing by 2^{16}).

#3	#3	#3	#3
----	----	----	----

-

0x00	0x00	0x80	0x00
------	------	------	------

=

#4 MSB	#4 LSB
--------	--------

5. Determine sign of the gain correction factor using the sign bits from [Step 2](#). If the offset corrected ADC value AND the gain correction word have the same sign, then the factor is positive and is left unchanged. If they have differing signs, then the factor is negative and must be multiplied by -1.

Randomized Lot Identification Bits

As an optional feature, Zilog is able to provide a factory-programmed random lot identifier. With this feature, all devices in a given production lot are programmed with the same random number. This random number is uniquely regenerated for each successive production lot and is not likely to be repeated.

The randomized lot identifier is a 32 byte binary value, stored in the Flash information page (see [Reading the Flash Information Page](#) on page 155 and [Randomized Lot Identifier](#) on page 166 for more details) and is unaffected by mass erasure of the device's Flash memory.

Reading the Flash Information Page

The following code example shows how to read data from the Flash information area.

```
; get value at info address 60 (FE60h)

ldx FPS, #%80 ; enable access to flash info page

ld R0, #%FE
ld R1, #%60
ldc R2, @RR0 ; R2 now contains the calibration value
```

Flash Option Bit Control Register Definitions

Trim Bit Address Register

The Trim Bit Address (TRMADR) register contains the target address for an access to the trim option bits ([Table 84](#)).

Table 84. Trim Bit Address Register (TRMADR)

BITS	7	6	5	4	3	2	1	0
FIELD	TRMADR - Trim Bit Address (00H to 1FH)							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FF6H							

Trim Bit Data Register

The Trim Bid Data (TRMDR) register contains the read or write data for access to the trim option bits (Table 85).

Table 85. Trim Bit Data Register (TRMDR)

BITS	7	6	5	4	3	2	1	0
FIELD	TRMDR - Trim Bit Data							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FF7H							

Flash Option Bit Address Space

The first two bytes of Flash program memory at addresses 0000H and 0001H are reserved for the user-programmable Flash option bits.

Flash Program Memory Address 0000H

Table 86. Flash Option Bits at Program Memory Address 0000H

BITS	7	6	5	4	3	2	1	0
FIELD	WDT_RES	WDT_AO	OSC_SEL[1:0]		VBO_AO	FRP	Reserved	FWP
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	Program Memory 0000H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

WDT_RES—Watchdog Timer Reset

0 = Watchdog Timer time-out generates an interrupt request. Interrupts must be globally enabled for the eZ8 CPU to acknowledge the interrupt request.

1 = Watchdog Timer time-out causes a system reset. This setting is the default for unprogrammed (erased) Flash.

WDT_AO—Watchdog Timer Always On

0 = Watchdog Timer is automatically enabled upon application of system power. Watchdog Timer can not be disabled.

Table 94. ADC Calibration Data Location (Continued)

Info Page Address	Memory Address	Compensation Usage	ADC Mode	Reference Type
34	FE34	Negative Gain High Byte	Differential Unbuffered	External 2.0 V
35	FE35	Negative Gain Low Byte	Differential Unbuffered	External 2.0 V
78	FE78	Offset	Differential 1x Buffered	Internal 2.0 V
18	FE18	Positive Gain High Byte	Differential 1x Buffered	Internal 2.0 V
19	FE19	Positive Gain Low Byte	Differential 1x Buffered	Internal 2.0 V
36	FE36	Negative Gain High Byte	Differential 1x Buffered	Internal 2.0 V
37	FE37	Negative Gain Low Byte	Differential 1x Buffered	Internal 2.0 V
7B	FE7B	Offset	Differential 1x Buffered	External 2.0 V
1A	FE1A	Positive Gain High Byte	Differential 1x Buffered	External 2.0 V
1B	FE1B	Positive Gain Low Byte	Differential 1x Buffered	External 2.0 V
38	FE38	Negative Gain High Byte	Differential 1x Buffered	External 2.0 V
39	FE39	Negative Gain Low Byte	Differential 1x Buffered	External 2.0 V

Table 115. Additional Symbols

Symbol	Definition
dst	Destination Operand
src	Source Operand
@	Indirect Address Prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flags Register
RP	Register Pointer
#	Immediate Operand Prefix
B	Binary Number Suffix
%	Hexadecimal Number Prefix
H	Hexadecimal Number Suffix

Assignment of a value is indicated by an arrow. For example,

$$\text{dst} \leftarrow \text{dst} + \text{src}$$

indicates the source data is added to the destination data and the result is stored in the destination location.

eZ8 CPU Instruction Classes

eZ8 CPU instructions can be divided functionally into the following groups:

- Arithmetic
- Bit Manipulation
- Block Transfer
- CPU Control
- Load
- Logical
- Program Control
- Rotate and Shift

Table 117. Bit Manipulation Instructions

Mnemonic	Operands	Instruction
BCLR	bit, dst	Bit Clear
BIT	p, bit, dst	Bit Set or Clear
BSET	bit, dst	Bit Set
BSWAP	dst	Bit Swap
CCF	—	Complement Carry Flag
RCF	—	Reset Carry Flag
SCF	—	Set Carry Flag
TCM	dst, src	Test Complement Under Mask
TCMX	dst, src	Test Complement Under Mask using Extended Addressing
TM	dst, src	Test Under Mask
TMX	dst, src	Test Under Mask using Extended Addressing

Table 118. Block Transfer Instructions

Mnemonic	Operands	Instruction
LDCI	dst, src	Load Constant to/from Program Memory and Auto-Increment Addresses
LDEI	dst, src	Load External Data to/from Data Memory and Auto-Increment Addresses

Table 119. CPU Control Instructions

Mnemonic	Operands	Instruction
ATM	—	Atomic Execution
CCF	—	Complement Carry Flag
DI	—	Disable Interrupts
EI	—	Enable Interrupts
HALT	—	Halt Mode
NOP	—	No Operation
RCF	—	Reset Carry Flag



Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP[®] F082A Series with 4 KB Flash											
Standard Temperature: 0 °C to 70 °C											
Z8F041APB020SC	4 KB	1 KB	128 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F041AQB020SC	4 KB	1 KB	128 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F041ASB020SC	4 KB	1 KB	128 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F041ASH020SC	4 KB	1 KB	128 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F041AHH020SC	4 KB	1 KB	128 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F041APH020SC	4 KB	1 KB	128 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F041ASJ020SC	4 KB	1 KB	128 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F041AHJ020SC	4 KB	1 KB	128 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F041APJ020SC	4 KB	1 KB	128 B	25	19	2	0	1	1	0	PDIP 28-pin package
Extended Temperature: -40 °C to 105 °C											
Z8F041APB020EC	4 KB	1 KB	128 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F041AQB020EC	4 KB	1 KB	128 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F041ASB020EC	4 KB	1 KB	128 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F041ASH020EC	4 KB	1 KB	128 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F041AHH020EC	4 KB	1 KB	128 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F041APH020EC	4 KB	1 KB	128 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F041ASJ020EC	4 KB	1 KB	128 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F041AHJ020EC	4 KB	1 KB	128 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F041APJ020EC	4 KB	1 KB	128 B	25	19	2	0	1	1	0	PDIP 28-pin package
Replace C with G for Lead-Free Packaging											

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP® F082A Series Development Kit											
Z8F08A28100KITG											Z8 Encore! XP F082A Series 28-Pin Development Kit
Z8F04A28100KITG											Z8 Encore! XP F042A Series 28-Pin Development Kit
Z8F04A08100KITG											Z8 Encore! XP F042A Series 8-Pin Development Kit
ZUSBSC00100ZACG											USB Smart Cable Accessory Kit
ZUSBOPTSC01ZACG											USB Opto-Isolated Smart Cable Accessory Kit
ZENETSC0100ZACG											Ethernet Smart Cable Accessory Kit

L

- LD 205
- LDC 205
- LDCI 204, 205
- LDE 205
- LDEI 204, 205
- LDX 205
- LEA 205
- load 205
- load constant 204
- load constant to/from program memory 205
- load constant with auto-increment addresses 205
- load effective address 205
- load external data 205
- load external data to/from data memory and auto-increment addresses 204
- load external to/from data memory and auto-increment addresses 205
- load using extended addressing 205
- logical AND 205
- logical AND/extended addressing 205
- logical exclusive OR 206
- logical exclusive OR/extended addressing 206
- logical instructions 205
- logical OR 205
- logical OR/extended addressing 206
- low power modes 33

M

- master interrupt enable 57
- memory
 - data 17
 - program 15
- mode
 - CAPTURE 85, 86
 - CAPTURE/COMPARE 85
 - CONTINUOUS 84
 - COUNTER 84
 - GATED 85
 - ONE-SHOT 84
 - PWM 85
- modes 85

- MULT 203
- multiply 203
- multiprocessor mode, UART 103

N

- NOP (no operation) 204
- notation
 - b 201
 - cc 201
 - DA 201
 - ER 201
 - IM 201
 - IR 201
 - lr 201
 - IRR 201
 - lrr 201
 - p 201
 - R 201
 - r 201
 - RA 201
 - RR 201
 - rr 201
 - vector 201
 - X 201
- notational shorthand 201

O

- OCD
 - architecture 173
 - auto-baud detector/generator 176
 - baud rate limits 177
 - block diagram 173
 - breakpoints 178
 - commands 179
 - control register 184
 - data format 176
 - DBG pin to RS-232 Interface 174
 - debug mode 175
 - debugger break 206
 - interface 174
 - serial errors 177
 - status register 185