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#### Zilog - Z8F012AHH020EC00TR Datasheet



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#### Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	16 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f012ahh020ec00tr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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#### Table 2. Signal Descriptions (Continued)

Signal Mnemonic	I/O	Description
Power Supply		
V <sub>DD</sub>	I	Digital Power Supply.
AV <sub>DD</sub>	Ι	Analog Power Supply.
V <sub>SS</sub>	I	Digital Ground.
AV <sub>SS</sub>	I	Analog Ground.
Note: The AVpp and A	AVec siar	nals are available only in 28-nin packages with ADC. They are replaced by PB6 and

**Note:** The AV<sub>DD</sub> and AV<sub>SS</sub> signals are available only in 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.

# **Pin Characteristics**

Table 3 describes the characteristics for each pin available on the Z8 Encore! XP F082A Series 20- and 28-pin devices. Data in Table 3 is sorted alphabetically by the pin symbol mnemonic.

Table 4 on page 14 provides detailed information about the characteristics for each pin available on the Z8 Encore! XP F082A Series 8-pin devices.

Note:

All six I/O pins on the 8-pin packages are 5 V-tolerant (unless the pull-up devices are enabled). The column in Table 3 below describes 5 V-tolerance for the 20- and 28-pin packages only.

#### Table 3. Pin Characteristics (20- and 28-pin Devices)

Symbol Mnemonic	Direction	Reset Direction	Active Low or Active High	Tristate Output	Internal Pull- up or Pull-down	Schmitt- Trigger Input	Open Drain Output	5 V Tolerance
AVDD	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
AVSS	N/A	N/A	N/A	N/A	N/A	N/A	N/A	NA
DBG	I/O	I	N/A	Yes	Yes	Yes	Yes	No
PA[7:0]	I/O	I	N/A	Yes	Programmable Pull-up	Yes	Yes, Programmable	PA[7:2] unless pullups enabled
PB[7:0]	I/O	I	N/A	Yes	Programmable Pull-up	Yes	Yes, Programmable	PB[7:6] unless pullups enabled



# **Address Space**

The eZ8 CPU can access the following three distinct address spaces:

- 1. The Register File contains addresses for the general-purpose registers and the eZ8 CPU, peripheral, and general-purpose I/O port control registers.
- 2. The Program Memory contains addresses for all memory locations having executable code and/or data.
- 3. The Data Memory contains addresses for all memory locations that contain data only.

These three address spaces are covered briefly in the following subsections. For more information on eZ8 CPU and its address space, refer to eZ8 CPU Core User Manual (UM0128) available for download at www.zilog.com.

# **Register File**

The Register File address space in the Z8 Encore!<sup>®</sup> MCU is 4 KB (4096 bytes). The Register File is composed of two sections: control registers and general-purpose registers. When instructions are executed, registers defined as sources are read, and registers defined as destinations are written. The architecture of the eZ8 CPU allows all general-purpose registers to function as accumulators, address pointers, index registers, stack areas, or scratch pad memory.

The upper 256 bytes of the 4 KB Register File address space are reserved for control of the eZ8 CPU, the on-chip peripherals, and the I/O ports. These registers are located at addresses from F00H to FFFH. Some of the addresses within the 256 B control register section are reserved (unavailable). Reading from a reserved Register File address returns an undefined value. Writing to reserved Register File addresses is not recommended and can produce unpredictable results.

The on-chip RAM always begins at address 000H in the Register File address space. The Z8 Encore! XP<sup>®</sup> F082A Series devices contain 256 B to 1 KB of on-chip RAM. Reading from Register File addresses outside the available RAM addresses (and not within the control register address space) returns an undefined value. Writing to these Register File addresses produces no effect.

# **Program Memory**

The eZ8 CPU supports 64 KB of Program Memory address space. The Z8 Encore! XP F082A Series devices contain 1 KB to 8 KB of on-chip Flash memory in the Program Memory address space, depending on the device. Reading from Program Memory

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# Reset, Stop Mode Recovery, and Low Voltage Detection

The Reset Controller within the Z8 Encore! XP<sup>®</sup> F082A Series controls Reset and Stop Mode Recovery operation and provides indication of low supply voltage conditions. In typical operation, the following events cause a Reset:

- Power-On Reset (POR)
- Voltage Brownout (VBO)
- Watchdog Timer time-out (when configured by the WDT\_RES Flash Option Bit to initiate a reset)
- External RESET pin assertion (when the alternate RESET function is enabled by the GPIO register)
- On-chip debugger initiated Reset (OCDCTL[0] set to 1)

When the device is in STOP mode, a Stop Mode Recovery is initiated by either of the following:

- Watchdog Timer time-out
- GPIO Port input pin transition on an enabled Stop Mode Recovery source

The low voltage detection circuitry on the device (available on the 8-pin product versions only) performs the following functions:

- Generates the VBO reset when the supply voltage drops below a minimum safe level.
- Generates an interrupt when the supply voltage drops below a user-defined level (8-pin devices only).

# **Reset Types**

The Z8 Encore! XP F082A Series provides several different types of Reset operation. Stop Mode Recovery is considered as a form of Reset. Table 8 lists the types of Reset and their operating characteristics. The System Reset is longer if the external crystal oscillator is enabled by the Flash option bits, allowing additional time for oscillator start-up.

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initiate Stop Mode Recovery without being written to the Port Input Data register or without initiating an interrupt (if enabled for that pin).

# Stop Mode Recovery Using the External RESET Pin

When the Z8 Encore! XP F082A Series device is in STOP mode and the external  $\overline{\text{RESET}}$  pin is driven Low, a system reset occurs. Because of a glitch filter operating on the  $\overline{\text{RESET}}$  pin, the Low pulse must be greater than the minimum width specified, or it is ignored. See Electrical Characteristics on page 221 for details.

# Low Voltage Detection

In addition to the Voltage Brownout (VBO) Reset described above, it is also possible to generate an interrupt when the supply voltage drops below a user-selected value. For details about configuring the Low Voltage Detection (LVD) and the threshold levels available, see Trim Bit Address 0003H on page 159. The LVD function is available on the 8-pin product versions only.

When the supply voltage drops below the LVD threshold, the LVD bit of the Reset Status (RSTSTAT) register is set to one. This bit remains one until the low-voltage condition goes away. Reading or writing this bit does not clear it. The LVD circuit can also generate an interrupt when so enabled, see Interrupt Vectors and Priority on page 58. The LVD bit is NOT latched, so enabling the interrupt is the only way to guarantee detection of a transient low voltage event.

The LVD functionality depends on circuitry shared with the VBO block; therefore, disabling the VBO also disables the LVD.

# **Reset Register Definitions**

The following sections define the Reset registers.

# **Reset Status Register**

The Reset Status (RSTSTAT) register is a read-only register that indicates the source of the most recent Reset event, indicates a Stop Mode Recovery event, and indicates a Watchdog Timer time-out. Reading this register resets the upper four bits to 0.

This register shares its address with the Watchdog Timer control register, which is write-only (see Table 11 on page 31).







Reserved—Must be 0.

C3ENL—Port C3 Interrupt Request Enable Low Bit C2ENL—Port C2 Interrupt Request Enable Low Bit C1ENL—Port C1 Interrupt Request Enable Low Bit C0ENL—Port C0 Interrupt Request Enable Low Bit

#### Interrupt Edge Select Register

The Interrupt Edge Select (IRQES) register (Table 45) determines whether an interrupt is generated for the rising edge or falling edge on the selected GPIO Port A input pin.

Table 45. Interrupt Edge Select Register (IRQES)

BITS	7	6	5	4	3	2	1	0
FIELD	IES7	IES6	IES5	IES4	IES3	IES2	IES1	IES0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR				FC	DH			

IES*x*—Interrupt Edge Select *x* 

0 = An interrupt request is generated on the falling edge of the PAx input.

1 = An interrupt request is generated on the rising edge of the PAx input.

where *x* indicates the specific GPIO Port pin number (0 through 7).

#### **Shared Interrupt Select Register**

The Shared Interrupt Select (IRQSS) register (Table 46) determines the source of the PADxS interrupts. The Shared Interrupt Select register selects between Port A and alternate sources for the individual interrupts.

Because these shared interrupts are edge-triggered, it is possible to generate an interrupt just by switching from one shared source to another. For this reason, an interrupt must be disabled before switching between sources.



- 2. Write to the Timer High and Low Byte registers to set the starting count value. Writing these registers only affects the first pass in GATED mode. After the first timer reset in GATED mode, counting always begins at the reset value of 0001H.
- 3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
- 4. Enable the timer interrupt, if appropriate, and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input deassertion and reload events. If appropriate, configure the timer interrupt to be generated only at the input deassertion event or the reload event by setting TICONFIG field of the TxCTL0 register.
- 5. Configure the associated GPIO port pin for the Timer Input alternate function.
- 6. Write to the Timer Control register to enable the timer.
- 7. Assert the Timer Input signal to initiate the counting.

#### CAPTURE/COMPARE Mode

In CAPTURE/COMPARE mode, the timer begins counting on the first external Timer Input transition. The acceptable transition (rising edge or falling edge) is set by the TPOL bit in the Timer Control Register. The timer input is the system clock.

Every subsequent acceptable transition (after the first) of the Timer Input signal captures the current count value. The Capture value is written to the Timer PWM High and Low Byte Registers. When the Capture event occurs, an interrupt is generated, the count value in the Timer High and Low Byte registers is reset to 0001H, and counting resumes. The INPCAP bit in TxCTL0 register is set to indicate the timer interrupt is caused by an input capture event.

If no Capture event occurs, the timer counts up to the 16-bit Compare value stored in the Timer Reload High and Low Byte registers. Upon reaching the Compare value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. The INPCAP bit in TxCTL0 register is cleared to indicate the timer interrupt is not because of an input capture event.

Follow the steps below for configuring a timer for CAPTURE/COMPARE mode and initiating the count:

- 1. Write to the Timer Control register to:
  - Disable the timer.
  - Configure the timer for CAPTURE/COMPARE mode.
  - Set the prescale value.
  - Set the Capture edge (rising or falling) for the Timer Input.
- 2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
- 3. Write to the Timer Reload High and Low Byte registers to set the Compare value.



110 = 64 cycles delay 111 = 128 cycles delay

INPCAP—Input Capture Event

This bit indicates if the most recent timer interrupt is caused by a Timer Input Capture Event.

0 = Previous timer interrupt is not a result of Timer Input Capture Event

1 = Previous timer interrupt is a result of Timer Input Capture Event

#### Timer 0–1 Control Register 1

The Timer 0–1 Control (TxCTL1) registers enable/disable the timers, set the prescaler value, and determine the timer operating mode (Table 49).

Table 49. Timer 0–1 Control Register 1 (TxCTL1)

BITS	7	6	5	4	3	2	1	0		
FIELD	TEN	TPOL		PRES		TMODE				
RESET	0	0	0	0	0	0 0 0				
R/W	R/W	R/W	R/W	R/W	R/W	R/W R/W R/W				
ADDR		F07H, F0FH								

TEN—Timer Enable

0 = Timer is disabled.

1 = Timer enabled to count.

TPOL—Timer Input/Output Polarity

Operation of this bit is a function of the current operating mode of the timer.

#### **ONE-SHOT mode**

When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

#### **CONTINUOUS mode**

When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

#### COUNTER mode

If the timer is enabled the Timer Output signal is complemented after timer reload.

0 = Count occurs on the rising edge of the Timer Input signal.

1 = Count occurs on the falling edge of the Timer Input signal.



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#### **PWM SINGLE OUTPUT mode**

0 = Timer Output is forced Low (0) when the timer is disabled. When enabled, the Timer Output is forced High (1) upon PWM count match and forced Low (0) upon Reload.

1 = Timer Output is forced High (1) when the timer is disabled. When enabled, the Timer Output is forced Low (0) upon PWM count match and forced High (1) upon Reload.

#### **CAPTURE mode**

0 = Count is captured on the rising edge of the Timer Input signal.

1 = Count is captured on the falling edge of the Timer Input signal.

#### **COMPARE mode**

When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

#### **GATED** mode

0 = Timer counts when the Timer Input signal is High (1) and interrupts are generated on the falling edge of the Timer Input.

1 = Timer counts when the Timer Input signal is Low (0) and interrupts are generated on the rising edge of the Timer Input.

#### **CAPTURE/COMPARE mode**

0 = Counting is started on the first rising edge of the Timer Input signal. The current count is captured on subsequent rising edges of the Timer Input signal.

1 = Counting is started on the first falling edge of the Timer Input signal. The current count is captured on subsequent falling edges of the Timer Input signal.

#### **PWM DUAL OUTPUT mode**

0 = Timer Output is forced Low (0) and Timer Output Complement is forced High (1) when the timer is disabled. When enabled, the Timer Output is forced High (1) upon PWM count match and forced Low (0) upon Reload. When enabled, the Timer Output Complement is forced Low (0) upon PWM count match and forced High (1) upon Reload. The PWMD field in TxCTL0 register is a programmable delay to control the number of cycles time delay before the Timer Output and the Timer Output Complement is forced to High (1).

1 = Timer Output is forced High (1) and Timer Output Complement is forced Low (0) when the timer is disabled. When enabled, the Timer Output is forced Low (0) upon PWM count match and forced High (1) upon Reload. When enabled, the Timer Output Complement is forced High (1) upon PWM count match and forced Low (0) upon Reload. The PWMD field in TxCTL0 register is a programmable delay to control the number of cycles time delay before the Timer Output and the Timer Output Complement is forced to Low (0).



1000 = PWM DUAL OUTPUT mode 1001 = CAPTURE RESTART mode 1010 = COMPARATOR COUNTER mode

# Timer 0–1 High and Low Byte Registers

The Timer 0–1 High and Low Byte (TxH and TxL) registers (Table 50 and Table 51) contain the current 16-bit timer count value. When the timer is enabled, a read from TxH causes the value in TxL to be stored in a temporary holding register. A read from TxL always returns this temporary register when the timers are enabled. When the timer is disabled, reads from TxL read the register directly.

Writing to the Timer High and Low Byte registers while the timer is enabled is not recommended. There are no temporary holding registers available for write operations, so simultaneous 16-bit writes are not possible. If either the Timer High or Low Byte registers are written during counting, the 8-bit written value is placed in the counter (High or Low Byte) at the next clock edge. The counter continues counting from the new value.

BITS	7	6	5	4	3	2	1	0	
FIELD	TH								
RESET	0 0 0 0 0 0 0 0								
R/W	R/W         R/W								
ADDR				F00H,	F08H				

#### Table 50. Timer 0–1 High Byte Register (TxH)

#### Table 51. Timer 0–1 Low Byte Register (TxL)

BITS	7	6	5	4	3	2	1	0
FIELD				Т	Ľ			
RESET	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F01H, F09H							

TH and TL-Timer High and Low Bytes

These 2 bytes, {TH[7:0], TL[7:0]}, contain the current 16-bit timer count value.

## **Timer Reload High and Low Byte Registers**

The Timer 0–1 Reload High and Low Byte (TxRH and TxRL) registers (Table 52 and Table 53) store a 16-bit reload value, {TRH[7:0], TRL[7:0]}. Values written to the Timer Reload High Byte register are stored in a temporary holding register. When a write to the



# Watchdog Timer

The Watchdog Timer (WDT) protects against corrupt or unreliable software, power faults, and other system-level problems which may place the Z8 Encore! XP<sup>®</sup> F082A Series devices into unsuitable operating states. The features of Watchdog Timer include:

- On-chip RC oscillator.
- A selectable time-out response: reset or interrupt.
- 24-bit programmable time-out value.

# Operation

The Watchdog Timer is a one-shot timer that resets or interrupts the Z8 Encore! XP F082A Series devices when the WDT reaches its terminal count. The Watchdog Timer uses a dedicated on-chip RC oscillator as its clock source. The Watchdog Timer operates in only two modes: ON and OFF. Once enabled, it always counts and must be refreshed to prevent a time-out. Perform an enable by executing the WDT instruction or by setting the WDT\_AO Flash Option Bit. The WDT\_AO bit forces the Watchdog Timer to operate immediately upon reset, even if a WDT instruction has not been executed.

The Watchdog Timer is a 24-bit reloadable downcounter that uses three 8-bit registers in the eZ8 CPU register space to set the reload value. The nominal WDT time-out period is described by the following equation:

WDT Time-out Period (ms) =  $\frac{\text{WDT Reload Value}}{10}$ 

where the WDT reload value is the decimal value of the 24-bit value given by {WDTU[7:0], WDTH[7:0], WDTL[7:0]} and the typical Watchdog Timer RC oscillator frequency is 10 kHz. The Watchdog Timer cannot be refreshed after it reaches 000002H. The WDT Reload Value must not be set to values below 000004H. Table 56 provides information about approximate time-out delays for the minimum and maximum WDT reload values.

#### Table 56. Watchdog Timer Approximate Time-Out Delays

WDT Reload Value	WDT Reload Value	Approximate (with 10 kHz typical V	e Time-Out Delay VDT oscillator frequency)
(Hex)	(Decimal)	Typical	Description
000004	4	400 µs	Minimum time-out delay
FFFFF	16,777,215	28 minutes	Maximum time-out delay



- 3. Write to the ADC Control Register 0 to configure the ADC for continuous conversion. The bit fields in the ADC Control register may be written simultaneously:
  - Write to the ANAIN[3:0] field to select from the available analog input sources (different input pins available depending on the device).
  - Set CONT to 1 to select continuous conversion.
  - If the internal VREF must be output to a pin, set the REFEXT bit to 1. The internal voltage reference must be enabled in this case.
  - Write the REFSELL bit of the pair {REFSELH, REFSELL} to select the internal voltage reference level or to disable the internal reference. The REFSELH bit is contained in ADC Control/Status Register 1.
  - Set CEN to 1 to start the conversions.
- 4. When the first conversion in continuous operation is complete (after 5129 system clock cycles, plus the 40 cycles for power-up, if necessary), the ADC control logic performs the following operations:
  - CEN resets to 0 to indicate the first conversion is complete. CEN remains 0 for all subsequent conversions in continuous operation.
  - An interrupt request is sent to the Interrupt Controller to indicate the conversion is complete.
- 5. The ADC writes a new data result every 256 system clock cycles. For each completed conversion, the ADC control logic performs the following operations:
  - Writes the 13-bit two's complement result to {ADCD\_H[7:0], ADCD L[7:3]}.
  - Sends an interrupt request to the Interrupt Controller denoting conversion complete.
- 6. To disable continuous conversion, clear the CONT bit in the ADC Control Register to 0.

#### Interrupts

The ADC is able to interrupt the CPU when a conversion has been completed. When the ADC is disabled, no new interrupts are asserted; however, an interrupt pending when the ADC is disabled is not cleared.

## **Calibration and Compensation**

The Z8 Encore! XP<sup>®</sup> F082A Series ADC is factory calibrated for offset error and gain error, with the compensation data stored in Flash memory. Alternatively, you can perform your own calibration, storing the values into Flash themselves. Thirdly, the user code can perform a manual offset calibration during DIFFERENTIAL mode operation.



Info Page Address	Memory Address	Usage
5C	FE5C	Randomized Lot ID Byte 23
5D	FE5D	Randomized Lot ID Byte 22
5E	FE5E	Randomized Lot ID Byte 21
5F	FE5F	Randomized Lot ID Byte 20
61	FE61	Randomized Lot ID Byte 19
62	FE62	Randomized Lot ID Byte 18
64	FE64	Randomized Lot ID Byte 17
65	FE65	Randomized Lot ID Byte 16
67	FE67	Randomized Lot ID Byte 15
68	FE68	Randomized Lot ID Byte 14
6A	FE6A	Randomized Lot ID Byte 13
6B	FE6B	Randomized Lot ID Byte 12
6D	FE6D	Randomized Lot ID Byte 11
6E	FE6E	Randomized Lot ID Byte 10
70	FE70	Randomized Lot ID Byte 9
71	FE71	Randomized Lot ID Byte 8
73	FE73	Randomized Lot ID Byte 7
74	FE74	Randomized Lot ID Byte 6
76	FE76	Randomized Lot ID Byte 5
77	FE77	Randomized Lot ID Byte 4
79	FE79	Randomized Lot ID Byte 3
7A	FE7A	Randomized Lot ID Byte 2
7C	FE7C	Randomized Lot ID Byte 1
7D	FE7D	Randomized Lot ID Byte 0 (least significant)

## Table 102. Randomized Lot ID Locations (Continued)



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Assembly	Symbolic	Addres	s Mode	Opcode(s)			Fla	ags			Fetch	Instr.
Mnemonic	Operation	dst	src	(Hex)	С	Ζ	S	۷	D	Н	Cycles	Cycles
HALT	Halt Mode			7F	_	_	_	_	-	_	1	2
INC dst	$dst \gets dst + 1$	R		20	-	*	*	_	-	_	2	2
		IR		21	-						2	3
		r		0E-FE	-						1	2
INCW dst	$dst \gets dst + 1$	RR		A0	-	*	*	*	-	-	2	5
		IRR		A1	-						2	6
IRET	$\begin{array}{l} FLAGS \leftarrow @SP \\ SP \leftarrow SP + 1 \\ PC \leftarrow @SP \\ SP \leftarrow SP + 2 \\ IRQCTL[7] \leftarrow 1 \end{array}$			BF	*	*	*	*	*	*	1	5
JP dst	$PC \gets dst$	DA		8D	-	_	-	-	-	-	3	2
		IRR		C4	-						2	3
JP cc, dst	if cc is true PC $\leftarrow$ dst	DA		0D-FD	_	_	-	-	-	-	3	2
JR dst	$PC \gets PC + X$	DA		8B	_	_	_	_	-	_	2	2
JR cc, dst	if cc is true PC $\leftarrow$ PC + X	DA		0B-FB	-	-	-	_	-	-	2	2
LD dst, rc	$dst \gets src$	r	IM	0C-FC	-	-	-	-	-	-	2	2
		r	X(r)	C7	-						3	3
		X(r)	r	D7	-						3	4
		r	lr	E3	-						2	3
		R	R	E4	-						3	2
		R	IR	E5	-						3	4
		R	IM	E6	-						3	2
		IR	IM	E7	-						3	3
		lr	r	F3	-						2	3
		IR	R	F5	-						3	3
Flags Notation:	* = Value is a functior – = Unaffected X = Undefined	of the result	of the o	peration.	0 = 1 =	Re Se	set t to	to ( 1	)			

## Table 124. eZ8 CPU Instruction Summary (Continued)



		V <sub>DI</sub>	<sub>D</sub> = 2.7 V to 3	3.6 V		
			Maximum <sup>2</sup>	Maximum <sup>3</sup>		
Symbol	Parameter	Typical $^1$	Std Temp	Ext Temp	Units	Conditions
I <sub>DD</sub> Stop	Supply Current in STOP Mode	0.1			μA	No peripherals enabled. All pins driven to $V_{DD}$ or $V_{SS}.$
I <sub>DD</sub> Halt	Supply Current in HALT	35	55	65	μA	32 kHz
	Mode (with all peripherals disabled)	520			μA	5.5 MHz
		2.1	2.85	2.85	mA	20 MHz
I <sub>DD</sub>	Supply Current in	2.8			mA	32 kHz
	ACTIVE Mode (with all peripherals disabled)	4.5	5.2	5.2	mA	5.5 MHz
		5.5	6.5	6.5	mA	10 MHz
	-	7.9	11.5	11.5	mA	20 MHz
I <sub>DD</sub> WDT	Watchdog Timer Supply Current	0.9	1.0	1.1	μA	
I <sub>DD</sub>	Crystal Oscillator	40			μA	32 kHz
XTAL	Supply Current	230			μA	4 MHz
	-	760			μA	20 MHz
I <sub>DD</sub> IPO	Internal Precision Oscillator Supply Current	350	500	550	μA	
I <sub>DD</sub> VBO	Voltage Brownout and Low-Voltage Detect	50			μA	For 20-/28-pin devices (VBO only); See Notes 4
	Supply Current					For 8-pin devices; See Notes 4
I <sub>DD</sub> ADC	Analog to Digital	2.8	3.1	3.2	mA	32 kHz
	Converter Supply Current (with External	3.1	3.6	3.7	mA	5.5 MHz
	Reference)	3.3	3.7	3.8	mA	10 MHz
	-	3.7	4.2	4.3	mA	20 MHz
I <sub>DD</sub> ADCRef	ADC Internal Reference Supply Current	0			μA	See Notes 4
I <sub>DD</sub> CMP	Comparator supply Current	150	180	190	μA	See Notes 4

# Table 128. Power Consumption

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Note: ZILOG supplies both options for production. Component layout PCB design should cover bigger option 01.

#### Figure 45. 28-Pin Plastic Dual Inline Package (PDIP)



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Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description	
Z8 Encore! XP <sup>®</sup> F082A Series with 2 KB Flash												
Standard Temperature: 0 °C to 70 °C												
Z8F021APB020SC	2 KB	512 B	64 B	6	13	2	0	1	1	0	PDIP 8-pin package	
Z8F021AQB020SC	2 KB	512 B	64 B	6	13	2	0	1	1	0	QFN 8-pin package	
Z8F021ASB020SC	2 KB	512 B	64 B	6	13	2	0	1	1	0	SOIC 8-pin package	
Z8F021ASH020SC	2 KB	512 B	64 B	17	19	2	0	1	1	0	SOIC 20-pin package	
Z8F021AHH020SC	2 KB	512 B	64 B	17	19	2	0	1	1	0	SSOP 20-pin package	
Z8F021APH020SC	2 KB	512 B	64 B	17	19	2	0	1	1	0	PDIP 20-pin package	
Z8F021ASJ020SC	2 KB	512 B	64 B	25	19	2	0	1	1	0	SOIC 28-pin package	
Z8F021AHJ020SC	2 KB	512 B	64 B	25	19	2	0	1	1	0	SSOP 28-pin package	
Z8F021APJ020SC	2 KB	512 B	64 B	25	19	2	0	1	1	0	PDIP 28-pin package	
Extended Temperature: -40 °C to 105 °C												
Z8F021APB020EC	2 KB	512 B	64 B	6	13	2	0	1	1	0	PDIP 8-pin package	
Z8F021AQB020EC	2 KB	512 B	64 B	6	13	2	0	1	1	0	QFN 8-pin package	
Z8F021ASB020EC	2 KB	512 B	64 B	6	13	2	0	1	1	0	SOIC 8-pin package	
Z8F021ASH020EC	2 KB	512 B	64 B	17	19	2	0	1	1	0	SOIC 20-pin package	
Z8F021AHH020EC	2 KB	512 B	64 B	17	19	2	0	1	1	0	SSOP 20-pin package	
Z8F021APH020EC	2 KB	512 B	64 B	17	19	2	0	1	1	0	PDIP 20-pin package	
Z8F021ASJ020EC	2 KB	512 B	64 B	25	19	2	0	1	1	0	SOIC 28-pin package	
Z8F021AHJ020EC	2 KB	512 B	64 B	25	19	2	0	1	1	0	SSOP 28-pin package	
Z8F021APJ020EC	2 KB	512 B	64 B	25	19	2	0	1	1	0	PDIP 28-pin package	
Replace C with G for Lead-Free Packaging												

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