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Zilog - Z8F012AHH020SC00TR Datasheet



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Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	16 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f012ahh020sc00tr

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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Pin Description

The Z8 Encore! XP[®] F082A Series products are available in a variety of packages styles and pin configurations. This chapter describes the signals and available pin configurations for each of the package styles. For information on physical package specifications, see Packaging on page 241.

Available Packages

The following package styles are available for each device in the Z8 Encore! XP F082A Series product line:

- SOIC
 - 8-, 20-, and 28-pin
- PDIP
 - 8-, 20-, and 28-pin
- SSOP
 - 20- and 28- pin
- QFN (this is an MLF-S, a QFN style package with an 8-pin SOIC footprint)
 - 8-pin

In addition, the Z8 Encore! XP F082A Series devices are available both with and without advanced analog capability (ADC, temperature sensor and op amp). Devices Z8F082A, Z8F042A, Z8F022A, and Z8F012A contain the advanced analog, while devices Z8F081A, Z8F041A, Z8F021A, and Z8F011A do not have the advanced analog capability.

Pin Configurations

Figure 2 through Figure 4 display the pin configurations for all the packages available in the Z8 Encore! XP F082A Series. See Table 2 on page 11 for a description of the signals. The analog input alternate functions (ANAx) are not available on the Z8F081A, Z8F041A, Z8F021A, and Z8F011A devices. The analog supply pins (AV_{DD} and AV_{SS}) are also not available on these parts, and are replaced by PB6 and PB7.

At reset, all Port A, B and C pins default to an input state. In addition, any alternate functionality is not enabled, so the pins function as general purpose input ports until programmed otherwise. At powerup, the PD0 pin defaults to the RESET alternate function.

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addresses outside the available Flash memory addresses returns FFH. Writing to these unimplemented Program Memory addresses produces no effect. Table 5 describes the Program Memory Maps for the Z8 Encore! XP F082A Series products.

Program Memory Address (Hex)	Function
Z8F082A and Z8F081A Products	
0000–0001	Flash Option Bits
0002–0003	Reset Vector
0004–0005	WDT Interrupt Vector
0006–0007	Illegal Instruction Trap
0008–0037	Interrupt Vectors*
0038–0039	Reserved
003A–003D	Oscillator Fail Trap Vectors
003E–1FFF	Program Memory
Z8F042A and Z8F041A Products	
0000–0001	Flash Option Bits
0002–0003	Reset Vector
0004–0005	WDT Interrupt Vector
0006–0007	Illegal Instruction Trap
0008–0037	Interrupt Vectors*
0038–0039	Reserved
003A-003D	Oscillator Fail Trap Vectors
003E-0FFF	Program Memory

 Table 5. Z8 Encore! XP F082A Series Program Memory Maps

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Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
F0B	Timer 1 Reload Low Byte	T1RL	FF	88
F0C	Timer 1 PWM High Byte	T1PWMH	00	88
F0D	Timer 1 PWM Low Byte	T1PWML	00	89
F0E	Timer 1 Control 0	T1CTL0	00	83
F0F	Timer 1 Control 1	T1CTL1	00	84
F10–F6F	Reserved	_	XX	
UART				
F40	UART Transmit/Receive Data Registers	TXD, RXD	XX	113
F41	UART Status 0 Register	U0STAT0	00	111
F42	UART Control 0 Register	U0CTL0	00	108
F43	UART Control 1 Register	U0CTL1	00	108
F44	UART Status 1 Register	U0STAT1	00	112
F45	UART Address Compare Register	U0ADDR	00	114
F46	UART Baud Rate High Byte Register	U0BRH	FF	114
F47	UART Baud Rate Low Byte Register	U0BRL	FF	114
Analog-to-Digit	tal Converter (ADC)			
F70	ADC Control 0	ADCCTL0	00	130
F71	ADC Control 1	ADCCTL1	80	130
F72	ADC Data High Byte	ADCD_H	XX	133
F73	ADC Data Low Bits	ADCD_L	XX	133
F74–F7F	Reserved	_	XX	
Low Power Co	ntrol			
F80	Power Control 0	PWRCTL0	80	35
F81	Reserved	_	XX	
LED Controller				
F82	LED Drive Enable	LEDEN	00	52
F83	LED Drive Level High Byte	LEDLVLH	00	53
F84	LED Drive Level Low Byte	LEDLVLL	00	54
F85	Reserved	—	XX	
Oscillator Cont	rol			
F86	Oscillator Control	OSCCTL	A0	190
F87–F8F	Reserved	_	XX	
Comparator 0				
F90	Comparator 0 Control	CMP0	14	136
XX=Undefined				

Table 7. Register File Address Map (Continued)

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Reset Sources

Table 9 lists the possible sources of a system reset.

Operating Mode	Reset Source	Special Conditions	
NORMAL or HALT modes	Power-On Reset/Voltage Brownout	Reset delay begins after supply voltage exceeds POR level.	
	Watchdog Timer time-out when configured for Reset	None.	
	RESET pin assertion	All reset pulses less than three system clocks in width are ignored.	
	On-Chip Debugger initiated Reset (OCDCTL[0] set to 1)	System Reset, except the On-Chip Debugger is unaffected by the reset.	
STOP mode	Power-On Reset/Voltage Brownout	Reset delay begins after supply voltage exceeds POR level.	
	RESET pin assertion	All reset pulses less than the specified analog delay are ignored. See Table 131 on page 229.	
	DBG pin driven Low	None.	

Table 9. Reset Sources and Resulting Reset Type

Power-On Reset

Z8 Encore! XP F082A Series devices contain an internal Power-On Reset circuit. The POR circuit monitors the supply voltage and holds the device in the Reset state until the supply voltage reaches a safe operating level. After the supply voltage exceeds the POR voltage threshold (V_{POR}), the device is held in the Reset state until the POR Counter has timed out. If the crystal oscillator is enabled by the option bits, this timeout is longer.

After the Z8 Encore! XP F082A Series device exits the Power-On Reset state, the eZ8 CPU fetches the Reset vector. Following Power-On Reset, the POR status bit in the Reset Status (RSTSTAT) register is set to 1.

Figure 5 displays Power-On Reset operation. See Electrical Characteristics on page 221 for the POR threshold voltage (V_{POR}).



Table 31. LED Drive Level Low Register (LEDLVLL)

BITS	7	6	5	4	3	2	1	0
FIELD		LEDLVLL[7:0]						
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F84H							

LEDLVLL[7:0]—LED Level Low Bit

{LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin.

00 = 3 mA01 = 7 mA10 = 13 mA

11 = 20 mA



Follow the steps below for configuring a timer for COMPARE mode and initiating the count:

- 1. Write to the Timer Control register to:
 - Disable the timer.
 - Configure the timer for COMPARE mode.
 - Set the prescale value.
 - Set the initial logic level (High or Low) for the Timer Output alternate function, if appropriate.
- 2. Write to the Timer High and Low Byte registers to set the starting count value.
- 3. Write to the Timer Reload High and Low Byte registers to set the Compare value.
- 4. Enable the timer interrupt, if appropriate, and set the timer interrupt priority by writing to the relevant interrupt registers.
- 5. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
- 6. Write to the Timer Control register to enable the timer and initiate counting.

In COMPARE mode, the system clock always provides the timer input. The Compare time can be calculated by the following equation:

COMPARE Mode Time (s) = $\frac{(Compare Value - Start Value) \times Prescale}{System Clock Frequency (Hz)}$

GATED Mode

In GATED mode, the timer counts only when the Timer Input signal is in its active state (asserted), as determined by the TPOL bit in the Timer Control register. When the Timer Input signal is asserted, counting begins. A timer interrupt is generated when the Timer Input signal is deasserted or a timer reload occurs. To determine if a Timer Input signal deassertion generated the interrupt, read the associated GPIO input value and compare to the value stored in the TPOL bit.

The timer counts up to the 16-bit Reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. When reaching the Reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes (assuming the Timer Input signal remains asserted). Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer reset.

Follow the steps below for configuring a timer for GATED mode and initiating the count:

- 1. Write to the Timer Control register to:
 - Disable the timer.
 - Configure the timer for GATED mode.
 - Set the prescale value.



- 4. Enable the timer interrupt, if appropriate, and set the timer interrupt priority by writing to the relevant interrupt registers.By default, the timer interrupt are generated for both input capture and reload events. If appropriate, configure the timer interrupt to be generated only at the input capture event or the reload event by setting TICONFIG field of the TxCTL0 register.
- 5. Configure the associated GPIO port pin for the Timer Input alternate function.
- 6. Write to the Timer Control register to enable the timer.
- 7. Counting begins on the first appropriate transition of the Timer Input signal. No interrupt is generated by this first edge.

In CAPTURE/COMPARE mode, the elapsed time from timer start to Capture event can be calculated using the following equation:

Capture Elapsed Time (s) = $\frac{(Capture Value - Start Value) \times Prescale}{System Clock Frequency (Hz)}$

Reading the Timer Count Values

The current count value in the timers can be read while counting (enabled). This capability has no effect on timer operation. When the timer is enabled and the Timer High Byte register is read, the contents of the Timer Low Byte register are placed in a holding register. A subsequent read from the Timer Low Byte register returns the value in the holding register. This operation allows accurate reads of the full 16-bit timer count value while enabled. When the timers are not enabled, a read from the Timer Low Byte register returns the actual value in the counter.

Timer Pin Signal Operation

Timer Output is a GPIO Port pin alternate function. The Timer Output is toggled every time the counter is reloaded.

The Timer Input can be used as a selectable counting source. It shares the same pin as the complementary timer output. When selected by the GPIO Alternate Function Registers, this pin functions as a timer input in all modes except for the DUAL PWM OUTPUT mode. For this mode, there is no timer input available.



1000 = PWM DUAL OUTPUT mode 1001 = CAPTURE RESTART mode 1010 = COMPARATOR COUNTER mode

Timer 0–1 High and Low Byte Registers

The Timer 0–1 High and Low Byte (TxH and TxL) registers (Table 50 and Table 51) contain the current 16-bit timer count value. When the timer is enabled, a read from TxH causes the value in TxL to be stored in a temporary holding register. A read from TxL always returns this temporary register when the timers are enabled. When the timer is disabled, reads from TxL read the register directly.

Writing to the Timer High and Low Byte registers while the timer is enabled is not recommended. There are no temporary holding registers available for write operations, so simultaneous 16-bit writes are not possible. If either the Timer High or Low Byte registers are written during counting, the 8-bit written value is placed in the counter (High or Low Byte) at the next clock edge. The counter continues counting from the new value.

BITS	7	6	5	4	3	2	1	0
FIELD	TH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR		F00H, F08H						

Table 50. Timer 0–1 High Byte Register (TxH)

Table 51. Timer 0–1 Low Byte Register (TxL)

BITS	7	6	5	4	3	2	1	0
FIELD	TL TL							
RESET	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F01H, F09H							

TH and TL-Timer High and Low Bytes

These 2 bytes, {TH[7:0], TL[7:0]}, contain the current 16-bit timer count value.

Timer Reload High and Low Byte Registers

The Timer 0–1 Reload High and Low Byte (TxRH and TxRL) registers (Table 52 and Table 53) store a 16-bit reload value, {TRH[7:0], TRL[7:0]}. Values written to the Timer Reload High Byte register are stored in a temporary holding register. When a write to the

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Universal Asynchronous Receiver/Transmitter

The universal asynchronous receiver/transmitter (UART) is a full-duplex communication channel capable of handling asynchronous data transfers. The UART uses a single 8-bit data mode with selectable parity. Features of the UART include:

- 8-bit asynchronous data transfer.
- Selectable even- and odd-parity generation and checking.
- Option of one or two STOP bits.
- Separate transmit and receive interrupts.
- Framing, parity, overrun and break detection.
- Separate transmit and receive enables.
- 16-bit baud rate generator (BRG).
- Selectable MULTIPROCESSOR (9-bit) mode with three configurable interrupt schemes.
- Baud rate generator (BRG) can be configured and used as a basic 16-bit timer.
- Driver enable (DE) output for external bus transceivers.

Architecture

The UART consists of three primary functional blocks: transmitter, receiver, and baud rate generator. The UART's transmitter and receiver function independently, but employ the same baud rate and data format. Figure 10 on page 98 displays the UART architecture.

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Low Power Operational Amplifier

Overview

The LPO is a general-purpose low power operational amplifier. Each of the three ports of the amplifier is accessible from the package pins. The LPO contains only one pin configuration: ANA0 is the output/feedback node, ANA1 is the inverting input and ANA2 is the non-inverting input.

Operation

To use the LPO, it must be enabled in the Power Control Register 0 (PWRCTL0). The default state of the LPO is OFF. To use the LPO, the LPO bit must be cleared, turning it ON (Power Control Register 0 (PWRCTL0) on page 35). When making normal ADC measurements on ANA0 (measurements not involving the LPO output), the LPO bit must be OFF. Turning the LPO bit ON interferes with normal ADC measurements.



Warning: The LPO bit enables the amplifier even in STOP mode. If the amplifier is not required in STOP mode, disable it. Failing to perform this results in STOP mode currents higher than necessary.

As with other ADC measurements, any pins used for analog purposes must be configured as such in the GPIO registers (see Port A–D Alternate Function Sub-Registers on page 47).

LPO output measurements are made on ANA0, as selected by the ANAIN[3:0] bits of ADC Control Register 0. It is also possible to make single-ended measurements on ANA1 and ANA2 while the amplifier is enabled, which is often useful for determining offset conditions. Differential measurements between ANA0 and ANA2 may be useful for noise cancellation purposes.

If the LPO output is routed to the ADC, then the BUFFMODE[2:0] bits of ADC Control/Status Register 1 must also be configured for unity-gain buffered operation. Sampling the LPO in an unbuffered mode is not recommended.

When either input is overdriven, the amplifier output saturates at the positive or negative supply voltage. No instability results.



Flash Memory

The products in the Z8 Encore! XP[®] F082A Series feature a non-volatile Flash memory of 8 KB (8192), 4 KB (4096), 2 KB (2048 bytes), or 1 KB (1024) with read/write/ erase capability. The Flash Memory can be programmed and erased in-circuit by user code or through the On-Chip Debugger. The features include:

- User controlled read and write protect capability
- Sector-based write protection scheme
- Additional protection schemes against accidental program and erasure

Architecture

The Flash memory array is arranged in pages with 512 bytes per page. The 512 byte page is the minimum Flash block size that can be erased. Each page is divided into 8 rows of 64 bytes.

For program or data protection, the Flash memory is also divided into sectors. In the Z8 Encore! XP F082A Series, these sectors are either 1024 bytes (in the 8 KB devices) or 512 bytes (all other memory sizes) in size. Page and sector sizes are not generally equal.

The first 2 bytes of the Flash Program memory are used as Flash Option Bits. For more information about their operation, see Flash Option Bits on page 153.

Table 76 describes the Flash memory configuration for each device in the Z8 Encore! XPF082A Series. Figure 21 displays the Flash memory arrangement.

Part Number	Flash Size KB (Bytes)	Flash Pages	Program Memory Addresses	Flash Sector Size (Bytes)
Z8F08xA	8 (8192)	16	0000H–1FFFH	1024
Z8F04xA	4 (4096)	8	0000H-0FFFH	512
Z8F02xA	2 (2048)	4	0000H-07FFH	512
Z8F01xA	1 (1024)	2	0000H-03FFH	512

Table 76. Z8 Encore! XP F082A Series Flash Memory Configurations

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Flash Status Register

The Flash Status (FSTAT) register indicates the current state of the Flash Controller. This register can be read at any time. The read-only Flash Status register shares its Register File address with the Write-only Flash Control register.

Table 79. Flash Status Register (FSTAT)

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved		FSTAT					
RESET	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R
ADDR	FF8H							

Reserved—Must be 0.

FSTAT—Flash Controller Status

000000 = Flash Controller locked

000001 = First unlock command received (73H written)

000010 = Second unlock command received (8CH written)

000011 = Flash Controller unlocked

000100 = Sector protect register selected

001xxx = Program operation in progress

010xxx = Page erase operation in progress

100xxx = Mass erase operation in progress

Flash Page Select Register

The Flash Page Select (FPS) register shares address space with the Flash Sector Protect Register. Unless the Flash controller is unlocked and written with 5EH, writes to this address target the Flash Page Select Register.

The register is used to select one of the available Flash memory pages to be programmed or erased. Each Flash Page contains 512 bytes of Flash memory. During a Page Erase operation, all Flash memory having addresses with the most significant 7 bits given by FPS[6:0] are chosen for program/erase operation.

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Reserved—Must be 1.

LVD TRIM-Low Voltage Detect Trim

This trimming affects the low voltage detection threshold. Each LSB represents a 50 mV change in the threshold level. Alternatively, the low voltage threshold may be computed from the options bit value by the following equation:

LVD_LVL = $3.6 \text{ V} - \text{LVD} \text{TRIM} \times 0.05 \text{ V}$

LV	/D Threshold ((V)
LVD_TRIM	Typical	Description
00000	3.60	Maximum LVD threshold
00001	3.55	
00010	3.50	
00011	3.45	
00100	3.40	
00101	3.35	
00110	3.30	
00111	3.25	
01000	3.20	
01001	3.15	
01010	3.10	Default on Reset
01011	3.05	
01100	3.00	
01101	2.95	
01110	2.90	
01111	2.85	
10000	2.80	
10001	2.75	
10010	2.70	
10011	2.70	
to	to 1.65	Minimum LVD throshold
11111	C0.1	



Oscillator Control

The Z8 Encore! $XP^{\mathbb{R}}$ F082A Series devices uses five possible clocking schemes, each user-selectable:

- Internal precision trimmed RC oscillator (IPO).
- On-chip oscillator using off-chip crystal or resonator.
- On-chip oscillator using external RC network.
- External clock drive.
- On-chip low power Watchdog Timer oscillator.
- Clock failure detection circuitry.

In addition, Z8 Encore! XP F082A Series devices contain clock failure detection and recovery circuitry, allowing continued operation despite a failure of the system clock oscillator.

Operation

This chapter discusses the logic used to select the system clock and handle primary oscillator failures.

System Clock Selection

The oscillator control block selects from the available clocks. Table 108 details each clock source and its usage.



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WDFEN-Watchdog Timer Oscillator Failure Detection Enable

1 = Failure detection of Watchdog Timer oscillator is enabled

0 = Failure detection of Watchdog Timer oscillator is disabled

SCKSEL—System Clock Oscillator Select

000 = Internal precision oscillator functions as system clock at 5.53 MHz

001 = Internal precision oscillator functions as system clock at 32 kHz

010 = Crystal oscillator or external RC oscillator functions as system clock

011 = Watchdog Timer oscillator functions as system

100 = External clock signal on PB3 functions as system clock

101 = Reserved

110 = Reserved

111 = Reserved

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Table 116 through Table 123 lists the instructions belonging to each group and the number of operands required for each instruction. Some instructions appear in more than one table as these instruction can be considered as a subset of more than one category. Within these tables, the source operand is identified as 'src', the destination operand is 'dst' and a condition code is 'cc'.

Mnemonic	Operands	Instruction
ADC	dst, src	Add with Carry
ADCX	dst, src	Add with Carry using Extended Addressing
ADD	dst, src	Add
ADDX	dst, src	Add using Extended Addressing
СР	dst, src	Compare
CPC	dst, src	Compare with Carry
CPCX	dst, src	Compare with Carry using Extended Addressing
СРХ	dst, src	Compare using Extended Addressing
DA	dst	Decimal Adjust
DEC	dst	Decrement
DECW	dst	Decrement Word
INC	dst	Increment
INCW	dst	Increment Word
MULT	dst	Multiply
SBC	dst, src	Subtract with Carry
SBCX	dst, src	Subtract with Carry using Extended Addressing
SUB	dst, src	Subtract
SUBX	dst, src	Subtract using Extended Addressing

Table 116. Arithmetic Instructions

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UART Timing

Figure 37 and Table 142 provide timing information for UART pins for the case where CTS is used for flow control. The CTS to DE assertion delay (T1) assumes the transmit data register has been loaded with data prior to CTS assertion.



		Delay (ns)				
Parameter	Abbreviation	Minimum	Maximum			
UART						
T ₁	CTS Fall to DE output delay	2 * XIN period	2 * XIN period + 1 bit time			
T ₂	DE assertion to TXD falling edge (start bit) delay	′±5				
T ₃	End of Stop Bit(s) to DE deassertion delay	± 5				

Table 142. UART Timing With CTS



Part Number	Flash	RAM	SQVN	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP [®] F082A Series with 8 KB Flash											
Z8F081APB020SC	8 KB	1 KB	0	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F081AQB020SC	8 KB	1 KB	0	6	13	2	0	1	1	0	QFN 8-pin package
Z8F081ASB020SC	8 KB	1 KB	0	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F081ASH020SC	8 KB	1 KB	0	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F081AHH020SC	8 KB	1 KB	0	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F081APH020SC	8 KB	1 KB	0	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F081ASJ020SC	8 KB	1 KB	0	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F081AHJ020SC	8 KB	1 KB	0	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F081APJ020SC	8 KB	1 KB	0	25	19	2	0	1	1	0	PDIP 28-pin package
Extended Temperature: -40 °C to 105 °C											
Z8F081APB020EC	8 KB	1 KB	0	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F081AQB020EC	8 KB	1 KB	0	6	13	2	0	1	1	0	QFN 8-pin package
Z8F081ASB020EC	8 KB	1 KB	0	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F081ASH020EC	8 KB	1 KB	0	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F081AHH020EC	8 KB	1 KB	0	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F081APH020EC	8 KB	1 KB	0	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F081ASJ020EC	8 KB	1 KB	0	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F081AHJ020EC	8 KB	1 KB	0	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F081APJ020EC	8 KB	1 KB	0	25	19	2	0	1	1	0	PDIP 28-pin package
Replace C with G for Lead-Free Packaging											



						_							
Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description		
Z8 Encore! XP [®] F082A Series Development Kit													
Z8F08A28100KITG		Z8 Encore! XP F082A Series 28-Pin Development Kit											
Z8F04A28100KITG		Z8 Encore! XP F042A Series 28-Pin Development Kit											
Z8F04A08100KITG		Z8 Encore! XP F042A Series 8-Pin Development Kit											
ZUSBSC00100ZACG		USB Smart Cable Accessory Kit											
ZUSBOPTSC01ZACG		USB Opto-Isolated Smart Cable Accessory Kit											
ZENETSC0100ZACG		Ethernet Smart Cable Accessory Kit											