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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	16 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f012ash020sc00tr

Table 14. Port Alternate Function Mapping (Non 8-Pin Parts) (Continued)

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port B	PB0	Reserved		AFS1[0]: 0
		ANA0/AMPOUT	ADC Analog Input/LPO Output	AFS1[0]: 1
	PB1	Reserved		AFS1[1]: 0
		ANA1/AMPINN	ADC Analog Input/LPO Input (N)	AFS1[1]: 1
	PB2	Reserved		AFS1[2]: 0
		ANA2/AMPINP	ADC Analog Input/LPO Input (P)	AFS1[2]: 1
	PB3	CLKIN	External Clock Input	AFS1[3]: 0
		ANA3	ADC Analog Input	AFS1[3]: 1
	PB4	Reserved		AFS1[4]: 0
		ANA7	ADC Analog Input	AFS1[4]: 1
	PB5	Reserved		AFS1[5]: 0
		VREF*	ADC Voltage Reference	AFS1[5]: 1
	PB6	Reserved		AFS1[6]: 0
		Reserved		AFS1[6]: 1
	PB7	Reserved		AFS1[7]: 0
		Reserved		AFS1[7]: 1

Note: Because there are at most two choices of alternate function for any pin of Port B, the Alternate Function Set register AFS2 is not used to select the function. Also, alternate function selection as described in [Port A–D Alternate Function Sub-Registers](#) on page 47 must also be enabled.

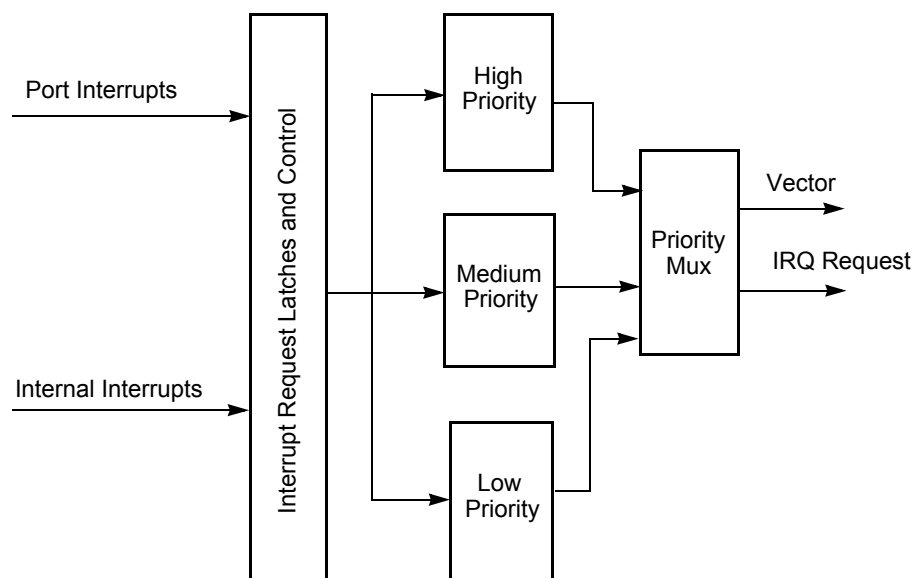
* VREF is available on PB5 in 28-pin products only.

Table 32. Trap and Interrupt Vectors in Order of Priority (Continued)

Priority	Program Memory Vector Address	Interrupt or Trap Source
	0034H	Port C Pin 1, both input edges
Lowest	0036H	Port C Pin 0, both input edges
	0038H	Reserved

Architecture

Figure 8 displays the interrupt controller block diagram.

**Figure 8. Interrupt Controller Block Diagram**

Operation

Master Interrupt Enable

The master interrupt enable bit (IRQE) in the Interrupt Control register globally enables and disables interrupts.

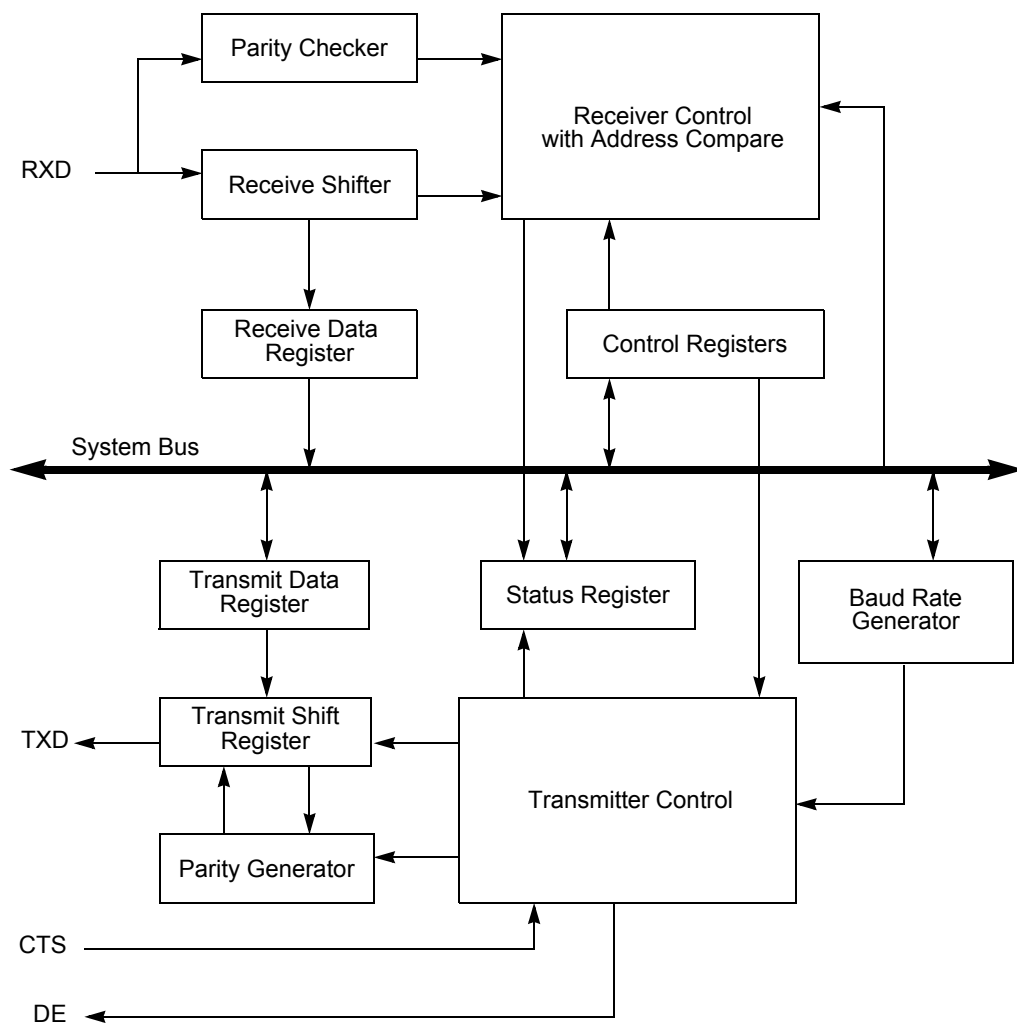


Figure 10. UART Block Diagram

Operation

Data Format

The UART always transmits and receives data in an 8-bit data format, least-significant bit first. An even or odd parity bit can be added to the data stream. Each character begins with an active Low START bit and ends with either 1 or 2 active High STOP bits. [Figure 11](#) and [Figure 12](#) display the asynchronous data format employed by the UART without parity and with parity, respectively.

The UART is now configured for interrupt-driven data transmission. Because the UART Transmit Data register is empty, an interrupt is generated immediately. When the UART Transmit interrupt is detected, the associated interrupt service routine (ISR) performs the following:

1. Write the UART Control 1 register to select the multiprocessor bit for the byte to be transmitted:
2. Set the Multiprocessor Bit Transmitter (MPBT) if sending an address byte, clear it if sending a data byte.
3. Write the data byte to the UART Transmit Data register. The transmitter automatically transfers the data to the Transmit Shift register and transmits the data.
4. Clear the UART Transmit interrupt bit in the applicable Interrupt Request register.
5. Execute the IRET instruction to return from the interrupt-service routine and wait for the Transmit Data register to again become empty.

Receiving Data using the Polled Method

Follow the steps below to configure the UART for polled data reception:

1. Write to the UART Baud Rate High and Low Byte registers to set an acceptable baud rate for the incoming data stream.
2. Enable the UART pin functions by configuring the associated GPIO Port pins for alternate function operation.
3. Write to the UART Control 1 register to enable MULTIPROCESSOR mode functions, if appropriate.
4. Write to the UART Control 0 register to:
 - Set the receive enable bit (REN) to enable the UART for data reception
 - Enable parity, if appropriate and if Multiprocessor mode is not enabled, and select either even or odd parity.
5. Check the RDA bit in the UART Status 0 register to determine if the Receive Data register contains a valid data byte (indicated by a 1). If RDA is set to 1 to indicate available data, continue to [Step 5](#). If the Receive Data register is empty (indicated by a 0), continue to monitor the RDA bit awaiting reception of the valid data.
6. Read data from the UART Receive Data register. If operating in MULTIPROCESSOR (9-bit) mode, further actions may be required depending on the MULTIPROCESSOR mode bits MPMD[1:0].
7. Return to [Step 4](#) to receive additional data.

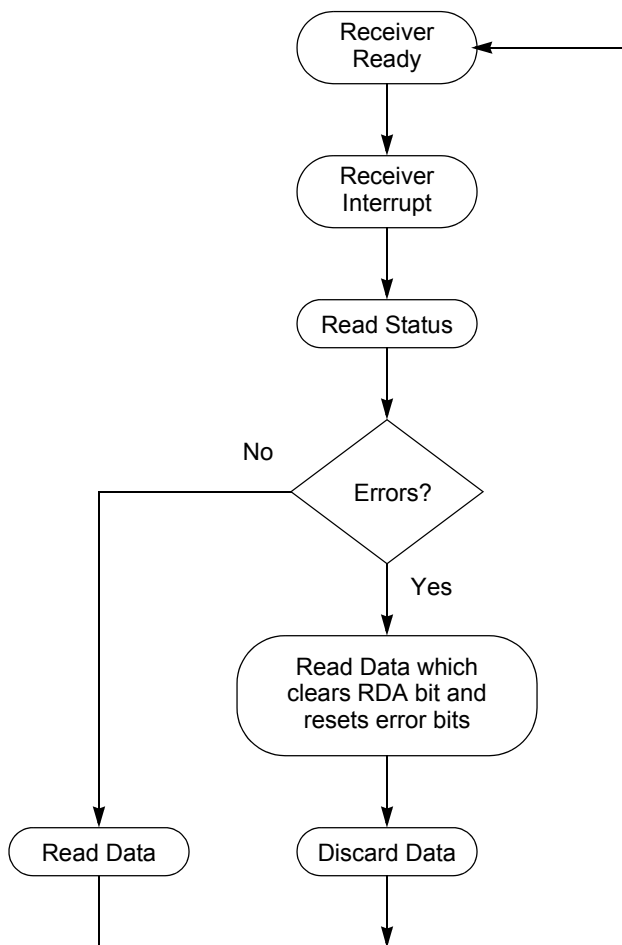


Figure 15. UART Receiver Interrupt Service Routine Flow

Baud Rate Generator Interrupts

If the baud rate generator (BRG) interrupt enable is set, the UART Receiver interrupt asserts when the UART Baud Rate Generator reloads. This condition allows the Baud Rate Generator to function as an additional counter if the UART functionality is not employed.

UART Baud Rate Generator

The UART Baud Rate Generator creates a lower frequency baud rate clock for data transmission. The input to the Baud Rate Generator is the system clock. The UART Baud Rate High and Low Byte registers combine to create a 16-bit baud rate divisor value

1 = Received data does not generate an interrupt request to the Interrupt Controller. Only receiver errors generate an interrupt request.

IREN—Infrared Encoder/Decoder Enable

0 = Infrared Encoder/Decoder is disabled. UART operates normally.

1 = Infrared Encoder/Decoder is enabled. The UART transmits and receives data through the Infrared Encoder/Decoder.

UART Status 0 Register

The UART Status 0 (UxSTAT0) and Status 1 (UxSTAT1) registers (Table 63 and Table 64) identify the current UART operating configuration and status.

Table 63. UART Status 0 Register (U0STAT0)

BITS	7	6	5	4	3	2	1	0
FIELD	RDA	PE	OE	FE	BRKD	TDRE	TXE	CTS
RESET	0	0	0	0	0	1	1	X
R/W	R	R	R	R	R	R	R	R
ADDR	F41H							

RDA—Receive Data Available

This bit indicates that the UART Receive Data register has received data. Reading the UART Receive Data register clears this bit.

0 = The UART Receive Data register is empty.

1 = There is a byte in the UART Receive Data register.

PE—Parity Error

This bit indicates that a parity error has occurred. Reading the UART Receive Data register clears this bit.

0 = No parity error has occurred.

1 = A parity error has occurred.

OE—Overrun Error

This bit indicates that an overrun error has occurred. An overrun occurs when new data is received and the UART Receive Data register has not been read. If the RDA bit is reset to 0, reading the UART Receive Data register clears this bit.

0 = No overrun error occurred.

1 = An overrun error occurred.

FE—Framing Error

This bit indicates that a framing error (no Stop bit following data reception) was detected. Reading the UART Receive Data register clears this bit.

3. Write to the [ADC Control Register 0](#) to configure the ADC for continuous conversion. The bit fields in the ADC Control register may be written simultaneously:
 - Write to the `ANAIN[3:0]` field to select from the available analog input sources (different input pins available depending on the device).
 - Set `CONT` to 1 to select continuous conversion.
 - If the internal `VREF` must be output to a pin, set the `REFEXT` bit to 1. The internal voltage reference must be enabled in this case.
 - Write the `REFSELL` bit of the pair `{REFSELH, REFSELL}` to select the internal voltage reference level or to disable the internal reference. The `REFSELH` bit is contained in [ADC Control/Status Register 1](#).
 - Set `CEN` to 1 to start the conversions.
4. When the first conversion in continuous operation is complete (after 5129 system clock cycles, plus the 40 cycles for power-up, if necessary), the ADC control logic performs the following operations:
 - `CEN` resets to 0 to indicate the first conversion is complete. `CEN` remains 0 for all subsequent conversions in continuous operation.
 - An interrupt request is sent to the Interrupt Controller to indicate the conversion is complete.
5. The ADC writes a new data result every 256 system clock cycles. For each completed conversion, the ADC control logic performs the following operations:
 - Writes the 13-bit two's complement result to `{ADCD_H[7:0], ADCD_L[7:3]}`.
 - Sends an interrupt request to the Interrupt Controller denoting conversion complete.
6. To disable continuous conversion, clear the `CONT` bit in the ADC Control Register to 0.

Interrupts

The ADC is able to interrupt the CPU when a conversion has been completed. When the ADC is disabled, no new interrupts are asserted; however, an interrupt pending when the ADC is disabled is not cleared.

Calibration and Compensation

The Z8 Encore! XP[®] F082A Series ADC is factory calibrated for offset error and gain error, with the compensation data stored in Flash memory. Alternatively, you can perform your own calibration, storing the values into Flash themselves. Thirdly, the user code can perform a manual offset calibration during DIFFERENTIAL mode operation.

ADC Control Register Definitions

ADC Control Register 0

The ADC Control Register 0 (ADCCTL0) selects the analog input channel and initiates the analog-to-digital conversion. It also selects the voltage reference configuration.

Table 71. ADC Control Register 0 (ADCCTL0)

BITS	7	6	5	4	3	2	1	0
FIELD	CEN	REFSELL	REFOUT	CONT	ANAIN[3:0]			
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F70H							

CEN—Conversion Enable

0 = Conversion is complete. Writing a 0 produces no effect. The ADC automatically clears this bit to 0 when a conversion is complete.

1 = Begin conversion. Writing a 1 to this bit starts a conversion. If a conversion is already in progress, the conversion restarts. This bit remains 1 until the conversion is complete.

REFSELL—Voltage Reference Level Select Low Bit; in conjunction with the High bit (REFSELH) in [ADC Control/Status Register 1](#), this determines the level of the internal voltage reference; the following details the effects of {REFSELH, REFSELL}; note that this reference is independent of the Comparator reference.

00= Internal Reference Disabled, reference comes from external pin

01= Internal Reference set to 1.0 V

10= Internal Reference set to 2.0 V (default)

11= Reserved

REFOUT—Internal Reference Output Enable

0 = Reference buffer is disabled; Vref pin is available for GPIO or analog functions

1 = The internal ADC reference is buffered and driven out to the Vref pin



Warning: When the ADC is used with an external reference ({REFSELH, REFSELL}=00), the REFOUT bit must be set to 0.

CONT

0 = Single-shot conversion. ADC data is output once at completion of the 5129 system clock cycles (measurements of the internal temperature sensor take twice as long)

1 = Continuous conversion. ADC data updated every 256 system clock cycles after an initial 5129 clock conversion (measurements of the internal temperature sensor take twice as long)

```

nop      ; wait for output to settle
clr irq0 ; clear any spurious interrupts pending
ei

```

Comparator Control Register Definitions

Comparator Control Register

The Comparator Control Register (CMP0) configures the comparator inputs and sets the value of the internal voltage reference.

Table 75. Comparator Control Register (CMP0)

BITS	7	6	5	4	3	2	1	0
FIELD	INPSEL	INNSEL	REFLVL				Reserved (20-/28-pin) REFLVL (8-pin)	
RESET	0	0	0	1	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F90H							

INPSEL—Signal Select for Positive Input

0 = GPIO pin used as positive comparator input

1 = temperature sensor used as positive comparator input

INNSEL—Signal Select for Negative Input

0 = internal reference disabled, GPIO pin used as negative comparator input

1 = internal reference enabled as negative comparator input

REFLVL—Internal Reference Voltage Level (this reference is independent of the ADC voltage reference). Note that the 8-pin devices contain two additional LSBs for increased resolution.

For 20-/28-pin devices:

0000 = 0.0 V

0001 = 0.2 V

0010 = 0.4 V

0011 = 0.6 V

0100 = 0.8 V

0101 = 1.0 V (Default)

0110 = 1.2 V

0111 = 1.4 V

1000 = 1.6 V

Operation

The Flash Controller programs and erases Flash memory. The Flash Controller provides the proper Flash controls and timing for Byte Programming, Page Erase, and Mass Erase of Flash memory.

The Flash Controller contains several protection mechanisms to prevent accidental programming or erasure. These mechanisms operate on the page, sector and full-memory levels.

The Flow Chart in [Figure 22](#) displays basic Flash Controller operation. The following subsections provide details about the various operations (Lock, Unlock, Byte Programming, Page Protect, Page Unprotect, Page Select, Page Erase, and Mass Erase) displayed in [Figure 22](#).

Non-Volatile Data Storage

The Z8 Encore! XP[®] F082A Series devices contain a non-volatile data storage (NVDS) element of up to 128 bytes. This memory can perform over 100,000 write cycles.

Operation

The NVDS is implemented by special purpose Zilog[®] software stored in areas of program memory, which are not user-accessible. These special-purpose routines use the Flash memory to store the data. The routines incorporate a dynamic addressing scheme to maximize the write/erase endurance of the Flash.

► **Note:** *Different members of the Z8 Encore! XP F082A Series feature multiple NVDS array sizes. See [Z8 Encore! XP[®] F082A Series Family Part Selection Guide](#) on page 3 for details. Also the members containing 8 KB of Flash memory do not include the NVDS feature.*

NVDS Code Interface

Two routines are required to access the NVDS: a write routine and a read routine. Both of these routines are accessed with a CALL instruction to a pre-defined address outside of the user-accessible program memory. Both the NVDS address and data are single-byte values. Because these routines disturb the working register set, user code must ensure that any required working register values are preserved by pushing them onto the stack or by changing the working register pointer just prior to NVDS execution.

During both read and write accesses to the NVDS, interrupt service is NOT disabled. Any interrupts that occur during the NVDS execution must take care not to disturb the working register and existing stack contents or else the array may become corrupted. Disabling interrupts before executing NVDS operations is recommended.

Use of the NVDS requires 15 bytes of available stack space. Also, the contents of the working register set are overwritten.

For correct NVDS operation, the Flash Frequency Registers must be programmed based on the system clock frequency (see [Flash Operation Timing Using the Flash Frequency Registers](#) on page 145).

Byte Write

To write a byte to the NVDS array, the user code must first push the address, then the data byte onto the stack. The user code issues a CALL instruction to the address of the byte-write routine (0x10B3). At the return from the sub-routine, the write status byte

Table 104. NVDS Read Time (Continued)

Operation	Minimum Latency	Maximum Latency
Read (128 byte array)	883	7609
Write (16 byte array)	4973	5009
Write (64 byte array)	4971	5013
Write (128 byte array)	4984	5023
Illegal Read	43	43
Illegal Write	31	31

If NVDS read performance is critical to your software architecture, there are some things you can do to optimize your code for speed, listed in order from most helpful to least helpful:

- Periodically refresh all addresses that are used. The optimal use of NVDS in terms of speed is to rotate the writes evenly among all addresses planned to use, bringing all reads closer to the minimum read time. Because the minimum read time is much less than the write time, however, actual speed benefits are not always realized.
- Use as few unique addresses as possible: this helps to optimize the impact of refreshing as well as minimize the requirement for it.

Table 108. Oscillator Configuration and Selection

Clock Source	Characteristics	Required Setup
Internal Precision RC Oscillator	<ul style="list-style-type: none"> • 32.8 kHz or 5.53 MHz • High accuracy • No external components required 	<ul style="list-style-type: none"> • Unlock and write Oscillator Control Register (OSCCTL) to enable and select oscillator at either 5.53 MHz or 32.8 kHz
External Crystal/Resonator	<ul style="list-style-type: none"> • 32 kHz to 20 MHz • Very high accuracy (dependent on crystal or resonator used) • Requires external components 	<ul style="list-style-type: none"> • Configure Flash option bits for correct external oscillator mode • Unlock and write OSCCTL to enable crystal oscillator, wait for it to stabilize and select as system clock (if the XTLDIS option bit has been de-asserted, no waiting is required)
External RC Oscillator	<ul style="list-style-type: none"> • 32 kHz to 4 MHz • Accuracy dependent on external components 	<ul style="list-style-type: none"> • Configure Flash option bits for correct external oscillator mode • Unlock and write OSCCTL to enable crystal oscillator and select as system clock
External Clock Drive	<ul style="list-style-type: none"> • 0 to 20 MHz • Accuracy dependent on external clock source 	<ul style="list-style-type: none"> • Write GPIO registers to configure PB3 pin for external clock function • Unlock and write OSCCTL to select external system clock • Apply external clock signal to GPIO
Internal Watchdog Timer Oscillator	<ul style="list-style-type: none"> • 10 kHz nominal • Low accuracy; no external components required • Very low power consumption 	<ul style="list-style-type: none"> • Enable WDT if not enabled and wait until WDT Oscillator is operating. • Unlock and write Oscillator Control Register (OSCCTL) to enable and select oscillator



Caution: *Unintentional accesses to the oscillator control register can actually stop the chip by switching to a non-functioning oscillator. To prevent this condition, the oscillator control block employs a register unlocking/locking scheme.*

OSC Control Register Unlocking/Locking

To write the oscillator control register, unlock it by making two writes to the OSCCTL register with the values E7H followed by 18H. A third write to the OSCCTL register changes the value of the actual register and returns the register to a locked state. Any other sequence of oscillator control register writes has no effect. The values written to unlock the register must be ordered correctly, but are not necessarily consecutive. It is possible to write to or read from other registers within the unlocking/locking operation.



Caution: *It is possible to disable the clock failure detection circuitry as well as all functioning clock sources. In this case, the Z8 Encore! XP F082A Series device ceases functioning and can only be recovered by Power-On-Reset.*

Oscillator Control Register Definitions

Oscillator Control Register

The Oscillator Control Register (OSCCTL) enables/disables the various oscillator circuits, enables/disables the failure detection/recovery circuitry and selects the primary oscillator, which becomes the system clock.

The Oscillator Control Register must be unlocked before writing. Writing the two step sequence E7H followed by 18H to the Oscillator Control Register unlocks it. The register is locked at successful completion of a register write to the OSCCTL.

Table 109. Oscillator Control Register (OSCCTL)

BITS	7	6	5	4	3	2	1	0
FIELD	INTEN	XTLEN	WDTEN	SOFEN	WDFEN	SCKSEL		
RESET	1	0	1	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F86H							

INTEN—Internal Precision Oscillator Enable

1 = Internal precision oscillator is enabled

0 = Internal precision oscillator is disabled

XTLEN—Crystal Oscillator Enable; this setting overrides the GPIO register control for PA0 and PA1

1 = Crystal oscillator is enabled

0 = Crystal oscillator is disabled

WDTEN—Watchdog Timer Oscillator Enable

1 = Watchdog Timer oscillator is enabled

0 = Watchdog Timer oscillator is disabled

SOFEN—System Clock Oscillator Failure Detection Enable

1 = Failure detection and recovery of system clock oscillator is enabled

0 = Failure detection and recovery of system clock oscillator is disabled

Assembly Language Syntax

For proper instruction execution, eZ8 CPU assembly language syntax requires that the operands be written as ‘destination, source’. After assembly, the object code usually has the operands in the order ‘source, destination’, but ordering is opcode-dependent. The following instruction examples illustrate the format of some basic assembly instructions and the resulting object code produced by the assembler. This binary format must be followed if manual program coding is preferred or if you intend to implement your own assembler.

Example 1: If the contents of Registers 43H and 08H are added and the result is stored in 43H, the assembly syntax and resulting object code is:

Table 112. Assembly Language Syntax Example 1

Assembly Language Code	ADD	43H,	08H	(ADD dst, src)
Object Code	04	08	43	(OPC src, dst)

Example 2: In general, when an instruction format requires an 8-bit register address, that address can specify any register location in the range 0–255 or, using Escaped Mode Addressing, a Working Register R0–R15. If the contents of Register 43H and Working Register R8 are added and the result is stored in 43H, the assembly syntax and resulting object code is:

Table 113. Assembly Language Syntax Example 2

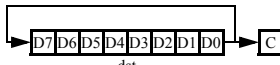
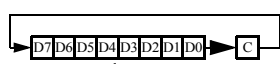
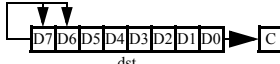
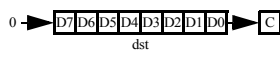
Assembly Language Code	ADD	43H,	R8	(ADD dst, src)
Object Code	04	E8	43	(OPC src, dst)

See the device-specific Product Specification to determine the exact register file range available. The register file size varies, depending on the device type.

eZ8 CPU Instruction Notation

In the eZ8 CPU Instruction Summary and Description sections, the operands, condition codes, status flags, and address modes are represented by a notational shorthand that is described in [Table 114](#).

Table 124. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
RR dst		R		E0	*	*	*	*	–	–	2	2
		IR		E1							2	3
RRC dst		R		C0	*	*	*	*	–	–	2	2
		IR		C1							2	3
SBC dst, src	$dst \leftarrow dst - src - C$	r	r	32	*	*	*	*	1	*	2	3
		r	lr	33							2	4
		R	R	34							3	3
		R	IR	35							3	4
		R	IM	36							3	3
		IR	IM	37							3	4
SBCX dst, src	$dst \leftarrow dst - src - C$	ER	ER	38	*	*	*	*	1	*	4	3
		ER	IM	39							4	3
SCF	$C \leftarrow 1$			DF	1	–	–	–	–	–	1	2
SRA dst		R		D0	*	*	*	0	–	–	2	2
		IR		D1							2	3
SRL dst		R		1F C0	*	*	0	*	–	–	3	2
		IR		1F C1							3	3
SRP src	$RP \leftarrow src$		IM	01	–	–	–	–	–	–	2	2
STOP	STOP Mode			6F	–	–	–	–	–	–	1	2
SUB dst, src	$dst \leftarrow dst - src$	r	r	22	*	*	*	*	1	*	2	3
		r	lr	23							2	4
		R	R	24							3	3
		R	IR	25							3	4
		R	IM	26							3	3
		IR	IM	27							3	4
Flags Notation:		* = Value is a function of the result of the operation. – = Unaffected X = Undefined				0 = Reset to 0 1 = Set to 1						

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP[®] F082A Series with 4 KB Flash, 10-Bit Analog-to-Digital Converter											
Standard Temperature: 0 °C to 70 °C											
Z8F042APB020SC	4 KB	1 KB	128 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F042AQB020SC	4 KB	1 KB	128 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F042ASB020SC	4 KB	1 KB	128 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F042ASH020SC	4 KB	1 KB	128 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F042AHH020SC	4 KB	1 KB	128 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F042APH020SC	4 KB	1 KB	128 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F042ASJ020SC	4 KB	1 KB	128 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F042AHJ020SC	4 KB	1 KB	128 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F042APJ020SC	4 KB	1 KB	128 B	23	20	2	8	1	1	1	PDIP 28-pin package
Extended Temperature: -40 °C to 105 °C											
Z8F042APB020EC	4 KB	1 KB	128 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F042AQB020EC	4 KB	1 KB	128 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F042ASB020EC	4 KB	1 KB	128 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F042ASH020EC	4 KB	1 KB	128 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F042AHH020EC	4 KB	1 KB	128 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F042APH020EC	4 KB	1 KB	128 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F042ASJ020EC	4 KB	1 KB	128 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F042AHJ020EC	4 KB	1 KB	128 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F042APJ020EC	4 KB	1 KB	128 B	23	20	2	8	1	1	1	PDIP 28-pin package
Replace C with G for Lead-Free Packaging											

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP[®] F082A Series with 2 KB Flash											
Standard Temperature: 0 °C to 70 °C											
Z8F021APB020SC	2 KB	512 B	64 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F021AQB020SC	2 KB	512 B	64 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F021ASB020SC	2 KB	512 B	64 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F021ASH020SC	2 KB	512 B	64 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F021AHH020SC	2 KB	512 B	64 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F021APH020SC	2 KB	512 B	64 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F021ASJ020SC	2 KB	512 B	64 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F021AHJ020SC	2 KB	512 B	64 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F021APJ020SC	2 KB	512 B	64 B	25	19	2	0	1	1	0	PDIP 28-pin package
Extended Temperature: -40 °C to 105 °C											
Z8F021APB020EC	2 KB	512 B	64 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F021AQB020EC	2 KB	512 B	64 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F021ASB020EC	2 KB	512 B	64 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F021ASH020EC	2 KB	512 B	64 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F021AHH020EC	2 KB	512 B	64 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F021APH020EC	2 KB	512 B	64 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F021ASJ020EC	2 KB	512 B	64 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F021AHJ020EC	2 KB	512 B	64 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F021APJ020EC	2 KB	512 B	64 B	25	19	2	0	1	1	0	PDIP 28-pin package
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