# Zilog - Z8F012ASJ020SC00TR Datasheet

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | eZ8 |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | IrDA, UART/USART |
| Peripherals | Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT |
| Number of I/O | 23 |
| Program Memory Size | 1KB (1K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 16 x 8 |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8f012asj020sc00tr |

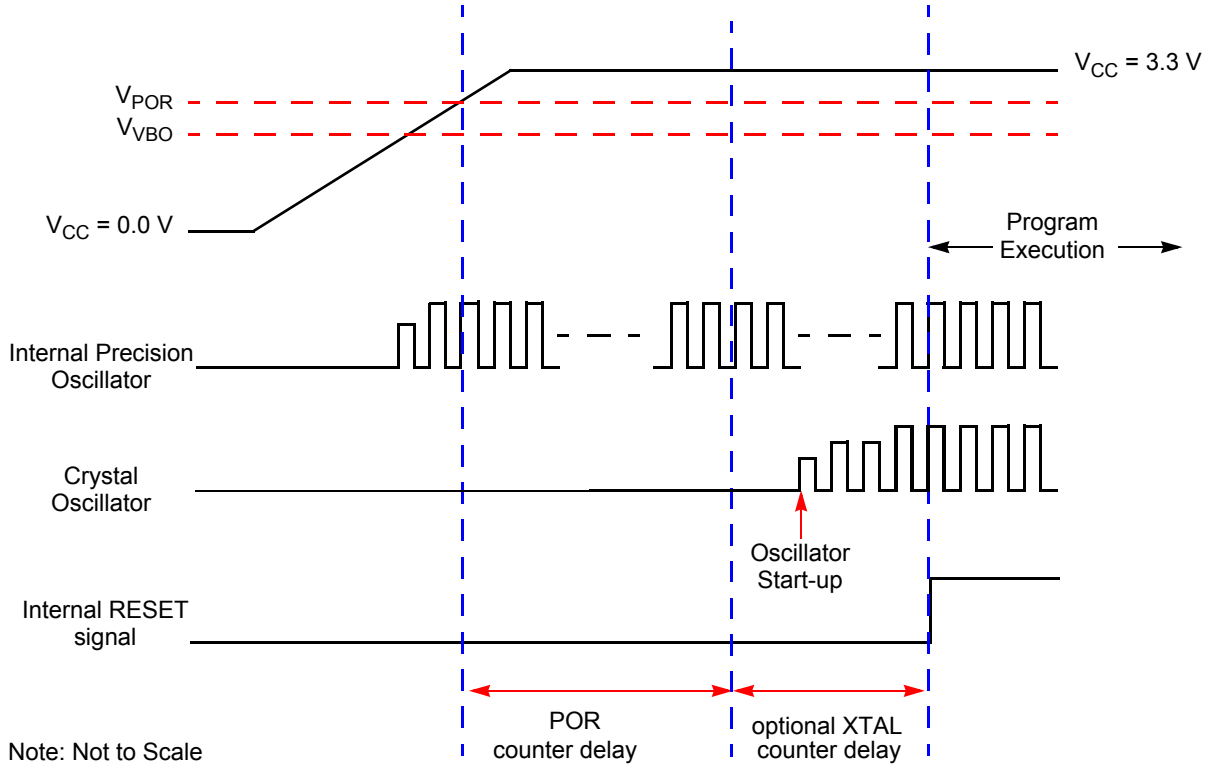



**Figure 5. Power-On Reset Operation**

## Voltage Brownout Reset

The devices in the Z8 Encore! XP F082A Series provide low Voltage Brownout (VBO) protection. The VBO circuit senses when the supply voltage drops to an unsafe level (below the VBO threshold voltage) and forces the device into the Reset state. While the supply voltage remains below the Power-On Reset voltage threshold ($V_{POR}$), the VBO block holds the device in the Reset.

After the supply voltage again exceeds the Power-On Reset voltage threshold, the device progresses through a full System Reset sequence, as described in the Power-On Reset section. Following Power-On Reset, the POR status bit in the Reset Status (RSTSTAT) register is set to 1. Figure 6 displays Voltage Brownout operation. See Electrical Characteristics on page 221 for the VBO and POR threshold voltages ($V_{VBO}$ and $V_{POR}$).

The Voltage Brownout circuit can be either enabled or disabled during STOP mode. Operation during STOP mode is set by the VBO_AO Flash Option Bit. See Flash Option Bits for information about configuring VBO_AO.

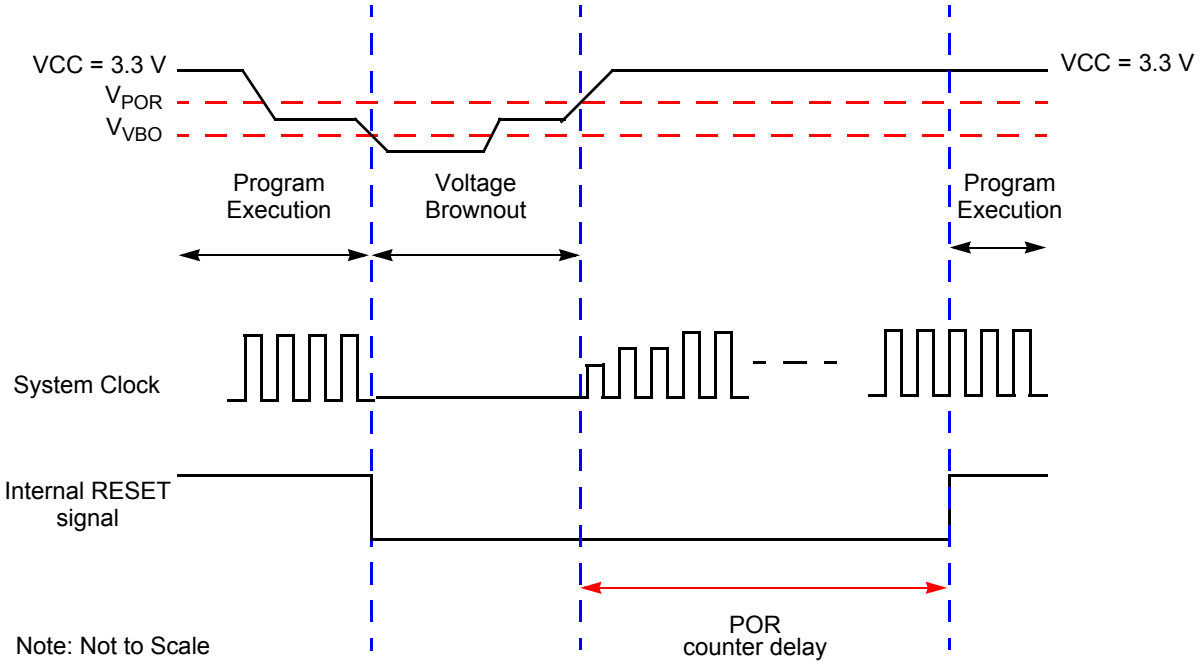



**Figure 6. Voltage Brownout Reset Operation**

The POR level is greater than the VBO level by the specified hysteresis value. This ensures that the device undergoes a Power-On Reset after recovering from a VBO condition.

## Watchdog Timer Reset

If the device is in NORMAL or HALT mode, the Watchdog Timer can initiate a System Reset at time-out if the WDT_RES Flash Option Bit is programmed to 1. This is the unprogrammed state of the WDT_RES Flash Option Bit. If the bit is programmed to 0, it configures the Watchdog Timer to cause an interrupt, not a System Reset, at time-out.

The WDT bit in the Reset Status (RSTSTAT) register is set to signify that the reset was initiated by the Watchdog Timer.

## External Reset Input

The $\overline{\text{RESET}}$ pin has a Schmitt-Triggered input and an internal pull-up resistor. Once the $\overline{\text{RESET}}$ pin is asserted for a minimum of four system clock cycles, the device progresses through the System Reset sequence. Because of the possible asynchronicity of the system clock and reset signals, the required reset duration may be as short as three clock periods

Reserved—Must be 0.

C3ENL—Port C3 Interrupt Request Enable Low Bit
C2ENL—Port C2 Interrupt Request Enable Low Bit
C1ENL—Port C1 Interrupt Request Enable Low Bit
C0ENL—Port C0 Interrupt Request Enable Low Bit

## Interrupt Edge Select Register

The Interrupt Edge Select (IRQES) register (Table 45) determines whether an interrupt is generated for the rising edge or falling edge on the selected GPIO Port A input pin.

**Table 45. Interrupt Edge Select Register (IRQES)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | IES7 | IES6 | IES5 | IES4 | IES3 | IES2 | IES1 | IES0 |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| ADDR | FCDH | | | | | | | |

IES*x*—Interrupt Edge Select *x*
0 = An interrupt request is generated on the falling edge of the PA*x* input.
1 = An interrupt request is generated on the rising edge of the PA*x* input.
where *x* indicates the specific GPIO Port pin number (0 through 7).

## Shared Interrupt Select Register

The Shared Interrupt Select (IRQSS) register (Table 46) determines the source of the PADxS interrupts. The Shared Interrupt Select register selects between Port A and alternate sources for the individual interrupts.

Because these shared interrupts are edge-triggered, it is possible to generate an interrupt just by switching from one shared source to another. For this reason, an interrupt must be disabled before switching between sources.

# Watchdog Timer

The Watchdog Timer (WDT) protects against corrupt or unreliable software, power faults, and other system-level problems which may place the Z8 Encore! XP® F082A Series devices into unsuitable operating states. The features of Watchdog Timer include:

- On-chip RC oscillator.
- A selectable time-out response: reset or interrupt.
- 24-bit programmable time-out value.

## Operation

The Watchdog Timer is a one-shot timer that resets or interrupts the Z8 Encore! XP F082A Series devices when the WDT reaches its terminal count. The Watchdog Timer uses a dedicated on-chip RC oscillator as its clock source. The Watchdog Timer operates in only two modes: ON and OFF. Once enabled, it always counts and must be refreshed to prevent a time-out. Perform an enable by executing the WDT instruction or by setting the WDT_AO Flash Option Bit. The WDT_AO bit forces the Watchdog Timer to operate immediately upon reset, even if a WDT instruction has not been executed.

The Watchdog Timer is a 24-bit reloadable downcounter that uses three 8-bit registers in the eZ8 CPU register space to set the reload value. The nominal WDT time-out period is described by the following equation:

$$\text{WDT Time-out Period (ms)} = \frac{\text{WDT Reload Value}}{10}$$

where the WDT reload value is the decimal value of the 24-bit value given by {WDTU[7:0], WDTH[7:0], WDTL[7:0]} and the typical Watchdog Timer RC oscillator frequency is 10 kHz. The Watchdog Timer cannot be refreshed after it reaches 000002H. The WDT Reload Value must not be set to values below 000004H. Table 56 provides information about approximate time-out delays for the minimum and maximum WDT reload values.

**Table 56. Watchdog Timer Approximate Time-Out Delays**

| WDT Reload Value (Hex) | WDT Reload Value (Decimal) | Approximate Time-Out Delay (with 10 kHz typical WDT oscillator frequency) | |
|---|---|---|---|
| | | Typical | Description |
| 000004 | 4 | 400 µs | Minimum time-out delay |
| FFFFFF | 16,777,215 | 28 minutes | Maximum time-out delay |

# ADC Control Register Definitions

## ADC Control Register 0

The ADC Control Register 0 (ADCCTL0) selects the analog input channel and initiates the analog-to-digital conversion. It also selects the voltage reference configuration.

**Table 71. ADC Control Register 0 (ADCCTL0)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | CEN | REFSELL | REFOUT | CONT | ANAIN[3:0] | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| ADDR | F70H | | | | | | | |

CEN—Conversion Enable
0 = Conversion is complete. Writing a 0 produces no effect. The ADC automatically clears this bit to 0 when a conversion is complete.
1 = Begin conversion. Writing a 1 to this bit starts a conversion. If a conversion is already in progress, the conversion restarts. This bit remains 1 until the conversion is complete.

REFSELL—Voltage Reference Level Select Low Bit; in conjunction with the High bit (REFSELH) in ADC Control/Status Register 1, this determines the level of the internal voltage reference; the following details the effects of {REFSELH, REFSELL}; note that this reference is independent of the Comparator reference.
00= Internal Reference Disabled, reference comes from external pin
01= Internal Reference set to 1.0 V
10= Internal Reference set to 2.0 V (default)
11= Reserved

REFOUT—Internal Reference Output Enable
0 = Reference buffer is disabled; Vref pin is available for GPIO or analog functions
1 = The internal ADC reference is buffered and driven out to the Vref pin

**Warning:** *When the ADC is used with an external reference ({REFSELH,REFSELL}=00), the REFOUT bit must be set to 0.*

CONT
0 = Single-shot conversion. ADC data is output once at completion of the 5129 system clock cycles (measurements of the internal temperature sensor take twice as long)
1 = Continuous conversion. ADC data updated every 256 system clock cycles after an initial 5129 clock conversion (measurements of the internal temperature sensor take twice as long)

## Flash Operation Timing Using the Flash Frequency Registers

Before performing either a program or erase operation on Flash memory, you must first configure the Flash Frequency High and Low Byte registers. The Flash Frequency registers allow programming and erasing of the Flash with system clock frequencies ranging from 32 kHz (32768 Hz) through 20 MHz.

The Flash Frequency High and Low Byte registers combine to form a 16-bit value, FFREQ, to control timing for Flash program and erase operations. The 16-bit binary Flash Frequency value must contain the system clock frequency (in kHz). This value is calculated using the following equation:

$$\text{FFREQ[15:0]} = \frac{\text{System Clock Frequency (Hz)}}{1000}$$

**Caution:** *Flash programming and erasure are not supported for system clock frequencies below 32 kHz (32768 Hz) or above 20 MHz. The Flash Frequency High and Low Byte registers must be loaded with the correct value to ensure operation of the Z8 Encore! XP® F082A Series devices.*

## Flash Code Protection Against External Access

The user code contained within the Flash memory can be protected against external access by the on-chip debugger. Programming the FRP Flash Option Bit prevents reading of the user code with the On-Chip Debugger. See Flash Option Bits on page 153 and On-Chip Debugger on page 173 for more information.

## Flash Code Protection Against Accidental Program and Erasure

The Z8 Encore! XP F082A Series provides several levels of protection against accidental program and erasure of the Flash memory contents. This protection is provided by a combination of the Flash Option bits, the register locking mechanism, the page select redundancy and the sector level protection control of the Flash Controller.

### Flash Code Protection Using the Flash Option Bits

The FRP and FWP Flash Option Bits combine to provide three levels of Flash Program Memory protection as listed in Table 77. See Flash Option Bits on page 153 for more information.

**Table 77. Flash Code Protection Using the Flash Option Bits**

| FWP | Flash Code Protection Description |
|---|---|
| 0 | Programming and erasing disabled for all of Flash Program Memory. In user code programming, Page Erase, and Mass Erase are all disabled. Mass Erase is available through the On-Chip Debugger. |
| 1 | Programming, Page Erase, and Mass Erase are enabled for all of Flash Program Memory. |

### Flash Code Protection Using the Flash Controller

At Reset, the Flash Controller locks to prevent accidental program or erasure of the Flash memory. To program or erase the Flash memory, first write the Page Select Register with the target page. Unlock the Flash Controller by making two consecutive writes to the Flash Control register with the values 73H and 8CH, sequentially. The Page Select Register must be rewritten with the target page. If the two Page Select writes do not match, the controller reverts to a locked state. If the two writes match, the selected page becomes active. See Figure 22 on page 144 for details.

After unlocking a specific page, you can enable either Page Program or Erase. Writing the value 95H causes a Page Erase only if the active page resides in a sector that is not protected. Any other value written to the Flash Control register locks the Flash Controller. Mass Erase is not allowed in the user code but only in through the Debug Port.

After unlocking a specific page, you can also write to any byte on that page. After a byte is written, the page remains unlocked, allowing for subsequent writes to other bytes on the same page. Further writes to the Flash Control Register cause the active page to revert to a locked state.

### Sector Based Flash Protection

The final protection mechanism is implemented on a per-sector basis. The Flash memories of Z8 Encore!® devices are divided into at most 8 sectors. A sector is 1/8 of the total size of the Flash memory, unless this value is smaller than the page size, in which case the sector and page sizes are equal.

The Sector Protect register controls the protection state of each Flash sector. This register is shared with the Page Select Register. It is accessed by writing 73H followed by 5EH to the Flash controller. The next write to the Flash Control Register targets the Sector Protect Register.

The Sector Protect Register is initialized to 0 on reset, putting each sector into an unprotected state. When a bit in the Sector Protect Register is written to 1, the corresponding sector is no longer written or erased by the CPU. External Flash programming through

### Trim Bit Data Register

The Trim Bid Data (TRMDR) register contains the read or write data for access to the trim option bits (Table 85).

**Table 85. Trim Bit Data Register (TRMDR)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | TRMDR - Trim Bit Data | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| ADDR | FF7H | | | | | | | |

## Flash Option Bit Address Space

The first two bytes of Flash program memory at addresses 0000H and 0001H are reserved for the user-programmable Flash option bits.

### Flash Program Memory Address 0000H

**Table 86. Flash Option Bits at Program Memory Address 0000H**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | WDT_RES | WDT_AO | OSC_SEL[1:0] | | VBO_AO | FRP | Reserved | FWP |
| RESET | U | U | U | U | U | U | U | U |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| ADDR | Program Memory 0000H | | | | | | | |

**Note:** U = Unchanged by Reset. R/W = Read/Write.

WDT_RES—Watchdog Timer Reset
0 = Watchdog Timer time-out generates an interrupt request. Interrupts must be globally enabled for the eZ8 CPU to acknowledge the interrupt request.
1 = Watchdog Timer time-out causes a system reset. This setting is the default for unprogrammed (erased) Flash.

WDT_AO—Watchdog Timer Always On
0 = Watchdog Timer is automatically enabled upon application of system power. Watchdog Timer can not be disabled.

**Table 94. ADC Calibration Data Location**

| Info Page Address | Memory Address | Compensation Usage | ADC Mode | Reference Type |
|---|---|---|---|---|
| 60 | FE60 | Offset | Single-Ended Unbuffered | Internal 2.0 V |
| 08 | FE08 | Gain High Byte | Single-Ended Unbuffered | Internal 2.0 V |
| 09 | FE09 | Gain Low Byte | Single-Ended Unbuffered | Internal 2.0 V |
| 63 | FE63 | Offset | Single-Ended Unbuffered | Internal 1.0 V |
| 0A | FE0A | Gain High Byte | Single-Ended Unbuffered | Internal 1.0 V |
| 0B | FE0B | Gain Low Byte | Single-Ended Unbuffered | Internal 1.0 V |
| 66 | FE66 | Offset | Single-Ended Unbuffered | External 2.0 V |
| 0C | FE0C | Gain High Byte | Single-Ended Unbuffered | External 2.0 V |
| 0D | FE0D | Gain Low Byte | Single-Ended Unbuffered | External 2.0 V |
| 69 | FE69 | Offset | Single-Ended 1x Buffered | Internal 2.0 V |
| 0E | FE0E | Gain High Byte | Single-Ended 1x Buffered | Internal 2.0 V |
| 0F | FE0F | Gain Low Byte | Single-Ended 1x Buffered | Internal 2.0 V |
| 6C | FE6C | Offset | Single-Ended 1x Buffered | External 2.0 V |
| 10 | FE10 | Gain High Byte | Single-Ended 1x Buffered | External 2.0 V |
| 11 | FE11 | Gain Low Byte | Single-Ended 1x Buffered | External 2.0 V |
| 6F | FE6F | Offset | Differential Unbuffered | Internal 2.0 V |
| 12 | FE12 | Positive Gain High Byte | Differential Unbuffered | Internal 2.0 V |
| 13 | FE13 | Positive Gain Low Byte | Differential Unbuffered | Internal 2.0 V |
| 30 | FE30 | Negative Gain High Byte | Differential Unbuffered | Internal 2.0 V |
| 31 | FE31 | Negative Gain Low Byte | Differential Unbuffered | Internal 2.0 V |
| 72 | FE72 | Offset | Differential Unbuffered | Internal 1.0 V |
| 14 | FE14 | Positive Gain High Byte | Differential Unbuffered | Internal 1.0 V |
| 15 | FE15 | Positive Gain Low Byte | Differential Unbuffered | Internal 1.0 V |
| 32 | FE32 | Negative Gain High Byte | Differential Unbuffered | Internal 1.0 V |
| 33 | FE33 | Negative Gain Low Byte | Differential Unbuffered | Internal 1.0 V |
| 75 | FE75 | Offset | Differential Unbuffered | External 2.0 V |
| 16 | FE16 | Positive Gain High Byte | Differential Unbuffered | External 2.0 V |
| 17 | FE17 | Positive Gain Low Byte | Differential Unbuffered | External 2.0 V |

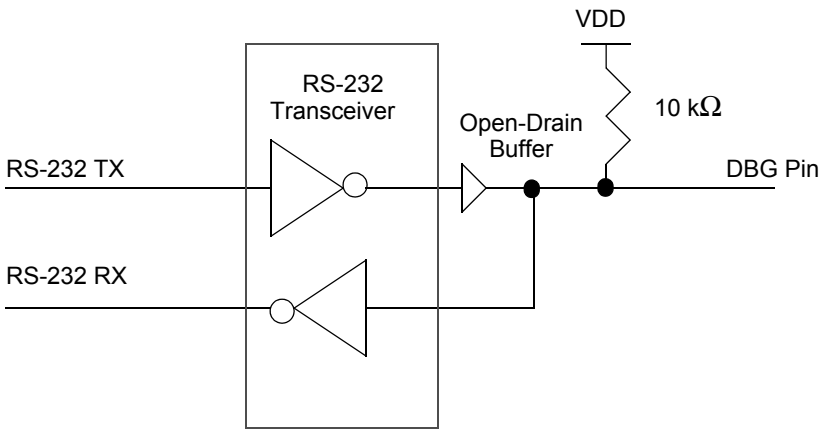



**Figure 25. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface (2)**

## DEBUG Mode

The operating characteristics of the devices in DEBUG mode are:

- The eZ8 CPU fetch unit stops, idling the eZ8 CPU, unless directed by the OCD to execute specific instructions.
- The system clock operates unless in STOP mode.
- All enabled on-chip peripherals operate unless in STOP mode.
- Automatically exits HALT mode.
- Constantly refreshes the Watchdog Timer, if enabled.

### Entering DEBUG Mode

The operating characteristics of the devices entering DEBUG mode are:

- The device enters DEBUG mode after the eZ8 CPU executes a BRK (Breakpoint) instruction.
- If the DBG pin is held Low during the final clock cycle of system reset, the part enters DEBUG mode immediately (20-/28-pin products only).

**Note:** *Holding the DBG pin Low for an additional 5000 (minimum) clock cycles after reset (making sure to account for any specified frequency error if using an internal oscillator) prevents a false interpretation of an Autobaud sequence (see* OCD Auto-Baud Detector/ Generator *on page 176).*

# Crystal Oscillator

The products in the Z8 Encore! XP® F082A Series contain an on-chip crystal oscillator for use with external crystals with 32 kHz to 20 MHz frequencies. In addition, the oscillator supports external RC networks with oscillation frequencies up to 4 MHz or ceramic resonators with frequencies up to 8 MHz. The on-chip crystal oscillator can be used to generate the primary system clock for the internal eZ8 CPU and the majority of the on-chip peripherals. Alternatively, the $X_{IN}$ input pin can also accept a CMOS-level clock input signal (32 kHz–20 MHz). If an external clock generator is used, the $X_{OUT}$ pin must be left unconnected. The Z8 Encore! XP F082A Series products do not contain an internal clock divider. The frequency of the signal on the $X_{IN}$ input pin determines the frequency of the system clock.

**Note:** *Although the XIN pin can be used as an input for an external clock generator, the CLKIN pin is better suited for such use (see* System Clock Selection *on page 187**).*

## Operating Modes

The Z8 Encore! XP F082A Series products support four oscillator modes:

- Minimum power for use with very low frequency crystals (32 kHz–1 MHz).
- Medium power for use with medium frequency crystals or ceramic resonators (0.5 MHz to 8 MHz).
- Maximum power for use with high frequency crystals (8 MHz to 20 MHz).
- On-chip oscillator configured for use with external RC networks (<4 MHz).

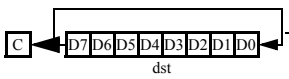
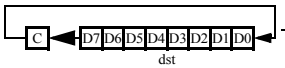
The oscillator mode is selected using user-programmable Flash Option Bits. See Flash Option Bits on page 153 for information.

## Crystal Oscillator Operation

The Flash Option bit XTLDIS controls whether the crystal oscillator is enabled during reset. The crystal may later be disabled after reset if a new oscillator has been selected as the system clock. If the crystal is manually enabled after reset through the OSCCTL register, the user code must wait at least 1000 crystal oscillator cycles for the crystal to stabilize. After this, the crystal oscillator may be selected as the system clock.

**Note:** *The stabilization time varies depending on the crystal or resonator used, as well as on the feedback network. See* Table 111 *for transconductance values to compute oscillator stabilization times.*

**Table 124. eZ8 CPU Instruction Summary (Continued)**

| Assembly Mnemonic | Symbolic Operation | Address Mode dst | Address Mode src | Opcode(s) (Hex) | Flags C | Z | S | V | D | H | Fetch Cycles | Instr. Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OR dst, src | dst ← dst OR src | r | r | 42 | – | * | * | 0 | – | – | 2 | 3 |
| | | r | Ir | 43 | | | | | | | 2 | 4 |
| | | R | R | 44 | | | | | | | 3 | 3 |
| | | R | IR | 45 | | | | | | | 3 | 4 |
| | | R | IM | 46 | | | | | | | 3 | 3 |
| | | IR | IM | 47 | | | | | | | 3 | 4 |
| ORX dst, src | dst ← dst OR src | ER | ER | 48 | – | * | * | 0 | – | – | 4 | 3 |
| | | ER | IM | 49 | | | | | | | 4 | 3 |
| POP dst | dst ← @SP<br>SP ← SP + 1 | R | | 50 | – | – | – | – | – | – | 2 | 2 |
| | | IR | | 51 | | | | | | | 2 | 3 |
| POPX dst | dst ← @SP<br>SP ← SP + 1 | ER | | D8 | – | – | – | – | – | – | 3 | 2 |
| PUSH src | SP ← SP – 1<br>@SP ← src | R | | 70 | – | – | – | – | – | – | 2 | 2 |
| | | IR | | 71 | | | | | | | 2 | 3 |
| | | IM | | IF70 | | | | | | | 3 | 2 |
| PUSHX src | SP ← SP – 1<br>@SP ← src | ER | | C8 | – | – | – | – | – | – | 3 | 2 |
| RCF | C ← 0 | | | CF | 0 | – | – | – | – | – | 1 | 2 |
| RET | PC ← @SP<br>SP ← SP + 2 | | | AF | – | – | – | – | – | – | 1 | 4 |
| RL dst |  | R | | 90 | * | * | * | * | – | – | 2 | 2 |
| | | IR | | 91 | | | | | | | 2 | 3 |
| RLC dst |  | R | | 10 | * | * | * | * | – | – | 2 | 2 |
| | | IR | | 11 | | | | | | | 2 | 3 |

| Flags Notation: | * = Value is a function of the result of the operation.<br>– = Unaffected<br>X = Undefined | 0 = Reset to 0<br>1 = Set to 1 |
|---|---|---|

**Table 128. Power Consumption (Continued)**

| | | $V_{DD}$ = 2.7 V to 3.6 V | | | | |
|---|---|---|---|---|---|---|
| | | | Maximum[2] | Maximum[3] | | |
| **Symbol** | **Parameter** | **Typical[1]** | **Std Temp** | **Ext Temp** | **Units** | **Conditions** |
| $I_{DD}$ LPO | Low-Power Operational Amplifier Supply Current | 3 | 5 | 5 | µA | Driving a high-impedance load |
| $I_{DD}$ TS | Temperature Sensor Supply Current | 60 | | | µA | See Notes 4 |
| $I_{DD}$ BG | Band Gap Supply Current | 320 | 480 | 500 | µA | For 20-/28-pin devices |
| | | | | | | For 8-pin devices |

**Notes**
1. Typical conditions are defined as $V_{DD}$ = 3.3 V and +30 °C.
2. Standard temperature is defined as $T_A$ = 0 °C to +70 °C; these values not tested in production for worst case behavior, but are derived from product characterization and provided for design guidance only.
3. Extended temperature is defined as $T_A$ = -40 °C to +105 °C; these values not tested in production for worst case behavior, but are derived from product characterization and provided for design guidance only.
4. For this block to operate, the bandgap circuit is automatically turned on and must be added to the total supply current. This bandgap current is only added once, regardless of how many peripherals are using it.

**Table 138. Temperature Sensor Electrical Characteristics**

| | | $V_{DD}$ = 2.7 V to 3.6 V | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Typical** | **Maximum** | **Units** | **Conditions** |
| $T_{AERR}$ | Temperature Error | | ±0.5 | ±2 | °C | Over the range +20 °C to +30 °C (as measured by ADC)[1] |
| | | | ±1 | ±5 | °C | Over the range +0 °C to +70 °C (as measured by ADC) |
| | | | ±2 | ±7 | °C | Over the range +0 °C to +105 °C (as measured by ADC) |
| | | | ±7 | | °C | Over the range -40 °C to +105 °C (as measured by ADC) |
| $T_{AERR}$ | Temperature Error | | TBD | | °C | Over the range -40 °C to +105 °C (as measured by comparator) |
| $t_{WAKE}$ | Wakeup Time | | 80 | 100 | µs | Time required for Temperature Sensor to stabilize after enabling |

[1]Devices are factory calibrated at for maximal accuracy between +20 °C and +30 °C, so the sensor is maximally accurate in that range. User re-calibration for a different temperature range is possible and increases accuracy near the new calibration point.

## General Purpose I/O Port Input Data Sample Timing

Figure 34 displays timing of the GPIO Port input sampling. The input value on a GPIO Port pin is sampled on the rising edge of the system clock. The Port value is available to the eZ8 CPU on the second rising clock edge following the change of the Port value.

| Part Number | Flash | RAM | NVDS | I/O Lines | Interrupts | 16-Bit Timers w/PWM | 10-Bit A/D Channels | UART with IrDA | Comparator | Temperature Sensor | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Z8 Encore! XP® F082A Series with 4 KB Flash, 10-Bit Analog-to-Digital Converter** | | | | | | | | | | | |
| **Standard Temperature: 0 °C to 70 °C** | | | | | | | | | | | |
| Z8F042APB020SC | 4 KB | 1 KB | 128 B | 6 | 14 | 2 | 4 | 1 | 1 | 1 | PDIP 8-pin package |
| Z8F042AQB020SC | 4 KB | 1 KB | 128 B | 6 | 14 | 2 | 4 | 1 | 1 | 1 | QFN 8-pin package |
| Z8F042ASB020SC | 4 KB | 1 KB | 128 B | 6 | 14 | 2 | 4 | 1 | 1 | 1 | SOIC 8-pin package |
| Z8F042ASH020SC | 4 KB | 1 KB | 128 B | 17 | 20 | 2 | 7 | 1 | 1 | 1 | SOIC 20-pin package |
| Z8F042AHH020SC | 4 KB | 1 KB | 128 B | 17 | 20 | 2 | 7 | 1 | 1 | 1 | SSOP 20-pin package |
| Z8F042APH020SC | 4 KB | 1 KB | 128 B | 17 | 20 | 2 | 7 | 1 | 1 | 1 | PDIP 20-pin package |
| Z8F042ASJ020SC | 4 KB | 1 KB | 128 B | 23 | 20 | 2 | 8 | 1 | 1 | 1 | SOIC 28-pin package |
| Z8F042AHJ020SC | 4 KB | 1 KB | 128 B | 23 | 20 | 2 | 8 | 1 | 1 | 1 | SSOP 28-pin package |
| Z8F042APJ020SC | 4 KB | 1 KB | 128 B | 23 | 20 | 2 | 8 | 1 | 1 | 1 | PDIP 28-pin package |
| **Extended Temperature: -40 °C to 105 °C** | | | | | | | | | | | |
| Z8F042APB020EC | 4 KB | 1 KB | 128 B | 6 | 14 | 2 | 4 | 1 | 1 | 1 | PDIP 8-pin package |
| Z8F042AQB020EC | 4 KB | 1 KB | 128 B | 6 | 14 | 2 | 4 | 1 | 1 | 1 | QFN 8-pin package |
| Z8F042ASB020EC | 4 KB | 1 KB | 128 B | 6 | 14 | 2 | 4 | 1 | 1 | 1 | SOIC 8-pin package |
| Z8F042ASH020EC | 4 KB | 1 KB | 128 B | 17 | 20 | 2 | 7 | 1 | 1 | 1 | SOIC 20-pin package |
| Z8F042AHH020EC | 4 KB | 1 KB | 128 B | 17 | 20 | 2 | 7 | 1 | 1 | 1 | SSOP 20-pin package |
| Z8F042APH020EC | 4 KB | 1 KB | 128 B | 17 | 20 | 2 | 7 | 1 | 1 | 1 | PDIP 20-pin package |
| Z8F042ASJ020EC | 4 KB | 1 KB | 128 B | 23 | 20 | 2 | 8 | 1 | 1 | 1 | SOIC 28-pin package |
| Z8F042AHJ020EC | 4 KB | 1 KB | 128 B | 23 | 20 | 2 | 8 | 1 | 1 | 1 | SSOP 28-pin package |
| Z8F042APJ020EC | 4 KB | 1 KB | 128 B | 23 | 20 | 2 | 8 | 1 | 1 | 1 | PDIP 28-pin package |
| Replace C with G for Lead-Free Packaging | | | | | | | | | | | |