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Zilog - Z8F021AHJ020SC00TR Datasheet



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Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f021ahj020sc00tr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



CPU and Peripheral Overview

eZ8 CPU Features

The eZ8 CPU, Zilog's latest 8-bit Central Processing Unit (CPU), meets the continuing demand for faster and more code-efficient microcontrollers. The eZ8 CPU executes a superset of the original $Z8^{\text{(P)}}$ instruction set. The features of eZ8 CPU include:

- Direct register-to-register architecture allows each register to function as an accumulator, improving execution time and decreasing the required program memory.
- Software stack allows much greater depth in subroutine calls and interrupts than hardware stacks.
- Compatible with existing Z8 code.
- Expanded internal Register File allows access of up to 4 KB.
- New instructions improve execution efficiency for code developed using higherlevel programming languages, including C.
- Pipelined instruction fetch and execution.
- New instructions for improved performance including BIT, BSWAP, BTJ, CPC, LDC, LDCI, LEA, MULT, and SRL.
- New instructions support 12-bit linear addressing of the Register File.
- Up to 10 MIPS operation.
- C-Compiler friendly.
- 2 to 9 clock cycles per instruction.

For more information on eZ8 CPU, refer to eZ8 CPU Core User Manual (UM0128) available for download at <u>www.zilog.com</u>.

10-Bit Analog-to-Digital Converter

The optional analog-to-digital converter (ADC) converts an analog input signal to a 10-bit binary number. The ADC accepts inputs from eight different analog input pins in both single-ended and differential modes. The ADC also features a unity gain buffer when high input impedance is required.



Universal Asynchronous Receiver/Transmitter

The full-duplex universal asynchronous receiver/transmitter (UART) is included in all Z8 Encore! XP package types. The UART supports 8- and 9-bit data modes and selectable parity. The UART also supports multi-drop address processing in hardware. The UART baud rate generator (BRG) can be configured and used as a basic 16-bit timer.

Timers

Two enhanced 16-bit reloadable timers can be used for timing/counting events or for motor control operations. These timers provide a 16-bit programmable reload counter and operate in ONE-SHOT, CONTINUOUS, GATED, CAPTURE, CAPTURE RESTART, COMPARE, CAPTURE and COMPARE, PWM SINGLE OUTPUT and PWM DUAL OUTPUT modes.

General-Purpose Input/Output

The Z8 Encore! XP F082A Series features 6 to 25 port pins (Ports A–D) for general- purpose input/output (GPIO). The number of GPIO pins available is a function of package, and each pin is individually programmable. 5 V tolerant input pins are available on all I/Os on 8-pin devices and most I/Os on other package types.

Direct LED Drive

The 20- and 28-pin devices support controlled current sinking output pins capable of driving LEDs without the need for a current limiting resistor. These LED drivers are independently programmable to four different intensity levels.

Flash Controller

The Flash Controller programs and erases Flash memory. The Flash Controller supports several protection mechanisms against accidental program and erasure, as well as factory serialization and read protection.

Non-Volatile Data Storage

The non-volatile data storage (NVDS) uses a hybrid hardware/software scheme to implement a byte programmable data memory and is capable of over 100,000 write cycles.

Note: Devices with 8 KB Flash memory do not include the NVDS feature.



Interrupt Controller

The Z8 Encore! XP[®] F082A Series products support up to 20 interrupts. These interrupts consist of 8 internal peripheral interrupts and 12 general-purpose I/O pin interrupt sources. The interrupts have three levels of programmable interrupt priority.

Reset Controller

The Z8 Encore! XP F082A Series products can be reset using the $\overline{\text{RESET}}$ pin, Power-On Reset, Watchdog Timer (WDT) time-out, STOP mode exit, or Voltage Brownout (VBO) warning signal. The $\overline{\text{RESET}}$ pin is bi-directional, that is, it functions as reset source as well as a reset indicator.

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Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
F0B	Timer 1 Reload Low Byte	T1RL	FF	88
F0C	Timer 1 PWM High Byte	T1PWMH	00	88
F0D	Timer 1 PWM Low Byte	T1PWML	00	89
F0E	Timer 1 Control 0	T1CTL0	00	83
F0F	Timer 1 Control 1	T1CTL1	00	84
F10–F6F	Reserved	_	XX	
UART				
F40	UART Transmit/Receive Data Registers	TXD, RXD	XX	113
F41	UART Status 0 Register	U0STAT0	00	111
F42	UART Control 0 Register	U0CTL0	00	108
F43	UART Control 1 Register	U0CTL1	00	108
F44	UART Status 1 Register	U0STAT1	00	112
F45	UART Address Compare Register	U0ADDR	00	114
F46	UART Baud Rate High Byte Register	U0BRH	FF	114
F47	UART Baud Rate Low Byte Register	U0BRL	FF	114
Analog-to-Digit	tal Converter (ADC)			
F70	ADC Control 0	ADCCTL0	00	130
F71	ADC Control 1	ADCCTL1	80	130
F72	ADC Data High Byte	ADCD_H	XX	133
F73	ADC Data Low Bits	ADCD_L	XX	133
F74–F7F	Reserved	_	XX	
Low Power Co	ntrol			
F80	Power Control 0	PWRCTL0	80	35
F81	Reserved	_	XX	
LED Controller				
F82	LED Drive Enable	LEDEN	00	52
F83	LED Drive Level High Byte	LEDLVLH	00	53
F84	LED Drive Level Low Byte	LEDLVLL	00	54
F85	Reserved	—	XX	
Oscillator Cont	rol			
F86	Oscillator Control	OSCCTL	A0	190
F87–F8F	Reserved	_	XX	
Comparator 0				
F90	Comparator 0 Control	CMP0	14	136
XX=Undefined				

Table 7. Register File Address Map (Continued)

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Figure 6. Voltage Brownout Reset Operation

The POR level is greater than the VBO level by the specified hysteresis value. This ensures that the device undergoes a Power-On Reset after recovering from a VBO condition.

Watchdog Timer Reset

If the device is in NORMAL or HALT mode, the Watchdog Timer can initiate a System Reset at time-out if the WDT_RES Flash Option Bit is programmed to 1. This is the unprogrammed state of the WDT_RES Flash Option Bit. If the bit is programmed to 0, it configures the Watchdog Timer to cause an interrupt, not a System Reset, at time-out.

The WDT bit in the Reset Status (RSTSTAT) register is set to signify that the reset was initiated by the Watchdog Timer.

External Reset Input

The $\overline{\text{RESET}}$ pin has a Schmitt-Triggered input and an internal pull-up resistor. Once the $\overline{\text{RESET}}$ pin is asserted for a minimum of four system clock cycles, the device progresses through the System Reset sequence. Because of the possible asynchronicity of the system clock and reset signals, the required reset duration may be as short as three clock periods



Low-Power Modes

The Z8 Encore! XP F082A Series products contain power-saving features. The highest level of power reduction is provided by the STOP mode, in which nearly all device functions are powered down. The next lower level of power reduction is provided by the HALT mode, in which the CPU is powered down.

Further power savings can be implemented by disabling individual peripheral blocks while in Active mode (defined as being in neither STOP nor HALT mode).

STOP Mode

Executing the eZ8 CPU's STOP instruction places the device into STOP mode, powering down all peripherals except the Voltage Brownout detector, the Low-power Operational Amplifier and the Watchdog Timer. These three blocks may also be disabled for additional power savings. Specifically, the operating characteristics are:

- Primary crystal oscillator and internal precision oscillator are stopped; XIN and XOUT (if previously enabled) are disabled, and PA0/PA1 revert to the states programmed by the GPIO registers.
- System clock is stopped.
- eZ8 CPU is stopped.
- Program counter (PC) stops incrementing.
- Watchdog Timer's internal RC oscillator continues to operate if enabled by the Oscillator Control register.
- If enabled, the Watchdog Timer logic continues to operate.
- If enabled for operation in STOP mode by the associated Flash Option Bit, the Voltage Brownout protection circuit continues to operate.
- Low-power operational amplifier continues to operate if enabled by the Power Control register to do so.
- All other on-chip peripherals are idle.

To minimize current in STOP mode, all GPIO pins that are configured as digital inputs must be driven to one of the supply rails (V_{CC} or GND). Additionally, any GPIOs configured as outputs must also be driven to one of the supply rails. The device can be brought out of STOP mode using Stop Mode Recovery. For more information on Stop Mode Recovery, see Reset, Stop Mode Recovery, and Low Voltage Detection on page 23.



Table 18. Port A–D Control Registers (PxCTL)

BITS	7	6	5	4	3	2	1	0
FIELD		PCTL						
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR			FI	D1H, FD5H,	FD9H, FDD	H		

PCTL[7:0]—Port Control

The Port Control register provides access to all sub-registers that configure the GPIO Port operation.

Port A–D Data Direction Sub-Registers

The Port A–D Data Direction sub-register is accessed through the Port A–D Control register by writing 01H to the Port A–D Address register (Table 19).

BITS	7	6	5	4	3	2	1	0
FIELD	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	lf 01H i	n Port A–D /	Address Reg	gister, acces	sible throug	n the Port A-	-D Control F	Register

Table 19. Port A–D Data Direction Sub-Registers (PxDD)

DD[7:0]—Data Direction

These bits control the direction of the associated port pin. Port Alternate Function operation overrides the Data Direction register setting.

0 = Output. Data in the Port A–D Output Data register is driven onto the port pin.

1 = Input. The port pin is sampled and the value written into the Port A–D Input Data Register. The output driver is tristated.

Port A–D Alternate Function Sub-Registers

The Port A–D Alternate Function sub-register (Table 20) is accessed through the Port A–D Control register by writing 02H to the Port A–D Address register. The Port A–D Alternate Function sub-registers enable the alternate function selection on pins. If disabled, pins functions as GPIO. If enabled, select one of four alternate functions using alternate function set subregisters 1 and 2 as described in the Port A–D Alternate Function



Figure 9. Timer Block Diagram

Operation

The timers are 16-bit up-counters. Minimum time-out delay is set by loading the value 0001H into the Timer Reload High and Low Byte registers and setting the prescale value to 1. Maximum time-out delay is set by loading the value 0000H into the Timer Reload High and Low Byte registers and setting the prescale value to 128. If the Timer reaches FFFFH, the timer rolls over to 0000H and continues counting.

Timer Operating Modes

The timers can be configured to operate in the following modes:

ONE-SHOT Mode

In ONE-SHOT mode, the timer counts up to the 16-bit Reload value stored in the Timer Reload High and Low byte registers. The timer input is the system clock. Upon reaching the Reload value, the timer generates an interrupt and the count value in the Timer High and Low Byte registers is reset to 0001H. The timer is automatically disabled and stops counting.

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Z8 Encore! XP[®] F082A Series

Product Specification



- 2. Write to the Timer High and Low Byte registers to set the starting count value. Writing these registers only affects the first pass in GATED mode. After the first timer reset in GATED mode, counting always begins at the reset value of 0001H.
- 3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
- 4. Enable the timer interrupt, if appropriate, and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input deassertion and reload events. If appropriate, configure the timer interrupt to be generated only at the input deassertion event or the reload event by setting TICONFIG field of the TxCTL0 register.
- 5. Configure the associated GPIO port pin for the Timer Input alternate function.
- 6. Write to the Timer Control register to enable the timer.
- 7. Assert the Timer Input signal to initiate the counting.

CAPTURE/COMPARE Mode

In CAPTURE/COMPARE mode, the timer begins counting on the first external Timer Input transition. The acceptable transition (rising edge or falling edge) is set by the TPOL bit in the Timer Control Register. The timer input is the system clock.

Every subsequent acceptable transition (after the first) of the Timer Input signal captures the current count value. The Capture value is written to the Timer PWM High and Low Byte Registers. When the Capture event occurs, an interrupt is generated, the count value in the Timer High and Low Byte registers is reset to 0001H, and counting resumes. The INPCAP bit in TxCTL0 register is set to indicate the timer interrupt is caused by an input capture event.

If no Capture event occurs, the timer counts up to the 16-bit Compare value stored in the Timer Reload High and Low Byte registers. Upon reaching the Compare value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. The INPCAP bit in TxCTL0 register is cleared to indicate the timer interrupt is not because of an input capture event.

Follow the steps below for configuring a timer for CAPTURE/COMPARE mode and initiating the count:

- 1. Write to the Timer Control register to:
 - Disable the timer.
 - Configure the timer for CAPTURE/COMPARE mode.
 - Set the prescale value.
 - Set the Capture edge (rising or falling) for the Timer Input.
- 2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
- 3. Write to the Timer Reload High and Low Byte registers to set the Compare value.



Watchdog Timer Reload Registers results in a one-second timeout at room temperature and 3.3 V supply voltage.

Timeouts other than one second may be obtained by scaling the calibration values up or down as required.

Note: *The Watchdog Timer accuracy still degrades as temperature and supply voltage vary. See* Table 133 on page 230 *for* details.

Watchdog Timer Control Register Definitions

Watchdog Timer Control Register

The Watchdog Timer Control (WDTCTL) register is a write-only control register. Writing the 55H, AAH unlock sequence to the WDTCTL register address unlocks the three Watchdog Timer Reload Byte registers (WDTU, WDTH, and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL register address produce no effect on the bits in the WDTCTL register. The locking mechanism prevents spurious writes to the Reload registers.

This register address is shared with the read-only Reset Status register.

BITS	7	6	5	4	3	2	1	0
FIELD	WDTUNLK							
RESET	Х	Х	Х	Х	Х	Х	Х	Х
R/W	W	W	W	W	W	W	W	W
ADDR	FF0H							
X = Undef	ined.							

Table 57. Watchdog Timer Control Register (WDTCTL)

WDTUNLK—Watchdog Timer Unlock

The software must write the correct unlocking sequence to this register before it is allowed to modify the contents of the Watchdog Timer reload registers.

Watchdog Timer Reload Upper, High and Low Byte Registers

The Watchdog Timer Reload Upper, High and Low Byte (WDTU, WDTH, WDTL) registers (Table 58 through Table 60) form the 24-bit reload value that is loaded into the Watchdog Timer when a WDT instruction executes. The 24-bit reload value is {WDTU[7:0], WDTH[7:0]}. Writing to these registers sets the appropriate Reload Value. Reading from these registers returns the current Watchdog Timer count value.

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Driver Enable is an active High signal that envelopes the entire transmitted data frame including parity and Stop bits as displayed in Figure 14. The Driver Enable signal asserts when a byte is written to the UART Transmit Data register. The Driver Enable signal asserts at least one UART bit period and no greater than two UART bit periods before the Start bit is transmitted. This allows a setup time to enable the transceiver. The Driver Enable signal deasserts one system clock period after the final Stop bit is transmitted. This one system clock delay allows both time for data to clear the transceiver before disabling it, as well as the ability to determine if another character follows the current character. In the event of back to back characters (new data must be written to the Transmit Data Register before the previous character is completely transmitted) the DE signal is not deasserted between characters. The DEPOL bit in the UART Control Register 1 sets the polarity of the Driver Enable signal.



Figure 14. UART Driver Enable Signal Timing (shown with 1 Stop Bit and Parity)

The Driver Enable to Start bit setup time is calculated as follows:

$$\left(\frac{1}{\text{Baud Rate (Hz)}}\right) \le \text{DE to Start Bit Setup Time (s)} \le \left(\frac{2}{\text{Baud Rate (Hz)}}\right)$$

UART Interrupts

The UART features separate interrupts for the transmitter and the receiver. In addition, when the UART primary functionality is disabled, the Baud Rate Generator can also function as a basic timer with interrupt capability.

Transmitter Interrupts

The transmitter generates a single interrupt when the Transmit Data Register Empty bit (TDRE) is set to 1. This indicates that the transmitter is ready to accept new data for transmission. The TDRE interrupt occurs after the Transmit shift register has shifted the first bit of data out. The Transmit Data register can now be written with the next character to

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Figure 19. Analog-to-Digital Converter Block Diagram

Operation

Data Format

In both SINGLE-ENDED and DIFFERENTIAL modes, the effective output of the ADC is an 11-bit, signed, two's complement digital value. In DIFFERENTIAL mode, the ADC



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#5 MSB #5 LSB

6. Add the gain correction factor to the original offset corrected value.

	#5 MSB	#5 LSB
+		
	#1 MSB	#1 LSB
=		

#6 MSB	#6 LSB
--------	--------

7. Shift the result to the right, using the sign bit determined in Step 1. This allows for the detection of computational overflow.

|--|

Output Data

The following is the output format of the corrected ADC value.

MSB	LSB
s v b a 9 8 7 6	5 4 3 2 1 0

The overflow bit in the corrected output indicates that the computed value was greater than the maximum logical value (+1023) or less than the minimum logical value (-1024). Unlike the hardware overflow bit, this is not a simple binary Flag. For a normal sample (non-overflow), the sign and the overflow bit matches. If the sign bit and overflow bit do not match, a computational overflow has occurred.

Input Buffer Stage

Many applications require the measurement of an input voltage source with a high output impedance. This ADC provides a buffered input for such situations. The drawback of the buffered input is a limitation of the input range. When using unity gain buffered mode, the input signal must be prevented from coming too close to either V_{SS} or V_{DD} . See Table 135 on page 231 for details.

This condition applies only to the input voltage level (with respect to ground) of each differential input signal. The actual differential input voltage magnitude may be less than 300 mV.

The input range of the unbuffered ADC swings from V_{SS} to V_{DD} . Input signals smaller than 300 mV must use the unbuffered input mode. If these signals do not contain low output impedances, they might require off-chip buffering.

Signals outside the allowable input range can be used without instability or device damage. Any ADC readings made outside the input range are subject to greater inaccuracy than specified.

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WDTCALH—Watchdog Timer Calibration High Byte The WDTCALH and WDTCALL bytes, when loaded into the Watchdog Timer reload registers result in a one second timeout at room temperature and 3.3 V supply voltage. To use the Watchdog Timer calibration, user code must load WDTU with 0x00, WDTH with WDTCALH and WDTL with WDTCALL.

Table 98. Watchdog Calibration Low Byte at 007FH (WDTCALL)

BITS	7	6	5	4	3	2	1	0
FIELD	WDTCALL							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	Information Page Memory 007FH							
Note: U =	Unchanged b	v Reset. R/W	= Read/Write	e.				

WDTCALL—Watchdog Timer Calibration Low Byte

The WDTCALH and WDTCALL bytes, when loaded into the Watchdog Timer reload registers result in a one second timeout at room temperature and 3.3 V supply voltage. To use the Watchdog Timer calibration, user code must load WDTU with 0x00, WDTH with WDTCALH and WDTL with WDTCALL.

Serialization Data

Table 99. Serial Number at 001C - 001F (S_NUM)

BITS	7	6	5	4	3	2	1	0
FIELD	S_NUM							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	Information Page Memory 001C-001F							
Note: U =	Unchanged b	y Reset. R/W	= Read/Write).				

S NUM—Serial Number Byte

The serial number is a unique four-byte binary value.

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resides in working register R0. The bit fields of this status byte are defined in Table 103. The contents of the status byte are undefined for write operations to illegal addresses. Also, user code must pop the address and data bytes off the stack.

The write routine uses 13 bytes of stack space in addition to the two bytes of address and data pushed by the user. Sufficient memory must be available for this stack usage.

Because of the Flash memory architecture, NVDS writes exhibit a non-uniform execution time. In general, a write takes $251 \,\mu s$ (assuming a 20 MHz system clock). Every 400 to 500 writes, however, a maintenance operation is necessary. In this rare occurrence, the write takes up to 61 ms to complete. Slower system clock speeds result in proportionally higher execution times.

NVDS byte writes to invalid addresses (those exceeding the NVDS array size) have no effect. Illegal write operations have a 2 μ s execution time.

Table 103. Write Status Byte

BITS	7	6	5	4	3	2	1	0
FIELD		Rese	erved		RCPY	PF	AWE	DWE
DEFAULT VALUE	0	0	0	0	0	0	0	0

Reserved—Must be 0.

RCPY—Recopy Subroutine Executed

A recopy subroutine was executed. These operations take significantly longer than a normal write operation.

PF—Power Failure Indicator

A power failure or system reset occurred during the most recent attempted write to the NVDS array.

AW-Address Write Error

An address byte failure occurred during the most recent attempted write to the NVDS array.

DWE—Data Write Error

A data byte failure occurred during the most recent attempted write to the NVDS array.

Byte Read

To read a byte from the NVDS array, user code must first push the address onto the stack. User code issues a CALL instruction to the address of the byte-read routine (0x1000). At the return from the sub-routine, the read byte resides in working register R0, and the read status byte resides in working register R1. The contents of the status byte are undefined for

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Figure 27 displays a recommended configuration for connection with an external fundamental-mode, parallel-resonant crystal operating at 20 MHz. Recommended 20 MHz crystal specifications are provided in Table 110. Printed circuit board layout must add no more than 4 pF of stray capacitance to either the X_{IN} or X_{OUT} pins. If oscillation does not occur, reduce the values of capacitors C₁ and C₂ to decrease loading.



Figure 27. Recommended 20 MHz Crystal Oscillator Configuration

Table 110. Rec	commended Cr	ystal Osc	illator S	pecifications
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Parameter	Value	Units	Comments
Frequency	20	MHz	
Resonance	Parallel		
Mode	Fundamental		
Series Resistance (R _S)	60	Ω	Maximum
Load Capacitance (C _L)	30	pF	Maximum
Shunt Capacitance (C ₀)	7	pF	Maximum
Drive Level	1	mW	Maximum

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	Lower Nibble (Hex)															
i	0	1	2	3	4	5	6	7	8	9	А	В	С	D	Е	F
	1.1	2.2	2.3	2.4	3.3	3.4	3.3	3.4	4.3	4.3	2.3	2.2	2.2	3.2	1.2	1.2
0	BRK	SRP	ADD	ADD	ADD	ADD	ADD	ADD	ADDX	ADDX	DJNZ	JR	LD	JP	INC	NOP
	0.0	IM	r1,r2	r1,Ir2	R2,R1	IR2,R1	R1,IM		ER2,ER1	IM,ER1	r1,X	CC,X	r1,IM	CC,DA	r1	0
1	RI C	Z.3 RIC														See 2nd Oncode
•	R1	IR1	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						Мар
	2.2	2.3	2.3	2.4	3.3	3.4	3.3	3.4	4.3	4.3						1.2
2	INC	INC	SUB	SUB	SUB	SUB	SUB	SUB	SUBX	SUBX						ATM
	R1	IR1	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
2	2.2	2.3	2.3 SBC	2.4	3.3 SBC	3.4	3.3 SBC	3.4 SBC	4.3	4.3						
3	R1	IR1	r1 r2	r1 lr2	82 R1	IR2 R1	B1 IM	IR1 IM	FR2 FR1	IM FR1						
	2.2	2.3	2.3	2.4	3.3	3.4	3.3	3.4	4.3	4.3						
4	DA	DA	OR	OR	OR	OR	OR	OR	ORX	ORX						
	R1	IR1	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
_	2.2	2.3	2.3	2.4	3.3	3.4	3.3	3.4	4.3	4.3						1.2
5	POP			AND												WDT
	2.2	23	23	24	3.3	3.4	3.3	3.4	4.3	4.3						12
6	COM	COM	ТСМ	TCM	тсм	тсм	тсм	тсм	тсмх	тсмх						STOP
	R1	IR1	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
	2.2	2.3	2.3	2.4	3.3	3.4	3.3	3.4	4.3	4.3						1.2
7	PUSH	PUSH	TM	TM	TM	TM	TM	TM		TMX						HALT
	R2	IRZ	r1,r2	r1,Ir2	RZ,R1	1RZ,R1	R1,IM	1R1,1M	ERZ,ERT	IM,ER1						10
8	DECW	DECW	LDE	LDEI	LDX	LDX		LDX	LDX	LDX						DI
Ũ	RR1	IRR1	r1,Irr2	lr1,lrr2	r1,ER2	lr1,ER2	IRR2,R1	IRR2,IR1	r1,rr2,X	rr1,r2,X						
	2.2	2.3	2.5	2.9	3.2	3.3	3.4	3.5	3.3	3.5						1.2
9	RL	RL	LDE	LDEI	LDX	LDX	LDX	LDX	LEA	LEA						EI
	R1	IR1	r2,Irr1	lr2,lrr1	r2,ER1	Ir2,ER1	R2,IRR1	IR2,IRR1	r1,r2,X	rr1,rr2,X						
Δ	2.5	2.6 INCW	2.3 CP	2.4 CP	3.3 CP	3.4 CP	3.3 CP	3.4 CP	4.3 CPX	4.3 CPX						1.4 RFT
~	RR1	IRR1	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
	2.2	2.3	2.3	2.4	3.3	3.4	3.3	3.4	4.3	4.3						1.5
В	CLR	CLR	XOR	XOR	XOR	XOR	XOR	XOR	XORX	XORX						IRET
	R1	IR1	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
C	2.2 RRC	2.3 RRC	2.5	2.9	2.3 IP	2.9		3.4 ID	3.2 DIISHY							1.2 RCF
C	R1	IR1	r1.lrr2	Ir1.Irr2	IRR1	Ir1.Irr2		r1.r2.X	ER2							i.oi
	2.2	2.3	2.5	2.9	2.6	2.2	3.3	3.4	3.2							1.2
D	SRA	SRA	LDC	LDCI	CALL	BSWAP	CALL	LD	POPX							SCF
	R1	IR1	r2,Irr1	lr2,Irr1	IRR1	R1	DA	r2,r1,X	ER1							
F	2.2	2.3	2.2 DIT	2.3	3.2	3.3	3.2	3.3	4.2	4.2						1.2
E	R1	IR1	n b r1	r1 lr2	R2 R1	IR2 R1	R1 IM	IR1 IM	ER2 FR1	IM FR1						CCF
	2.2	2.3	2.6	2.3	2.8	3.3	3.3	3.4		, בו גו						
F	SWAP	SWAP	TRAP	LD	MULT	LD	BTJ	BTJ			V	V		♥		
	R1	IR1	Vector	lr1,r2	RR1	R2,IR1	p,b,r1,X	p,b,lr1,X			۷	1	V	V	V	

Figure 31. First Opcode Map

Upper Nibble (Hex)

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General Purpose I/O Port Output Timing

Figure 35 and Table 140 provide timing information for GPIO Port pins.



Figure 35. GPIO Port Output Timing

			Delay (ns)			
Parameter	Abbreviation	-	Minimum	Maximum		
GPIO Port p	bins					
T ₁	XIN Rise to Port Output Valid Delay		_	15		
T ₂	XIN Rise to Port Output Hold Time		2	_		

Table 140. GPIO Port Output Timing



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electrical characteristics and timing 230, 233 interrupt in normal operation 92 interrupt in STOP mode 92 operation 135 refresh 92, 205 reload unlock sequence 93 reload upper, high and low registers 94 reset 27 reset in normal operation 93 reset in STOP mode 93 time-out response 92 WDTCTL register 31, 94, 136, 190 WDTH register 95 WDTL register 95 working register 201 working register pair 201 WTDU register 95

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X 201 XOR 206 XORX 206

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Z8 Encore! block diagram 4 features 1 part selection guide 2



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