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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f021aph020sc">https://www.e-xfl.com/product-detail/zilog/z8f021aph020sc</a>

# Register Map

Table 7 provides the address map for the Register File of the Z8 Encore! XP<sup>®</sup> F082A Series devices. Not all devices and package styles in the Z8 Encore! XP F082A Series support the ADC, or all of the GPIO Ports. Consider registers for unimplemented peripherals as Reserved.

**Table 7. Register File Address Map**

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
<b>General-Purpose RAM</b>				
<b>Z8F082A/Z8F081A Devices</b>				
000–3FF	General-Purpose Register File RAM	—	XX	
400–EFF	Reserved	—	XX	
<b>Z8F042A/Z8F041A Devices</b>				
000–3FF	General-Purpose Register File RAM	—	XX	
400–EFF	Reserved	—	XX	
<b>Z8F022A/Z8F021A Devices</b>				
000–1FF	General-Purpose Register File RAM	—	XX	
200–EFF	Reserved	—	XX	
<b>Z8F012A/Z8F011A Devices</b>				
000–0FF	General-Purpose Register File RAM	—	XX	
100–EFF	Reserved	—	XX	
<b>Timer 0</b>				
F00	Timer 0 High Byte	T0H	00	<a href="#">87</a>
F01	Timer 0 Low Byte	T0L	01	<a href="#">87</a>
F02	Timer 0 Reload High Byte	T0RH	FF	<a href="#">88</a>
F03	Timer 0 Reload Low Byte	T0RL	FF	<a href="#">88</a>
F04	Timer 0 PWM High Byte	T0PWMH	00	<a href="#">88</a>
F05	Timer 0 PWM Low Byte	T0PWML	00	<a href="#">89</a>
F06	Timer 0 Control 0	T0CTL0	00	<a href="#">83</a>
F07	Timer 0 Control 1	T0CTL1	00	<a href="#">84</a>
<b>Timer 1</b>				
F08	Timer 1 High Byte	T1H	00	<a href="#">87</a>
F09	Timer 1 Low Byte	T1L	01	<a href="#">87</a>
F0A	Timer 1 Reload High Byte	T1RH	FF	<a href="#">88</a>
XX=Undefined				

# Reset, Stop Mode Recovery, and Low Voltage Detection

The Reset Controller within the Z8 Encore! XP<sup>®</sup> F082A Series controls Reset and Stop Mode Recovery operation and provides indication of low supply voltage conditions. In typical operation, the following events cause a Reset:

- Power-On Reset (POR)
- Voltage Brownout (VBO)
- Watchdog Timer time-out (when configured by the WDT\_RES Flash Option Bit to initiate a reset)
- External  $\overline{\text{RESET}}$  pin assertion (when the alternate RESET function is enabled by the GPIO register)
- On-chip debugger initiated Reset (OCDCTL[0] set to 1)

When the device is in STOP mode, a Stop Mode Recovery is initiated by either of the following:

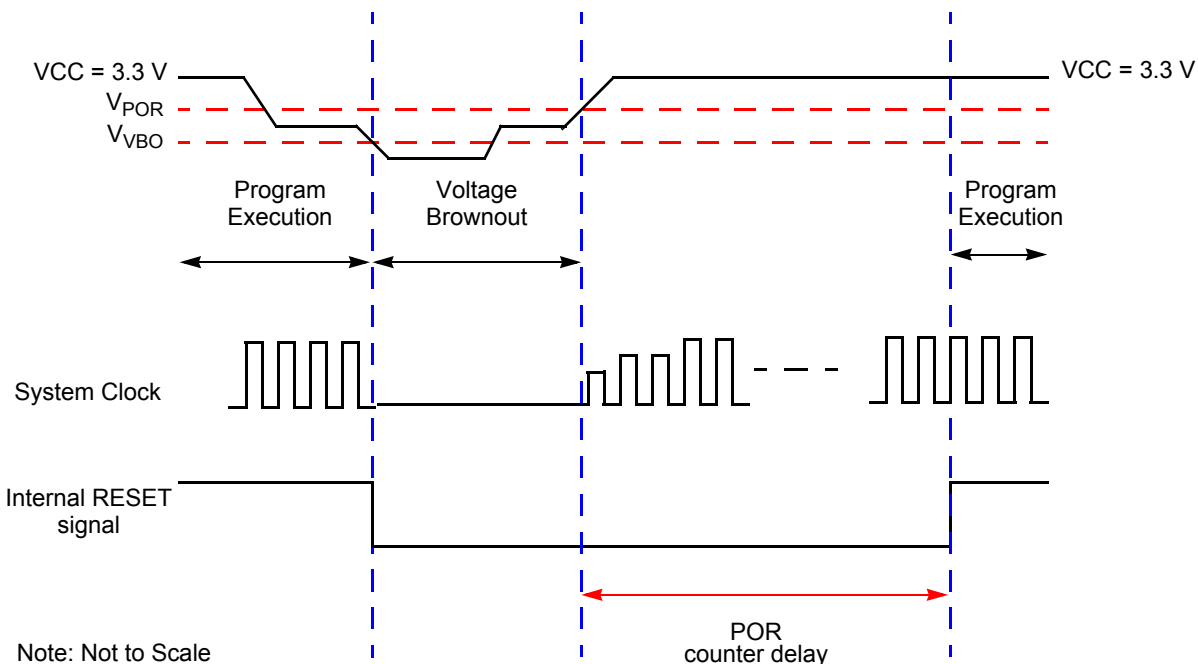
- Watchdog Timer time-out
- GPIO Port input pin transition on an enabled Stop Mode Recovery source

The low voltage detection circuitry on the device (available on the 8-pin product versions only) performs the following functions:

- Generates the VBO reset when the supply voltage drops below a minimum safe level.
- Generates an interrupt when the supply voltage drops below a user-defined level (8-pin devices only).

## Reset Types

The Z8 Encore! XP F082A Series provides several different types of Reset operation. Stop Mode Recovery is considered as a form of Reset. [Table 8](#) lists the types of Reset and their operating characteristics. The System Reset is longer if the external crystal oscillator is enabled by the Flash option bits, allowing additional time for oscillator start-up.



**Figure 6. Voltage Brownout Reset Operation**

The POR level is greater than the VBO level by the specified hysteresis value. This ensures that the device undergoes a Power-On Reset after recovering from a VBO condition.

## Watchdog Timer Reset

If the device is in NORMAL or HALT mode, the Watchdog Timer can initiate a System Reset at time-out if the WDT\_RES Flash Option Bit is programmed to 1. This is the unprogrammed state of the WDT\_RES Flash Option Bit. If the bit is programmed to 0, it configures the Watchdog Timer to cause an interrupt, not a System Reset, at time-out.

The WDT bit in the Reset Status (RSTSTAT) register is set to signify that the reset was initiated by the Watchdog Timer.

## External Reset Input

The RESET pin has a Schmitt-Triggered input and an internal pull-up resistor. Once the RESET pin is asserted for a minimum of four system clock cycles, the device progresses through the System Reset sequence. Because of the possible asynchronicity of the system clock and reset signals, the required reset duration may be as short as three clock periods

## Interrupt Request 2 Register

The Interrupt Request 2 (IRQ2) register ([Table 35](#)) stores interrupt requests for both vectored and polled interrupts. When a request is presented to the interrupt controller, the corresponding bit in the IRQ2 register becomes 1. If interrupts are globally enabled (vectored interrupts), the interrupt controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU can read the Interrupt Request 2 register to determine if any interrupt requests are pending.

**Table 35. Interrupt Request 2 Register (IRQ2)**

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved				PC3I	PC2I	PC1I	PC0I
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FC6H							

Reserved—Must be 0.

PCxI—Port C Pin *x* Interrupt Request

0 = No interrupt request is pending for GPIO Port C pin *x*.

1 = An interrupt request from GPIO Port C pin *x* is awaiting service.

where *x* indicates the specific GPIO Port C pin number (0–3).

## IRQ0 Enable High and Low Bit Registers

[Table 36](#) describes the priority control for IRQ0. The IRQ0 Enable High and Low Bit registers ([Table 37](#) and [Table 38](#)) form a priority encoded enabling for interrupts in the Interrupt Request 0 register.

**Table 36. IRQ0 Enable and Priority Encoding**

IRQ0ENH[x]	IRQ0ENL[x]	Priority	Description
0	0	Disabled	Disabled
0	1	Level 1	Low
1	0	Level 2	Medium
1	1	Level 3	High

where *x* indicates the register bits from 0–7.

110 = 64 cycles delay

111 = 128 cycles delay

INPCAP—Input Capture Event

This bit indicates if the most recent timer interrupt is caused by a Timer Input Capture Event.

0 = Previous timer interrupt is not a result of Timer Input Capture Event

1 = Previous timer interrupt is a result of Timer Input Capture Event

### Timer 0–1 Control Register 1

The Timer 0–1 Control (TxCTL1) registers enable/disable the timers, set the prescaler value, and determine the timer operating mode (Table 49).

**Table 49. Timer 0–1 Control Register 1 (TxCTL1)**

BITS	7	6	5	4	3	2	1	0
FIELD	TEN	TPOL	PRES			TMODE		
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F07H, F0FH							

TEN—Timer Enable

0 = Timer is disabled.

1 = Timer enabled to count.

TPOL—Timer Input/Output Polarity

Operation of this bit is a function of the current operating mode of the timer.

#### ONE-SHOT mode

When the timer is disabled, the Timer Output signal is set to the value of this bit.

When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

#### CONTINUOUS mode

When the timer is disabled, the Timer Output signal is set to the value of this bit.

When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

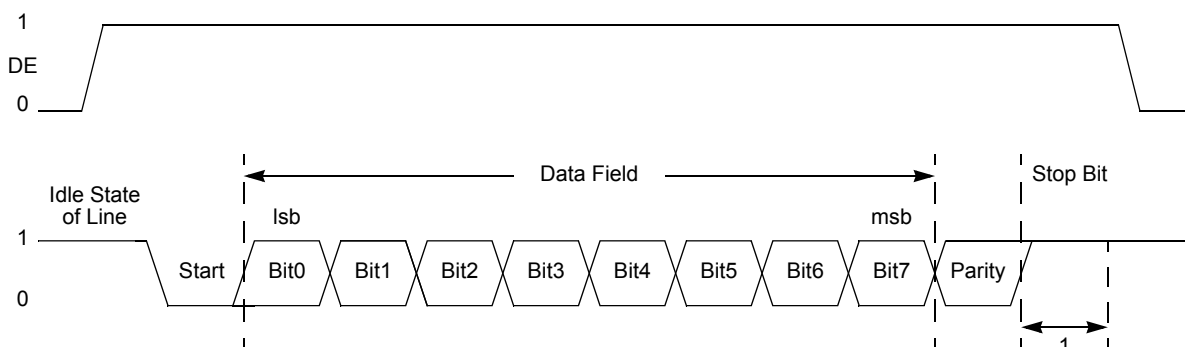
#### COUNTER mode

If the timer is enabled the Timer Output signal is complemented after timer reload.

0 = Count occurs on the rising edge of the Timer Input signal.

1 = Count occurs on the falling edge of the Timer Input signal.

Driver Enable is an active High signal that envelopes the entire transmitted data frame including parity and Stop bits as displayed in Figure 14. The Driver Enable signal asserts when a byte is written to the UART Transmit Data register. The Driver Enable signal asserts at least one UART bit period and no greater than two UART bit periods before the Start bit is transmitted. This allows a setup time to enable the transceiver. The Driver Enable signal deasserts one system clock period after the final Stop bit is transmitted. This one system clock delay allows both time for data to clear the transceiver before disabling it, as well as the ability to determine if another character follows the current character. In the event of back to back characters (new data must be written to the Transmit Data Register before the previous character is completely transmitted) the DE signal is not deasserted between characters. The DEPOL bit in the UART Control Register 1 sets the polarity of the Driver Enable signal.



**Figure 14. UART Driver Enable Signal Timing (shown with 1 Stop Bit and Parity)**

The Driver Enable to Start bit setup time is calculated as follows:

$$\left( \frac{1}{\text{Baud Rate (Hz)}} \right) \leq \text{DE to Start Bit Setup Time (s)} \leq \left( \frac{2}{\text{Baud Rate (Hz)}} \right)$$

## UART Interrupts

The UART features separate interrupts for the transmitter and the receiver. In addition, when the UART primary functionality is disabled, the Baud Rate Generator can also function as a basic timer with interrupt capability.

### Transmitter Interrupts

The transmitter generates a single interrupt when the Transmit Data Register Empty bit (TDRE) is set to 1. This indicates that the transmitter is ready to accept new data for transmission. The TDRE interrupt occurs after the Transmit shift register has shifted the first bit of data out. The Transmit Data register can now be written with the next character to

and the CTSE bit. If the  $\overline{\text{CTS}}$  signal is Low and the CTSE bit is 1, the transmitter is enabled.

0 = Transmitter disabled.

1 = Transmitter enabled.

REN—Receive Enable

This bit enables or disables the receiver.

0 = Receiver disabled.

1 = Receiver enabled.

CTSE—CTS Enable

0 = The  $\overline{\text{CTS}}$  signal has no effect on the transmitter.

1 = The UART recognizes the  $\overline{\text{CTS}}$  signal as an enable control from the transmitter.

PEN—Parity Enable

This bit enables or disables parity. Even or odd is determined by the PSEL bit.

0 = Parity is disabled.

1 = The transmitter sends data with an additional parity bit and the receiver receives an additional parity bit.

PSEL—Parity Select

0 = Even parity is transmitted and expected on all received data.

1 = Odd parity is transmitted and expected on all received data.

SBRK—Send Break

This bit pauses or breaks data transmission. Sending a break interrupts any transmission in progress, so ensure that the transmitter has finished sending data before setting this bit.

0 = No break is sent.

1 = Forces a break condition by setting the output of the transmitter to zero.

STOP—Stop Bit Select

0 = The transmitter sends one stop bit.

1 = The transmitter sends two stop bits.

LBEN—Loop Back Enable

0 = Normal operation.

1 = All transmitted data is looped back to the receiver.

**Table 62. UART Control 1 Register (U0CTL1)**

BITS	7	6	5	4	3	2	1	0
FIELD	MPMD[1]	MPEN	MPMD[0]	MPBT	DEPOL	BRGCTL	RDAIRQ	IREN
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F43H							



MPRX—Multiprocessor Receive

Returns the value of the most recent multiprocessor bit received. Reading from the UART Receive Data register resets this bit to 0.

## UART Transmit Data Register

Data bytes written to the UART Transmit Data (UxTXD) register (Table 65) are shifted out on the TXD<sub>x</sub> pin. The Write-only UART Transmit Data register shares a Register File address with the read-only UART Receive Data register.

**Table 65. UART Transmit Data Register (U0TXD)**

BITS	7	6	5	4	3	2	1	0
FIELD	TXD							
RESET	X	X	X	X	X	X	X	X
R/W	W	W	W	W	W	W	W	W
ADDR	F40H							

TXD—Transmit Data

UART transmitter data byte to be shifted out through the TXD<sub>x</sub> pin.

## UART Receive Data Register

Data bytes received through the RXD<sub>x</sub> pin are stored in the UART Receive Data (UxRXD) register (Table 66). The read-only UART Receive Data register shares a Register File address with the Write-only UART Transmit Data register.

**Table 66. UART Receive Data Register (U0RXD)**

BITS	7	6	5	4	3	2	1	0
FIELD	RXD							
RESET	X	X	X	X	X	X	X	X
R/W	R	R	R	R	R	R	R	R
ADDR	F40H							
X = Undefined.								

RXD—Receive Data

UART receiver data byte from the RXD<sub>x</sub> pin

## ADC Control Register Definitions

### ADC Control Register 0

The ADC Control Register 0 (ADCCTL0) selects the analog input channel and initiates the analog-to-digital conversion. It also selects the voltage reference configuration.

**Table 71. ADC Control Register 0 (ADCCTL0)**

BITS	7	6	5	4	3	2	1	0
FIELD	CEN	REFSELL	REFOUT	CONT	ANAIN[3:0]			
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F70H							

CEN—Conversion Enable

0 = Conversion is complete. Writing a 0 produces no effect. The ADC automatically clears this bit to 0 when a conversion is complete.

1 = Begin conversion. Writing a 1 to this bit starts a conversion. If a conversion is already in progress, the conversion restarts. This bit remains 1 until the conversion is complete.

REFSELL—Voltage Reference Level Select Low Bit; in conjunction with the High bit (REFSELH) in [ADC Control/Status Register 1](#), this determines the level of the internal voltage reference; the following details the effects of {REFSELH, REFSELL}; note that this reference is independent of the Comparator reference.

00= Internal Reference Disabled, reference comes from external pin

01= Internal Reference set to 1.0 V

10= Internal Reference set to 2.0 V (default)

11= Reserved

REFOUT—Internal Reference Output Enable

0 = Reference buffer is disabled; Vref pin is available for GPIO or analog functions

1 = The internal ADC reference is buffered and driven out to the Vref pin



**Warning:** When the ADC is used with an external reference ({REFSELH, REFSELL}=00), the REFOUT bit must be set to 0.

CONT

0 = Single-shot conversion. ADC data is output once at completion of the 5129 system clock cycles (measurements of the internal temperature sensor take twice as long)

1 = Continuous conversion. ADC data updated every 256 system clock cycles after an initial 5129 clock conversion (measurements of the internal temperature sensor take twice as long)

**ANAIN[3:0]—Analog Input Select**

These bits select the analog input for conversion. Not all Port pins in this list are available in all packages for the Z8 Encore! XP<sup>®</sup> F082A Series. For information on port pins available with each package style, see [Pin Description](#) on page 9. Do not enable unavailable analog inputs. Usage of these bits changes depending on the buffer mode selected in [ADC Control/Status Register 1](#).

For the reserved values, all input switches are disabled to avoid leakage or other undesirable operation. ADC samples taken with reserved bit settings are undefined.

**SINGLE-ENDED:**

- 0000 = ANA0 (transimpedance amp output when enabled)
- 0001 = ANA1 (transimpedance amp inverting input)
- 0010 = ANA2 (transimpedance amp non-inverting input)
- 0011 = ANA3
- 0100 = ANA4
- 0101 = ANA5
- 0110 = ANA6
- 0111 = ANA7
- 1000 = Reserved
- 1001 = Reserved
- 1010 = Reserved
- 1011 = Reserved
- 1100 = Hold transimpedance input nodes (ANA1 and ANA2) to ground.
- 1101 = Reserved
- 1110 = Temperature Sensor.
- 1111 = Reserved.

**DIFFERENTIAL (non-inverting input and inverting input respectively):**

- 0000 = ANA0 and ANA1
- 0001 = ANA2 and ANA3
- 0010 = ANA4 and ANA5
- 0011 = ANA1 and ANA0
- 0100 = ANA3 and ANA2
- 0101 = ANA5 and ANA4
- 0110 = ANA6 and ANA5
- 0111 = ANA0 and ANA2
- 1000 = ANA0 and ANA3
- 1001 = ANA0 and ANA4
- 1010 = ANA0 and ANA5
- 1011 = Reserved
- 1100 = Reserved
- 1101 = Reserved
- 1110 = Reserved
- 1111 = Manual Offset Calibration Mode

## Operation

The Flash Controller programs and erases Flash memory. The Flash Controller provides the proper Flash controls and timing for Byte Programming, Page Erase, and Mass Erase of Flash memory.

The Flash Controller contains several protection mechanisms to prevent accidental programming or erasure. These mechanisms operate on the page, sector and full-memory levels.

The Flow Chart in [Figure 22](#) displays basic Flash Controller operation. The following subsections provide details about the various operations (Lock, Unlock, Byte Programming, Page Protect, Page Unprotect, Page Select, Page Erase, and Mass Erase) displayed in [Figure 22](#).

value 63H to the Flash Control register initiates the Mass Erase operation. While the Flash Controller executes the Mass Erase operation, the eZ8 CPU idles but the system clock and on-chip peripherals continue to operate. Using the On-Chip Debugger, poll the Flash Status register to determine when the Mass Erase operation is complete. When the Mass Erase is complete, the Flash Controller returns to its locked state.

## Flash Controller Bypass

The Flash Controller can be bypassed and the control signals for the Flash memory brought out to the GPIO pins. Bypassing the Flash Controller allows faster Row Programming algorithms by controlling the Flash programming signals directly.

Row programming is recommended for gang programming applications and large volume customers who do not require in-circuit initial programming of the Flash memory. Page Erase operations are also supported when the Flash Controller is bypassed.

For more information on bypassing the Flash Controller, refer to *Third-Party Flash Programming Support for Z8 Encore!<sup>®</sup> MCU Application Note (AN0117)* available for download at [www.zilog.com](http://www.zilog.com).

## Flash Controller Behavior in DEBUG Mode

The following changes in behavior of the Flash Controller occur when the Flash Controller is accessed using the On-Chip Debugger:

- The Flash Write Protect option bit is ignored.
- The Flash Sector Protect register is ignored for programming and erase operations.
- Programming operations are not limited to the page selected in the Page Select register.
- Bits in the Flash Sector Protect register can be written to one or zero.
- The second write of the Page Select register to unlock the Flash Controller is not necessary.
- The Page Select register can be written when the Flash Controller is unlocked.
- The Mass Erase command is enabled through the Flash Control register.



**Caution:** *For security reasons, the Flash controller allows only a single page to be opened for write/erase. When writing multiple Flash pages, the flash controller must go through the unlock sequence again to select another page.*

**Table 80. Flash Page Select Register (FPS)**

BITS	7	6	5	4	3	2	1	0
FIELD	INFO_EN	PAGE						
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FF9H							

INFO\_EN—Information Area Enable

0 = Information Area us not selected.

1 = Information Area is selected. The Information Area is mapped into the Program Memory address space at addresses FE00H through FFFFH.

PAGE—Page Select

This 7-bit field identifies the Flash memory page for Page Erase and page unlocking. Program Memory Address[15:9] = PAGE[6:0]. For the Z8F08xx devices, the upper 3 bits must be zero. For the Z8F04xx devices, the upper 4 bits must be zero. For Z8F02xx devices, the upper 5 bits must always be 0. For the Z8F01xx devices, the upper 6 bits must always be 0.

## Flash Sector Protect Register

The Flash Sector Protect (FPROT) register is shared with the Flash Page Select Register. When the [Flash Control Register](#) is written with 73H followed by 5EH, the next write to this address targets the Flash Sector Protect Register. In all other cases, it targets the Flash Page Select Register.

This register selects one of the 8 available Flash memory sectors to be protected. The reset state of each Sector Protect bit is an unprotected state. After a sector is protected by setting its corresponding register bit, it cannot be unprotected (the register bit cannot be cleared) without powering down the device.

**Table 81. Flash Sector Protect Register (FPROT)**

BITS	7	6	5	4	3	2	1	0
FIELD	SPROT7	SPROT6	SPROT5	SPROT4	SPROT3	SPROT2	SPROT1	SPROT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FF9H							

## Breakpoints in Flash Memory

The BRK instruction is opcode 00H, which corresponds to the fully programmed state of a byte in Flash memory. To implement a Breakpoint, write 00H to the required break address, overwriting the current instruction. To remove a Breakpoint, the corresponding page of Flash memory must be erased and reprogrammed with the original data.

## Runtime Counter

The On-Chip Debugger contains a 16-bit Runtime Counter. It counts system clock cycles between Breakpoints. The counter starts counting when the On-Chip Debugger leaves DEBUG mode and stops counting when it enters DEBUG mode again or when it reaches the maximum count of FFFFH.

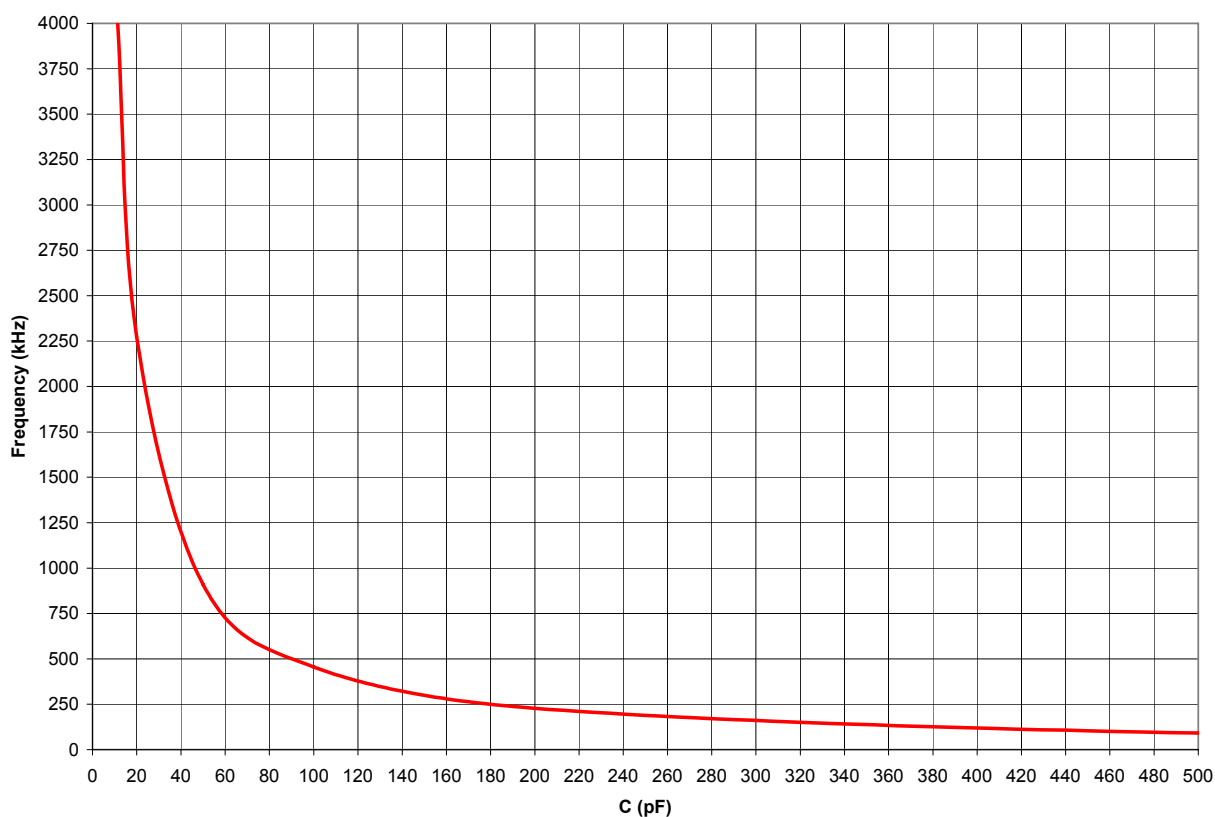
## On-Chip Debugger Commands

The host communicates to the on-chip debugger by sending OCD commands using the DBG interface. During normal operation, only a subset of the OCD commands are available. In DEBUG mode, all OCD commands become available unless the user code and control registers are protected by programming the Flash Read Protect Option bit (FRP). The Flash Read Protect Option bit prevents the code in memory from being read out of the Z8 Encore! XP F082A Series products. When this option is enabled, several of the OCD commands are disabled. Table 106 on page 184 is a summary of the On-chip debugger commands. Each OCD command is described in further detail in the bulleted list following this table. Table 106 on page 184 also indicates those commands that operate when the device is not in DEBUG mode (normal operation) and those commands that are disabled by programming the Flash Read Protect Option bit.

Debug Command	Command Byte	Enabled when NOT in DEBUG mode?	Disabled by Flash Read Protect Option Bit
Read OCD Revision	00H	Yes	—
Reserved	01H	—	—
Read OCD Status Register	02H	Yes	—
Read Runtime Counter	03H	—	—
Write OCD Control Register	04H	Yes	Cannot clear DBGMODE bit
Read OCD Control Register	05H	Yes	—
Write Program Counter	06H	—	Disabled
Read Program Counter	07H	—	Disabled

Figure 29 displays the typical (3.3 V and 25 °C) oscillator frequency as a function of the capacitor ( $C$  in pF) employed in the RC network assuming a 45 K $\Omega$  external resistor. For very small values of  $C$ , the parasitic capacitance of the oscillator XIN pin and the printed circuit board must be included in the estimation of the oscillator frequency.

It is possible to operate the RC oscillator using only the parasitic capacitance of the package and printed circuit board. To minimize sensitivity to external parasitics, external capacitance values in excess of 20 pF are recommended.



**Figure 29. Typical RC Oscillator Frequency as a Function of the External Capacitance with a 45 k $\Omega$  Resistor**



**Caution:**

*When using the external RC oscillator mode, the oscillator can stop oscillating if the power supply drops below 2.7 V, but before the power supply drops to the Voltage Brownout threshold. The oscillator resumes oscillation when the supply voltage exceeds 2.7 V.*



Table 124. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
XOR dst, src	dst ← dst XOR src	r	r	B2	–	*	*	0	–	–	2	3
		r	lr	B3							2	4
		R	R	B4							3	3
		R	IR	B5							3	4
		R	IM	B6							3	3
		IR	IM	B7							3	4
XORX dst, src	dst ← dst XOR src	ER	ER	B8	–	*	*	0	–	–	4	3
		ER	IM	B9							4	3
Flags Notation:	* = Value is a function of the result of the operation. – = Unaffected X = Undefined				0 = Reset to 0 1 = Set to 1							

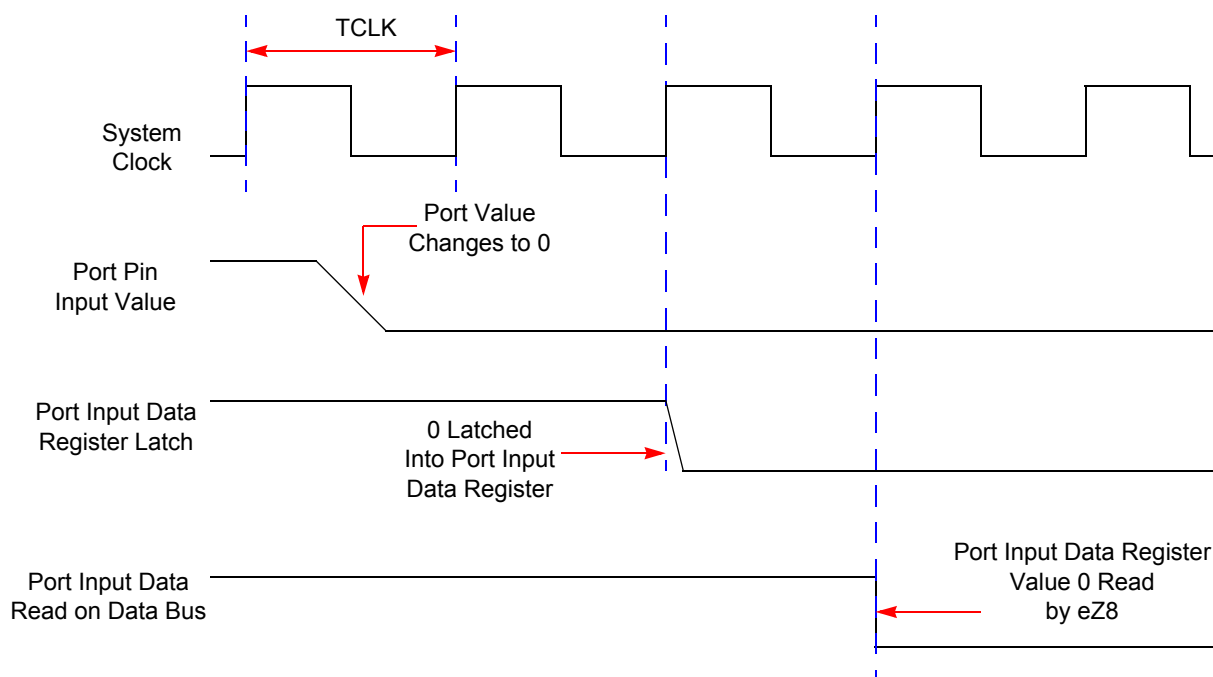


Figure 34. Port Input Sample Timing

Table 139. GPIO Port Input Timing

Parameter Abbreviation		Delay (ns)	
		Minimum	Maximum
$T_{S\_PORT}$	Port Input Transition to XIN Rise Setup Time (Not pictured)	5	–
$T_{H\_PORT}$	XIN Rise to Port Input Transition Hold Time (Not pictured)	0	–
$T_{SMR}$	GPIO Port Pin Pulse Width to ensure Stop Mode Recovery (for GPIO Port Pins enabled as SMR sources)	1 $\mu$ s	

Figure 44 displays the 20-pin Small Shrink Outline Package (SSOP) available for the Z8 Encore! XP F082A Series devices.

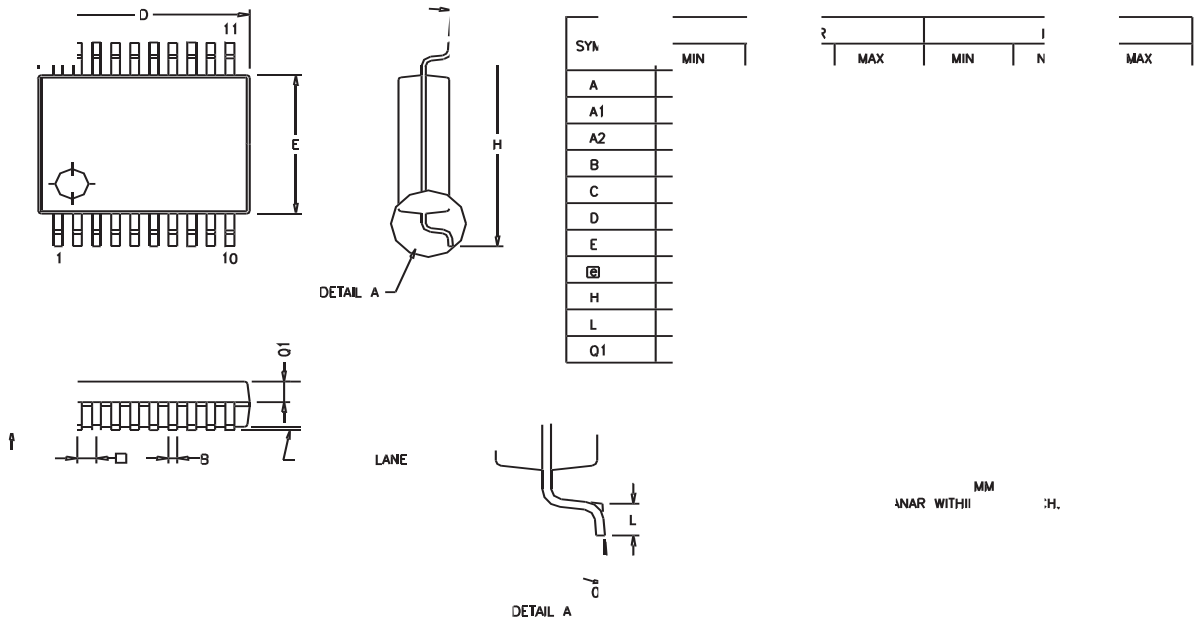


Figure 44. 20-Pin Small Shrink Outline Package (SSOP)

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
<b>Z8 Encore! XP<sup>®</sup> F082A Series with 2 KB Flash, 10-Bit Analog-to-Digital Converter</b>											
<b>Standard Temperature: 0 °C to 70 °C</b>											
Z8F022APB020SC	2 KB	512 B	64 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F022AQB020SC	2 KB	512 B	64 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F022ASB020SC	2 KB	512 B	64 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F022ASH020SC	2 KB	512 B	64 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F022AHH020SC	2 KB	512 B	64 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F022APH020SC	2 KB	512 B	64 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F022ASJ020SC	2 KB	512 B	64 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F022AHJ020SC	2 KB	512 B	64 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F022APJ020SC	2 KB	512 B	64 B	23	20	2	8	1	1	1	PDIP 28-pin package
<b>Extended Temperature: -40 °C to 105 °C</b>											
Z8F022APB020EC	2 KB	512 B	64 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F022AQB020EC	2 KB	512 B	64 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F022ASB020EC	2 KB	512 B	64 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F022ASH020EC	2 KB	512 B	64 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F022AHH020EC	2 KB	512 B	64 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F022APH020EC	2 KB	512 B	64 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F022ASJ020EC	2 KB	512 B	64 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F022AHJ020EC	2 KB	512 B	64 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F022APJ020EC	2 KB	512 B	64 B	23	20	2	8	1	1	1	PDIP 28-pin package
Replace C with G for Lead-Free Packaging											

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
<b>Z8 Encore! XP<sup>®</sup> F082A Series Development Kit</b>											
<b>Z8F08A28100KITG</b>											<b>Z8 Encore! XP F082A Series 28-Pin Development Kit</b>
<b>Z8F04A28100KITG</b>											<b>Z8 Encore! XP F042A Series 28-Pin Development Kit</b>
<b>Z8F04A08100KITG</b>											<b>Z8 Encore! XP F042A Series 8-Pin Development Kit</b>
<b>ZUSBSC00100ZACG</b>											<b>USB Smart Cable Accessory Kit</b>
<b>ZUSBOPTSC01ZACG</b>											<b>USB Opto-Isolated Smart Cable Accessory Kit</b>
<b>ZENETSC0100ZACG</b>											<b>Ethernet Smart Cable Accessory Kit</b>