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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	6
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f021asb020sc">https://www.e-xfl.com/product-detail/zilog/z8f021asb020sc</a>

The pin configurations listed are preliminary and subject to change based on manufacturing limitations.

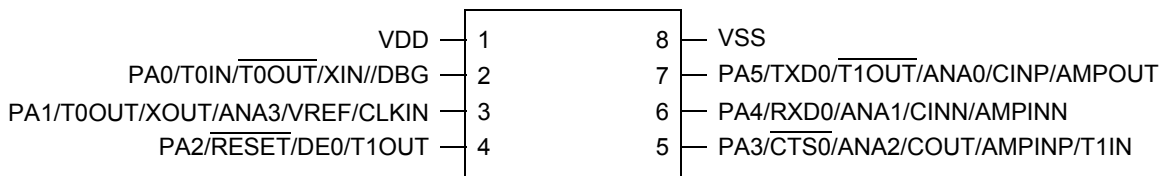


Figure 2. Z8F08xA, Z8F04xA, Z8F02xA, and Z8F01xA in 8-Pin SOIC, QFN/MLF-S, or PDIP Package

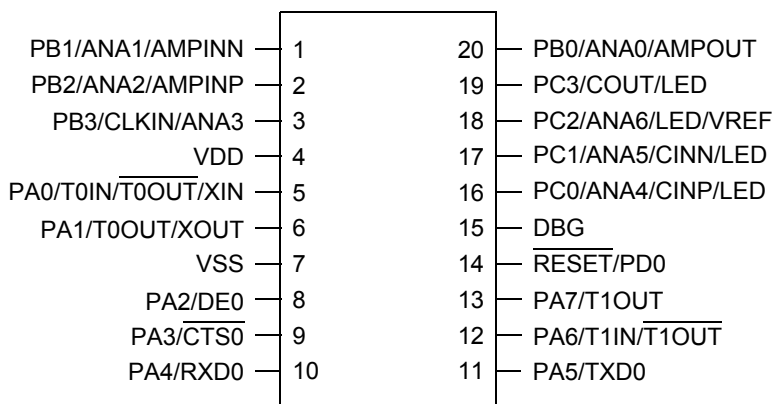


Figure 3. Z8F08xA, Z8F04xA, Z8F02xA, and Z8F01xA in 20-Pin SOIC, SSOP or PDIP Package

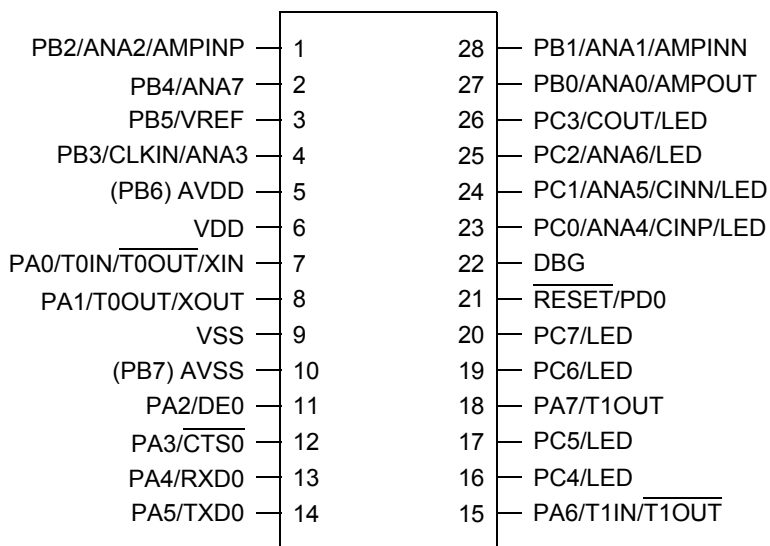


Figure 4. Z8F08xA, Z8F04xA, Z8F02xA, and Z8F01xA in 28-Pin SOIC, SSOP or PDIP Package

**Table 5. Z8 Encore! XP F082A Series Program Memory Maps (Continued)**

Program Memory Address (Hex)	Function
<b>Z8F022A and Z8F021A Products</b>	
0000–0001	Flash Option Bits
0002–0003	Reset Vector
0004–0005	WDT Interrupt Vector
0006–0007	Illegal Instruction Trap
0008–0037	Interrupt Vectors*
0038–0039	Reserved
003A–003D	Oscillator Fail Trap Vectors
003E–07FF	Program Memory
<b>Z8F012A and Z8F011A Products</b>	
0000–0001	Flash Option Bits
0002–0003	Reset Vector
0004–0005	WDT Interrupt Vector
0006–0007	Illegal Instruction Trap
0008–0037	Interrupt Vectors*
0038–0039	Reserved
003A–003D	Oscillator Fail Trap Vectors
003E–03FF	Program Memory
* See <a href="#">Table 32</a> on page 56 for a list of the interrupt vectors.	

## Data Memory

The Z8 Encore! XP F082A Series does not use the eZ8 CPU's 64 KB Data Memory address space.

## Flash Information Area

[Table 6](#) on page 18 describes the Z8 Encore! XP F082A Series Flash Information Area. This 128 B Information Area is accessed by setting bit 7 of the Flash Page Select Register to 1. When access is enabled, the Flash Information Area is mapped into the Program Memory and overlays the 128 bytes at addresses FE00H to FF7FH. When the Information Area access is enabled, all reads from these Program Memory addresses return the Infor-

Reserved—Must be 0.

C3ENL—Port C3 Interrupt Request Enable Low Bit

C2ENL—Port C2 Interrupt Request Enable Low Bit

C1ENL—Port C1 Interrupt Request Enable Low Bit

C0ENL—Port C0 Interrupt Request Enable Low Bit

## Interrupt Edge Select Register

The Interrupt Edge Select (IRQES) register ([Table 45](#)) determines whether an interrupt is generated for the rising edge or falling edge on the selected GPIO Port A input pin.

**Table 45. Interrupt Edge Select Register (IRQES)**

BITS	7	6	5	4	3	2	1	0
FIELD	IES7	IES6	IES5	IES4	IES3	IES2	IES1	IES0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FCDH							

IES<sub>x</sub>—Interrupt Edge Select *x*

0 = An interrupt request is generated on the falling edge of the PA<sub>x</sub> input.

1 = An interrupt request is generated on the rising edge of the PA<sub>x</sub> input.

where *x* indicates the specific GPIO Port pin number (0 through 7).

## Shared Interrupt Select Register

The Shared Interrupt Select (IRQSS) register ([Table 46](#)) determines the source of the PAD<sub>x</sub>S interrupts. The Shared Interrupt Select register selects between Port A and alternate sources for the individual interrupts.

Because these shared interrupts are edge-triggered, it is possible to generate an interrupt just by switching from one shared source to another. For this reason, an interrupt must be disabled before switching between sources.

Follow the steps below for configuring a timer for COUNTER mode and initiating the count:

1. Write to the Timer Control register to:
  - Disable the timer.
  - Configure the timer for COUNTER mode.
  - Select either the rising edge or falling edge of the Timer Input signal for the count. This selection also sets the initial logic level (High or Low) for the Timer Output alternate function. However, the Timer Output function is not required to be enabled.
2. Write to the Timer High and Low Byte registers to set the starting count value. This only affects the first pass in COUNTER mode. After the first timer Reload in COUNTER mode, counting always begins at the reset value of 0001H. In COUNTER mode the Timer High and Low Byte registers must be written with the value 0001H.
3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
4. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
5. Configure the associated GPIO port pin for the Timer Input alternate function.
6. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
7. Write to the Timer Control register to enable the timer.

In COUNTER mode, the number of Timer Input transitions since the timer start is given by the following equation:

$$\text{COUNTER Mode Timer Input Transitions} = \text{Current Count Value} - \text{Start Value}$$

### COMPARATOR COUNTER Mode

In COMPARATOR COUNTER mode, the timer counts input transitions from the analog comparator output. The TPOL bit in the Timer Control Register selects whether the count occurs on the rising edge or the falling edge of the comparator output signal. In COMPARATOR COUNTER mode, the prescaler is disabled.



**Caution:** *The frequency of the comparator output signal must not exceed one-fourth the system clock frequency. Further, the high or low state of the comparator output signal pulse must be no less than twice the system clock period. A shorter pulse may not be captured.*

After reaching the Reload value stored in the Timer Reload High and Low Byte registers, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer Reload.

## Timer Control Register Definitions

### Timer 0–1 Control Registers

#### Time 0–1 Control Register 0

The Timer Control Register 0 (TxCTL0) and Timer Control Register 1 (TxCTL1) determine the timer operating mode (Table 48). It also includes a programmable PWM dead-band delay, two bits to configure timer interrupt definition, and a status bit to identify if the most recent timer interrupt is caused by an input capture event.

**Table 48. Timer 0–1 Control Register 0 (TxCTL0)**

BITS	7	6	5	4	3	2	1	0
FIELD	TMODEHI	TICONFIG		Reserved	PWMD			INPCAP
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
ADDR	F06H, F0EH							

**TMODEHI**—Timer Mode High Bit

This bit along with the TMODE field in TxCTL1 register determines the operating mode of the timer. This is the most significant bit of the Timer mode selection value. See the TxCTL1 register description for details of the full timer mode decoding.

**TICONFIG**—Timer Interrupt Configuration

This field configures timer interrupt definition.

0x = Timer Interrupt occurs on all defined Reload, Compare and Input Events

10 = Timer Interrupt only on defined Input Capture/Deassertion Events

11 = Timer Interrupt only on defined Reload/Compare Events

Reserved—Must be 0.

**PWMD**—PWM Delay value

This field is a programmable delay to control the number of system clock cycles delay before the Timer Output and the Timer Output Complement are forced to their active state.

000 = No delay

001 = 2 cycles delay

010 = 4 cycles delay

011 = 8 cycles delay

100 = 16 cycles delay

101 = 32 cycles delay

### WDT Reset in Normal Operation

If configured to generate a Reset when a time-out occurs, the Watchdog Timer forces the device into the System Reset state. The WDT status bit in the Reset Status (RSTSTAT) register is set to 1. For more information on system reset, see [Reset, Stop Mode Recovery, and Low Voltage Detection](#) on page 23.

### WDT Reset in STOP Mode

If configured to generate a Reset when a time-out occurs and the device is in STOP mode, the Watchdog Timer initiates a Stop Mode Recovery. Both the WDT status bit and the STOP bit in the Reset Status (RSTSTAT) register are set to 1 following WDT time-out in STOP mode.

## Watchdog Timer Reload Unlock Sequence

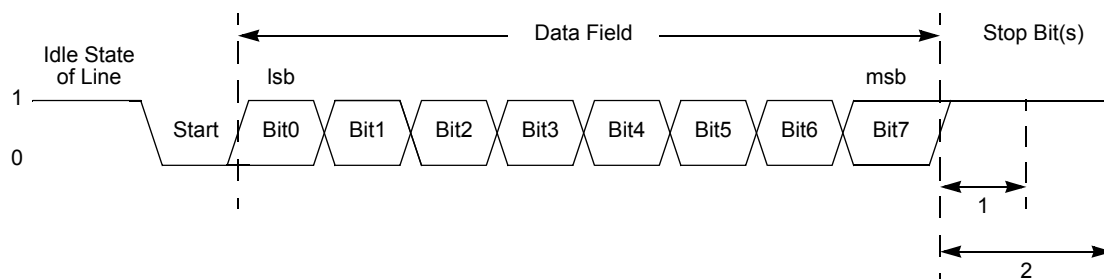
Writing the unlock sequence to the Watchdog Timer (WDTCTL) Control register address unlocks the three Watchdog Timer Reload Byte registers (WDTU, WDTM, and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL register address produce no effect on the bits in the WDTCTL register. The locking mechanism prevents spurious writes to the Reload registers. Follow the steps below to unlock the Watchdog Timer Reload Byte registers (WDTU, WDTM, and WDTL) for write access.

1. Write 55H to the Watchdog Timer Control register (WDTCTL).
2. Write AAH to the Watchdog Timer Control register (WDTCTL).
3. Write the Watchdog Timer Reload Upper Byte register (WDTU) with the desired time-out value.
4. Write the Watchdog Timer Reload High Byte register (WDTM) with the desired time-out value.
5. Write the Watchdog Timer Reload Low Byte register (WDTL) with the desired time-out value.

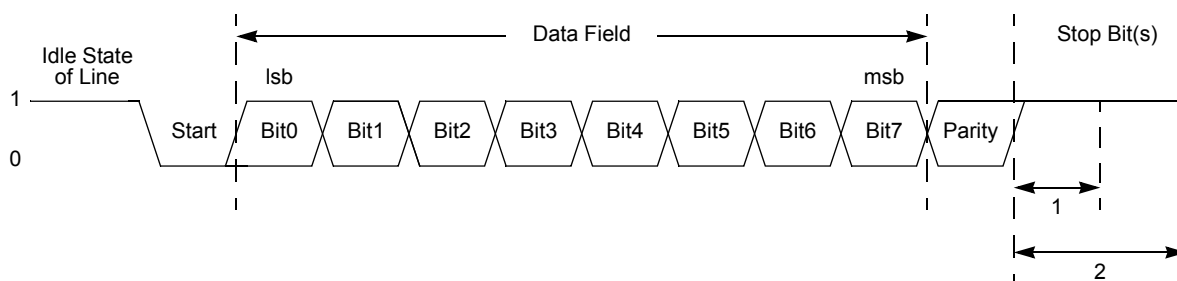
All three Watchdog Timer Reload registers must be written in the order just listed. There must be no other register writes between each of these operations. If a register write occurs, the lock state machine resets and no further writes can occur unless the sequence is restarted. The value in the Watchdog Timer Reload registers is loaded into the counter when the Watchdog Timer is first enabled and every time a WDT instruction is executed.

## Watchdog Timer Calibration

Due to its extremely low operating current, the Watchdog Timer oscillator is somewhat inaccurate. This variation can be corrected using the calibration data stored in the Flash Information Page (see [Table 97](#) and [Table 98](#) on page 165). Loading these values into the



**Figure 11. UART Asynchronous Data Format without Parity**



**Figure 12. UART Asynchronous Data Format with Parity**

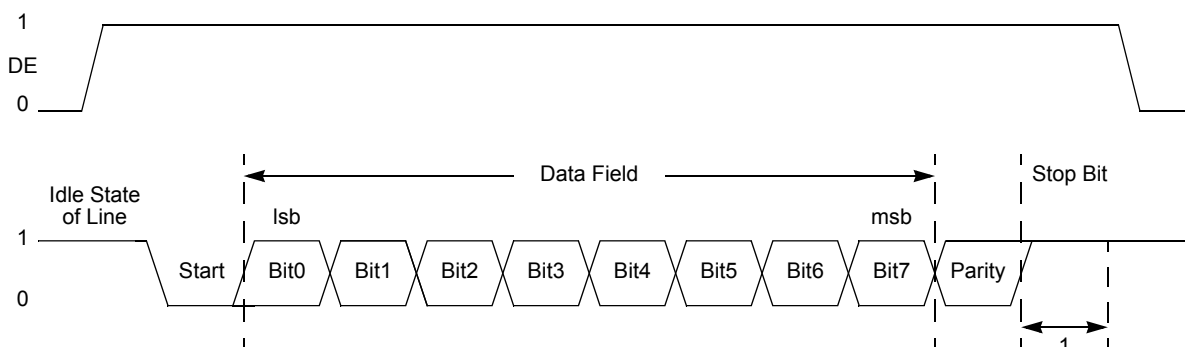
## Transmitting Data using the Polled Method

Follow the steps below to transmit data using the polled method of operation:

1. Write to the UART Baud Rate High and Low Byte registers to set the required baud rate.
2. Enable the UART pin functions by configuring the associated GPIO Port pins for alternate function operation.
3. Write to the UART Control 1 register, if MULTIPROCESSOR mode is appropriate, to enable MULTIPROCESSOR (9-bit) mode functions.
4. Set the Multiprocessor Mode Select (MPEN) bit to enable MULTIPROCESSOR mode.
5. Write to the UART Control 0 register to:
  - Set the transmit enable bit (TEN) to enable the UART for data transmission.
  - Set the parity enable bit (PEN), if parity is appropriate and MULTIPROCESSOR mode is not enabled, and select either even or odd parity (PSEL).
  - Set or clear the CTSE bit to enable or disable control from the remote receiver using the  $\overline{\text{CTS}}$  pin.



Driver Enable is an active High signal that envelopes the entire transmitted data frame including parity and Stop bits as displayed in Figure 14. The Driver Enable signal asserts when a byte is written to the UART Transmit Data register. The Driver Enable signal asserts at least one UART bit period and no greater than two UART bit periods before the Start bit is transmitted. This allows a setup time to enable the transceiver. The Driver Enable signal deasserts one system clock period after the final Stop bit is transmitted. This one system clock delay allows both time for data to clear the transceiver before disabling it, as well as the ability to determine if another character follows the current character. In the event of back to back characters (new data must be written to the Transmit Data Register before the previous character is completely transmitted) the DE signal is not deasserted between characters. The DEPOL bit in the UART Control Register 1 sets the polarity of the Driver Enable signal.



**Figure 14. UART Driver Enable Signal Timing (shown with 1 Stop Bit and Parity)**

The Driver Enable to Start bit setup time is calculated as follows:

$$\left( \frac{1}{\text{Baud Rate (Hz)}} \right) \leq \text{DE to Start Bit Setup Time (s)} \leq \left( \frac{2}{\text{Baud Rate (Hz)}} \right)$$

## UART Interrupts

The UART features separate interrupts for the transmitter and the receiver. In addition, when the UART primary functionality is disabled, the Baud Rate Generator can also function as a basic timer with interrupt capability.

### Transmitter Interrupts

The transmitter generates a single interrupt when the Transmit Data Register Empty bit (TDRE) is set to 1. This indicates that the transmitter is ready to accept new data for transmission. The TDRE interrupt occurs after the Transmit shift register has shifted the first bit of data out. The Transmit Data register can now be written with the next character to

## Factory Calibration

Devices that have been factory calibrated contain 30 bytes of calibration data in the Flash option bit space. This data consists of 3 bytes for each input mode, one for offset and two for gain correction. For a list of input modes for which calibration data exists, see [Zilog Calibration Data](#) on page 161.

## User Calibration

If you have precision references available, its own external calibration can be performed using any input modes. This calibration data takes into account buffer offset and non-linearity, so it is recommended that this calibration be performed separately for each of the ADC input modes planned for use.

## Manual Offset Calibration

When uncalibrated, the ADC has significant offset (see [Table 135](#) on page 231). Subsequently, manual offset calibration capability is built into the block. When the [ADC Control Register 0](#) sets the input mode (`ANAIN[2:0]`) to MANUAL OFFSET CALIBRATION mode, the differential inputs to the ADC are shorted together by an internal switch. Reading the ADC value at this point produces 0 in an ideal system. The value actually read is the ADC offset. This value can be stored in non-volatile memory (see [Non-Volatile Data Storage](#) on page 169) and accessed by user code to compensate for the input offset error. There is no provision for manual gain calibration.

## Software Compensation Procedure Using Factory Calibration Data

The value read from the ADC high and low byte registers is uncompensated. The user mode software must apply gain and offset correction to this uncompensated value for maximum accuracy. The following equation yields the compensated value:

$$\text{ADC}_{\text{comp}} = (\text{ADC}_{\text{uncomp}} - \text{OFFCAL}) + ((\text{ADC}_{\text{uncomp}} - \text{OFFCAL}) \times \text{GAINCAL}) / 2^{16}$$

where GAINCAL is the gain calibration value, OFFCAL is the offset calibration value and  $\text{ADC}_{\text{uncomp}}$  is the uncompensated value read from the ADC. All values are in two's complement format.



### Note:

*The offset compensation is performed first, followed by the gain compensation. One bit of resolution is lost because of rounding on both the offset and gain computations. As a result the ADC registers read back 13 bits: 1 sign bit, two calibration bits lost to rounding and 10 data bits.*

*Also note that in the second term, the multiplication must be performed before the division by  $2^{16}$ . Otherwise, the second term incorrectly evaluates to zero.*

**Table 80. Flash Page Select Register (FPS)**

BITS	7	6	5	4	3	2	1	0
FIELD	INFO_EN	PAGE						
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FF9H							

INFO\_EN—Information Area Enable

0 = Information Area us not selected.

1 = Information Area is selected. The Information Area is mapped into the Program Memory address space at addresses FE00H through FFFFH.

PAGE—Page Select

This 7-bit field identifies the Flash memory page for Page Erase and page unlocking. Program Memory Address[15:9] = PAGE[6:0]. For the Z8F08xx devices, the upper 3 bits must be zero. For the Z8F04xx devices, the upper 4 bits must be zero. For Z8F02xx devices, the upper 5 bits must always be 0. For the Z8F01xx devices, the upper 6 bits must always be 0.

## Flash Sector Protect Register

The Flash Sector Protect (FPROT) register is shared with the Flash Page Select Register. When the [Flash Control Register](#) is written with 73H followed by 5EH, the next write to this address targets the Flash Sector Protect Register. In all other cases, it targets the Flash Page Select Register.

This register selects one of the 8 available Flash memory sectors to be protected. The reset state of each Sector Protect bit is an unprotected state. After a sector is protected by setting its corresponding register bit, it cannot be unprotected (the register bit cannot be cleared) without powering down the device.

**Table 81. Flash Sector Protect Register (FPROT)**

BITS	7	6	5	4	3	2	1	0
FIELD	SPROT7	SPROT6	SPROT5	SPROT4	SPROT3	SPROT2	SPROT1	SPROT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FF9H							

# Crystal Oscillator

The products in the Z8 Encore! XP<sup>®</sup> F082A Series contain an on-chip crystal oscillator for use with external crystals with 32 kHz to 20 MHz frequencies. In addition, the oscillator supports external RC networks with oscillation frequencies up to 4 MHz or ceramic resonators with frequencies up to 8 MHz. The on-chip crystal oscillator can be used to generate the primary system clock for the internal eZ8 CPU and the majority of the on-chip peripherals. Alternatively, the X<sub>IN</sub> input pin can also accept a CMOS-level clock input signal (32 kHz–20 MHz). If an external clock generator is used, the X<sub>OUT</sub> pin must be left unconnected. The Z8 Encore! XP F082A Series products do not contain an internal clock divider. The frequency of the signal on the X<sub>IN</sub> input pin determines the frequency of the system clock.

► **Note:** *Although the XIN pin can be used as an input for an external clock generator, the CLKIN pin is better suited for such use (see [System Clock Selection](#) on page 187).*

## Operating Modes

The Z8 Encore! XP F082A Series products support four oscillator modes:

- Minimum power for use with very low frequency crystals (32 kHz–1 MHz).
- Medium power for use with medium frequency crystals or ceramic resonators (0.5 MHz to 8 MHz).
- Maximum power for use with high frequency crystals (8 MHz to 20 MHz).
- On-chip oscillator configured for use with external RC networks (<4 MHz).

The oscillator mode is selected using user-programmable Flash Option Bits. See [Flash Option Bits](#) on page 153 for information.

## Crystal Oscillator Operation

The Flash Option bit XTLDIS controls whether the crystal oscillator is enabled during reset. The crystal may later be disabled after reset if a new oscillator has been selected as the system clock. If the crystal is manually enabled after reset through the OSCCTL register, the user code must wait at least 1000 crystal oscillator cycles for the crystal to stabilize. After this, the crystal oscillator may be selected as the system clock.

► **Note:** *The stabilization time varies depending on the crystal or resonator used, as well as on the feedback network. See [Table 111](#) for transconductance values to compute oscillator stabilization times.*

**Table 117. Bit Manipulation Instructions**

<b>Mnemonic</b>	<b>Operands</b>	<b>Instruction</b>
BCLR	bit, dst	Bit Clear
BIT	p, bit, dst	Bit Set or Clear
BSET	bit, dst	Bit Set
BSWAP	dst	Bit Swap
CCF	—	Complement Carry Flag
RCF	—	Reset Carry Flag
SCF	—	Set Carry Flag
TCM	dst, src	Test Complement Under Mask
TCMX	dst, src	Test Complement Under Mask using Extended Addressing
TM	dst, src	Test Under Mask
TMX	dst, src	Test Under Mask using Extended Addressing

**Table 118. Block Transfer Instructions**

<b>Mnemonic</b>	<b>Operands</b>	<b>Instruction</b>
LDCI	dst, src	Load Constant to/from Program Memory and Auto-Increment Addresses
LDEI	dst, src	Load External Data to/from Data Memory and Auto-Increment Addresses

**Table 119. CPU Control Instructions**

<b>Mnemonic</b>	<b>Operands</b>	<b>Instruction</b>
ATM	—	Atomic Execution
CCF	—	Complement Carry Flag
DI	—	Disable Interrupts
EI	—	Enable Interrupts
HALT	—	Halt Mode
NOP	—	No Operation
RCF	—	Reset Carry Flag



**Table 130. Internal Precision Oscillator Electrical Characteristics**

		$V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$ $T_A = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$ (unless otherwise stated)				
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions
$F_{IPO}$	Internal Precision Oscillator Frequency (High Speed)		5.53		MHz	$V_{DD} = 3.3 \text{ V}$ $T_A = 30 \text{ }^{\circ}\text{C}$
$F_{IPO}$	Internal Precision Oscillator Frequency (Low Speed)		32.7		kHz	$V_{DD} = 3.3 \text{ V}$ $T_A = 30 \text{ }^{\circ}\text{C}$
$F_{IPO}$	Internal Precision Oscillator Error		$\pm 1$	$\pm 4$	%	
$T_{IPOST}$	Internal Precision Oscillator Startup Time		3		$\mu\text{s}$	

**Table 135. Analog-to-Digital Converter Electrical Characteristics and Timing (Continued)**

		$V_{DD} = 3.0\text{ V to }3.6\text{ V}$ $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$ (unless otherwise stated)				
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions
	Single-Shot Conversion Time	–	5129	–	System clock cycles	All measurements but temperature sensor cycles
			10258			Temperature sensor measurement
	Continuous Conversion Time	–	256	–	System clock cycles	All measurements but temperature sensor cycles
			512			Temperature sensor measurement
	Signal Input Bandwidth	–	10		kHz	As defined by -3 dB point
$R_S$	Analog Source Impedance <sup>4</sup>	–	–	10	k $\Omega$	In unbuffered mode
				500	k $\Omega$	In buffered modes
$Z_{in}$	Input Impedance	–	150		k $\Omega$	In unbuffered mode at 20 MHz <sup>5</sup>
				10	M $\Omega$	In buffered modes
$V_{in}$	Input Voltage Range	0		$V_{DD}$	V	Unbuffered Mode
		0.3		$V_{DD}-1.1$	V	Buffered Modes

► **Note:** *These values define the range over which the ADC performs within spec; exceeding these values does not cause damage or instability; see [DC Characteristics](#) on page 222 for absolute pin voltage limits*

**Notes**

1. Analog source impedance affects the ADC offset voltage (because of pin leakage) and input settling time.
2. Devices are factory calibrated at  $V_{DD} = 3.3\text{ V}$  and  $T_A = +30\text{ }^{\circ}\text{C}$ , so the ADC is maximally accurate under these conditions.
3. LSBs are defined assuming 10-bit resolution.
4. This is the maximum recommended resistance seen by the ADC input pin.
5. The input impedance is inversely proportional to the system clock frequency.



## General Purpose I/O Port Output Timing

Figure 35 and Table 140 provide timing information for GPIO Port pins.

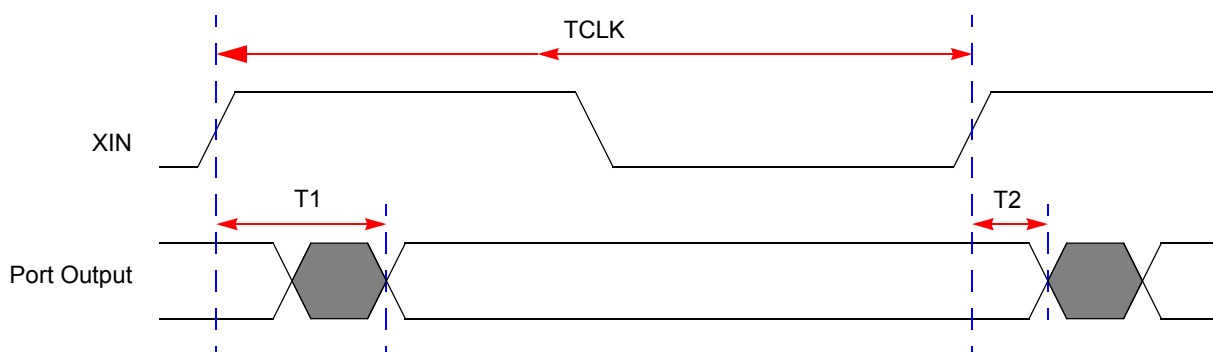


Figure 35. GPIO Port Output Timing

Table 140. GPIO Port Output Timing

Parameter	Abbreviation	Delay (ns)	
		Minimum	Maximum
GPIO Port pins			
T <sub>1</sub>	XIN Rise to Port Output Valid Delay	–	15
T <sub>2</sub>	XIN Rise to Port Output Hold Time	2	–

Figure 38 and Table 143 provide timing information for UART pins for the case where CTS is not used for flow control. DE asserts after the transmit data register has been written. DE remains asserted for multiple characters as long as the transmit data register is written with the next character before the current character has completed.

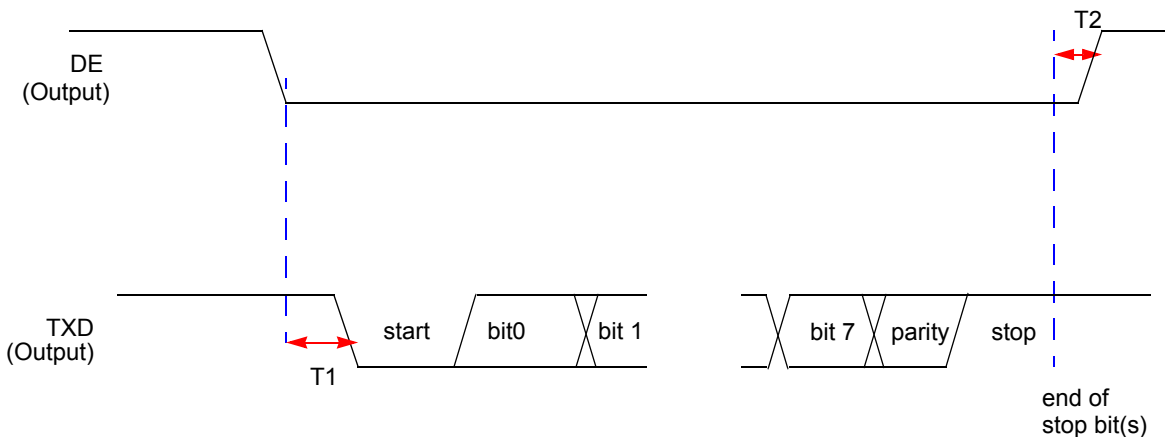


Figure 38. UART Timing Without CTS

Table 143. UART Timing Without CTS

Parameter	Abbreviation	Delay (ns)	
		Minimum	Maximum
UART			
T <sub>1</sub>	DE assertion to TXD falling edge (start bit) delay	1 * XIN period	1 bit time
T <sub>2</sub>	End of Stop Bit(s) to DE deassertion delay (Tx data register is empty)	± 5	

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
<b>Z8 Encore! XP<sup>®</sup> F082A Series with 2 KB Flash, 10-Bit Analog-to-Digital Converter</b>											
<b>Standard Temperature: 0 °C to 70 °C</b>											
Z8F022APB020SC	2 KB	512 B	64 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F022AQB020SC	2 KB	512 B	64 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F022ASB020SC	2 KB	512 B	64 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F022ASH020SC	2 KB	512 B	64 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F022AHH020SC	2 KB	512 B	64 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F022APH020SC	2 KB	512 B	64 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F022ASJ020SC	2 KB	512 B	64 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F022AHJ020SC	2 KB	512 B	64 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F022APJ020SC	2 KB	512 B	64 B	23	20	2	8	1	1	1	PDIP 28-pin package
<b>Extended Temperature: -40 °C to 105 °C</b>											
Z8F022APB020EC	2 KB	512 B	64 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F022AQB020EC	2 KB	512 B	64 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F022ASB020EC	2 KB	512 B	64 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F022ASH020EC	2 KB	512 B	64 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F022AHH020EC	2 KB	512 B	64 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F022APH020EC	2 KB	512 B	64 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F022ASJ020EC	2 KB	512 B	64 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F022AHJ020EC	2 KB	512 B	64 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F022APJ020EC	2 KB	512 B	64 B	23	20	2	8	1	1	1	PDIP 28-pin package
Replace C with G for Lead-Free Packaging											

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
<b>Z8 Encore! XP<sup>®</sup> F082A Series with 1 KB Flash, 10-Bit Analog-to-Digital Converter</b>											
<b>Standard Temperature: 0 °C to 70 °C</b>											
Z8F012APB020SC	1 KB	256 B	16 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F012AQB020SC	1 KB	256 B	16 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F012ASB020SC	1 KB	256 B	16 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F012ASH020SC	1 KB	256 B	16 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F012AHH020SC	1 KB	256 B	16 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F012APH020SC	1 KB	256 B	16 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F012ASJ020SC	1 KB	256 B	16 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F012AHJ020SC	1 KB	256 B	16 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F012APJ020SC	1 KB	256 B	16 B	23	20	2	8	1	1	1	PDIP 28-pin package
<b>Extended Temperature: -40 °C to 105 °C</b>											
Z8F012APB020EC	1 KB	256 B	16 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F012AQB020EC	1 KB	256 B	16 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F012ASB020EC	1 KB	256 B	16 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F012ASH020EC	1 KB	256 B	16 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F012AHH020EC	1 KB	256 B	16 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F012APH020EC	1 KB	256 B	16 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F012ASJ020EC	1 KB	256 B	16 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F012AHJ020EC	1 KB	256 B	16 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F012APJ020EC	1 KB	256 B	16 B	23	20	2	8	1	1	1	PDIP 28-pin package
Replace C with G for Lead-Free Packaging											

- electrical characteristics and timing 230, 233
- interrupt in normal operation 92
- interrupt in STOP mode 92
- operation 135
- refresh 92, 205
- reload unlock sequence 93
- reload upper, high and low registers 94
- reset 27
- reset in normal operation 93
- reset in STOP mode 93
- time-out response 92
- WDTCTL register 31, 94, 136, 190
- WDTH register 95
- WDTL register 95
- working register 201
- working register pair 201
- WTDU register 95

## **X**

- X 201
- XOR 206
- XORX 206

## **Z**

- Z8 Encore!
  - block diagram 4
  - features 1
  - part selection guide 2