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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f021ash020sc

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### Table 18. Port A–D Control Registers (PxCTL)

BITS	7	6	5	4	3	2	1	0
FIELD	PCTL							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR			FI	D1H, FD5H,	FD9H, FDD	H		

PCTL[7:0]—Port Control

The Port Control register provides access to all sub-registers that configure the GPIO Port operation.

# Port A–D Data Direction Sub-Registers

The Port A–D Data Direction sub-register is accessed through the Port A–D Control register by writing 01H to the Port A–D Address register (Table 19).

BITS	7	6	5	4	3	2	1	0
FIELD	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	lf 01H i	n Port A–D /	Address Reg	gister, acces	sible throug	n the Port A-	-D Control F	Register

## Table 19. Port A–D Data Direction Sub-Registers (PxDD)

### DD[7:0]—Data Direction

These bits control the direction of the associated port pin. Port Alternate Function operation overrides the Data Direction register setting.

0 = Output. Data in the Port A–D Output Data register is driven onto the port pin.

1 = Input. The port pin is sampled and the value written into the Port A–D Input Data Register. The output driver is tristated.

# Port A–D Alternate Function Sub-Registers

The Port A–D Alternate Function sub-register (Table 20) is accessed through the Port A–D Control register by writing 02H to the Port A–D Address register. The Port A–D Alternate Function sub-registers enable the alternate function selection on pins. If disabled, pins functions as GPIO. If enabled, select one of four alternate functions using alternate function set subregisters 1 and 2 as described in the Port A–D Alternate Function



function). (Push-pull output)

1 = The source current for the associated pin is disabled (open-drain mode).

### Port A–D High Drive Enable Sub-Registers

The Port A–D High Drive Enable sub-register (Table 22) is accessed through the Port A–D Control register by writing 04H to the Port A–D Address register. Setting the bits in the Port A–D High Drive Enable sub-registers to 1 configures the specified port pins for high current output drive operation. The Port A–D High Drive Enable sub-register affects the pins directly and, as a result, alternate functions are also affected.

Table 22. Port A–D High Drive Enable Sub-Registers (PxHDE)

BITS	7	6	5	4	3	2	1	0	
FIELD	PHDE7	PHDE6	PHDE5	PHDE4	PHDE3	PHDE2	PHDE1	PHDE0	
RESET	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ADDR	lf 04H i	If 04H in Port A–D Address Register, accessible through the Port A–D Control Register							

PHDE[7:0]—Port High Drive Enabled

0 = The Port pin is configured for standard output current drive.

1 = The Port pin is configured for high output current drive.

### Port A–D Stop Mode Recovery Source Enable Sub-Registers

The Port A–D Stop Mode Recovery Source Enable sub-register (Table 23) is accessed through the Port A–D Control register by writing 05H to the Port A–D Address register. Setting the bits in the Port A–D Stop Mode Recovery Source Enable sub-registers to 1 configures the specified Port pins as a Stop Mode Recovery source. During STOP mode, any logic transition on a Port pin enabled as a Stop Mode Recovery source initiates Stop Mode Recovery.

Table 23. Port A–D Stop Mode Recove	ry Source Enable Sub-Registers (PxSMRE)
-------------------------------------	---

BITS	7	6	5	4	3	2	1	0
FIELD	PSMRE7	PSMRE6	PSMRE5	PSMRE4	PSMRE3	PSMRE2	PSMRE1	PSMRE0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	lf 05H i	n Port A–D	Address Reg	gister, acces	sible throug	n the Port A-	-D Control F	Register

PSMRE[7:0]—Port Stop Mode Recovery Source Enabled

0 = The Port pin is not configured as a Stop Mode Recovery source. Transitions on this pin



Interrupts are globally enabled by any of the following actions:

- Execution of an EI (Enable Interrupt) instruction
- Execution of an IRET (Return from Interrupt) instruction
- Writing a 1 to the IRQE bit in the Interrupt Control register

Interrupts are globally disabled by any of the following actions:

- Execution of a DI (Disable Interrupt) instruction
- eZ8 CPU acknowledgement of an interrupt service request from the interrupt controller
- Writing a 0 to the IRQE bit in the Interrupt Control register
- Reset
- Execution of a Trap instruction
- Illegal Instruction Trap
- Primary Oscillator Fail Trap
- Watchdog Oscillator Fail Trap

### **Interrupt Vectors and Priority**

The interrupt controller supports three levels of interrupt priority. Level 3 is the highest priority, Level 2 is the second highest priority, and Level 1 is the lowest priority. If all of the interrupts are enabled with identical interrupt priority (all as Level 2 interrupts, for example), the interrupt priority is assigned from highest to lowest as specified in Table 32 on page 56. Level 3 interrupts are always assigned higher priority than Level 2 interrupts which, in turn, always are assigned higher priority than Level 1 interrupts. Within each interrupt priority level (Level 1, Level 2, or Level 3), priority is assigned as specified in Table 32, above. Reset, Watchdog Timer interrupt (if enabled), Primary Oscillator Fail Trap, Watchdog Oscillator Fail Trap, and Illegal Instruction Trap always have highest (level 3) priority.

### **Interrupt Assertion**

Interrupt sources assert their interrupt requests for only a single system clock period (single pulse). When the interrupt request is acknowledged by the eZ8 CPU, the corresponding bit in the Interrupt Request register is cleared until the next interrupt occurs. Writing a 0 to the corresponding bit in the Interrupt Request register likewise clears the interrupt request.



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### Interrupt Request 2 Register

The Interrupt Request 2 (IRQ2) register (Table 35) stores interrupt requests for both vectored and polled interrupts. When a request is presented to the interrupt controller, the corresponding bit in the IRQ2 register becomes 1. If interrupts are globally enabled (vectored interrupts), the interrupt controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU can read the Interrupt Request 2 register to determine if any interrupt requests are pending.

### Table 35. Interrupt Request 2 Register (IRQ2)

BITS	7	6	5	4	3	2	1	0
FIELD		Rese	erved		PC3I	PC2I	PC1I	PC0I
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR				FC	6H			

Reserved—Must be 0.

PCxI—Port C Pin x Interrupt Request

0 = No interrupt request is pending for GPIO Port C pin x.

1 = An interrupt request from GPIO Port C pin x is awaiting service.

where x indicates the specific GPIO Port C pin number (0-3).

## **IRQ0 Enable High and Low Bit Registers**

Table 36 describes the priority control for IRQ0. The IRQ0 Enable High and Low Bit registers (Table 37 and Table 38) form a priority encoded enabling for interrupts in the Interrupt Request 0 register.

### Table 36. IRQ0 Enable and Priority Encoding

IRQ0ENH[x]	IRQ0ENL[x]	Priority	Description
0	0	Disabled	Disabled
0	1	Level 1	Low
1	0	Level 2	Medium
1	1	Level 3	High

where x indicates the register bits from 0–7.



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### **CAPTURE RESTART mode**

0 = Count is captured on the rising edge of the Timer Input signal. 1 = Count is captured on the falling edge of the Timer Input signal.

# COMPARATOR COUNTER mode

When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload. Also:

0 = Count is captured on the rising edge of the comparator output. 1 = Count is captured on the falling edge of the comparator output.

**Caution:** When the Timer Output alternate function TxOUT on a GPIO port pin is enabled, TxOUT changes to whatever state the TPOL bit is in. The timer does not need to be enabled for that to happen. Also, the Port data direction sub register is not needed to be set to output on TxOUT. Changing the TPOL bit with the timer enabled and running does not immediately change the TxOUT.

#### PRES—Prescale value

The timer input clock is divided by  $2^{PRES}$ , where PRES can be set from 0 to 7. The prescaler is reset each time the Timer is disabled. This reset ensures proper clock division each time the Timer is restarted.

000 = Divide by 1 001 = Divide by 2 010 = Divide by 4 011 = Divide by 8 100 = Divide by 16 101 = Divide by 32 110 = Divide by 64 111 = Divide by 128

#### TMODE—Timer mode

This field along with the TMODEHI bit in TxCTL0 register determines the operating mode of the timer. TMODEHI is the most significant bit of the Timer mode selection value. The entire operating mode bits are expressed as {TMODEHI, TMODE[2:0]}. The TMODEHI is bit 7 of the TxCTL0 register while TMODE[2:0] is the lower 3 bits of the TxCTL1 register.

- 0000 = ONE-SHOT mode
- 0001 = CONTINUOUS mode
- 0010 = COUNTER mode
- 0011 = PWM SINGLE OUTPUT mode
- 0100 = CAPTURE mode
- 0101 = COMPARE mode
- 0110 = GATED mode
- 0111 = CAPTURE/COMPARE mode



Watchdog Timer Reload Registers results in a one-second timeout at room temperature and 3.3 V supply voltage.

Timeouts other than one second may be obtained by scaling the calibration values up or down as required.

**Note:** *The Watchdog Timer accuracy still degrades as temperature and supply voltage vary. See* Table 133 on page 230 *for* details.

# Watchdog Timer Control Register Definitions

### Watchdog Timer Control Register

The Watchdog Timer Control (WDTCTL) register is a write-only control register. Writing the 55H, AAH unlock sequence to the WDTCTL register address unlocks the three Watchdog Timer Reload Byte registers (WDTU, WDTH, and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL register address produce no effect on the bits in the WDTCTL register. The locking mechanism prevents spurious writes to the Reload registers.

This register address is shared with the read-only Reset Status register.

BITS	7	6	5	4	3	2	1	0	
FIELD	WDTUNLK								
RESET	Х	Х	Х	Х	Х	Х	Х	Х	
R/W	W	W	W	W	W	W	W	W	
ADDR	FF0H								
X = Undef	ined.								

### Table 57. Watchdog Timer Control Register (WDTCTL)

WDTUNLK—Watchdog Timer Unlock

The software must write the correct unlocking sequence to this register before it is allowed to modify the contents of the Watchdog Timer reload registers.

## Watchdog Timer Reload Upper, High and Low Byte Registers

The Watchdog Timer Reload Upper, High and Low Byte (WDTU, WDTH, WDTL) registers (Table 58 through Table 60) form the 24-bit reload value that is loaded into the Watchdog Timer when a WDT instruction executes. The 24-bit reload value is {WDTU[7:0], WDTH[7:0]}. Writing to these registers sets the appropriate Reload Value. Reading from these registers returns the current Watchdog Timer count value.

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- 6. Check the TDRE bit in the UART Status 0 register to determine if the Transmit Data register is empty (indicated by a 1). If empty, continue to Step 7. If the Transmit Data register is full (indicated by a 0), continue to monitor the TDRE bit until the Transmit Data register becomes available to receive new data.
- 7. Write the UART Control 1 register to select the outgoing address bit.
- 8. Set the Multiprocessor Bit Transmitter (MPBT) if sending an address byte, clear it if sending a data byte.
- 9. Write the data byte to the UART Transmit Data register. The transmitter automatically transfers the data to the Transmit Shift register and transmits the data.
- 10. Make any changes to the Multiprocessor Bit Transmitter (MPBT) value, if appropriate and MULTIPROCESSOR mode is enabled.
- 11. To transmit additional bytes, return to Step 5.

### Transmitting Data using the Interrupt-Driven Method

The UART Transmitter interrupt indicates the availability of the Transmit Data register to accept new data for transmission. Follow the steps below to configure the UART for interrupt-driven data transmission:

- 1. Write to the UART Baud Rate High and Low Byte registers to set the appropriate baud rate.
- 2. Enable the UART pin functions by configuring the associated GPIO Port pins for alternate function operation.
- 3. Execute a DI instruction to disable interrupts.
- 4. Write to the Interrupt control registers to enable the UART Transmitter interrupt and set the acceptable priority.
- 5. Write to the UART Control 1 register to enable MULTIPROCESSOR (9-bit) mode functions, if MULTIPROCESSOR mode is appropriate.
- 6. Set the MULTIPROCESSOR Mode Select (MPEN) to Enable MULTIPROCESSOR mode.
- 7. Write to the UART Control 0 register to:
  - Set the transmit enable bit (TEN) to enable the UART for data transmission.
  - Enable parity, if appropriate and if MULTIPROCESSOR mode is not enabled, and select either even or odd parity.
  - Set or clear CTSE to enable or disable control from the remote receiver using the  $\overline{\text{CTS}}$  pin.
- 8. Execute an EI instruction to enable interrupts.



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3.579545 MHz System Clock								
Acceptable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)					
1250.0	N/A	N/A	N/A					
625.0	N/A	N/A	N/A					
250.0	1	223.72	-10.51					
115.2	2	111.9	-2.90					
57.6	4	55.9	-2.90					
38.4	6	37.3	-2.90					
19.2	12	18.6	-2.90					
9.60	23	9.73	1.32					
4.80	47	4.76	-0.83					
2.40	93	2.41	0.23					
1.20	186	1.20	0.23					
0.60	373	0.60	-0.04					
0.30	746	0.30	-0.04					
-								

### Table 70. UART Baud Rates (Continued)

1.8432 MHz \$	System Clock		
Acceptable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)
1250.0	N/A	N/A	N/A
625.0	N/A	N/A	N/A
250.0	N/A	N/A	N/A
115.2	1	115.2	0.00
57.6	2	57.6	0.00
38.4	3	38.4	0.00
19.2	6	19.2	0.00
9.60	12	9.60	0.00
4.80	24	4.80	0.00
2.40	48	2.40	0.00
1.20	96	1.20	0.00
0.60	192	0.60	0.00
0.30	384	0.30	0.00



# **Trim Bit Data Register**

The Trim Bid Data (TRMDR) register contains the read or write data for access to the trim option bits (Table 85).

## Table 85. Trim Bit Data Register (TRMDR)

BITS	7	6	5	4	3	2	1	0		
FIELD	TRMDR - Trim Bit Data									
RESET	0	0	0	0	0	0	0	0		
R/W	R/W         R/W									
ADDR	FF7H									

# Flash Option Bit Address Space

The first two bytes of Flash program memory at addresses 0000H and 0001H are reserved for the user-programmable Flash option bits.

# Flash Program Memory Address 0000H

 Table 86. Flash Option Bits at Program Memory Address 0000H

BITS	7	6	5	4	3	2	1	0
FIELD	WDT_RES	WDT_AO	OSC_SEL[1:0]		VBO_AO	FRP	Reserved	FWP
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	Program Memory 0000H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

WDT\_RES—Watchdog Timer Reset

0 = Watchdog Timer time-out generates an interrupt request. Interrupts must be globally enabled for the eZ8 CPU to acknowledge the interrupt request.

1 = Watchdog Timer time-out causes a system reset. This setting is the default for unprogrammed (erased) Flash.

WDT\_AO—Watchdog Timer Always On

0 = Watchdog Timer is automatically enabled upon application of system power. Watchdog Timer can not be disabled.



# **On-Chip Debugger**

The Z8 Encore! XP<sup>®</sup> F082A Series devices contain an integrated On-Chip Debugger (OCD) that provides advanced debugging features including:

- Single pin interface.
- Reading and writing of the register file.
- Reading and writing of program and data memory.
- Setting of breakpoints and watchpoints.
- Executing eZ8 CPU instructions.
- Debug pin sharing with general-purpose input-output function to maximize pins available to the user (8-pin product only).

# Architecture

The on-chip debugger consists of four primary functional blocks: transmitter, receiver, auto-baud detector/generator, and debug controller. Figure 23 displays the architecture of the on-chip debugger.



Figure 23. On-Chip Debugger Block Diagram





### Figure 25. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface (2)

### **DEBUG Mode**

The operating characteristics of the devices in DEBUG mode are:

- The eZ8 CPU fetch unit stops, idling the eZ8 CPU, unless directed by the OCD to execute specific instructions.
- The system clock operates unless in STOP mode.
- All enabled on-chip peripherals operate unless in STOP mode.
- Automatically exits HALT mode.
- Constantly refreshes the Watchdog Timer, if enabled.

### **Entering DEBUG Mode**

The operating characteristics of the devices entering DEBUG mode are:

- The device enters DEBUG mode after the eZ8 CPU executes a BRK (Breakpoint) instruction.
- If the DBG pin is held Low during the final clock cycle of system reset, the part enters DEBUG mode immediately (20-/28-pin products only).
- **Note:** Holding the DBG pin Low for an additional 5000 (minimum) clock cycles after reset (making sure to account for any specified frequency error if using an internal oscillator) prevents a false interpretation of an Autobaud sequence (see OCD Auto-Baud Detector/Generator on page 176).

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Write Memory, Read Memory, Write Register, Read Register, Read Memory CRC, Step Instruction, Stuff Instruction, and Execute Instruction commands.

DBG  $\leftarrow$  03H DBG  $\rightarrow$  RuntimeCounter[15:8] DBG  $\rightarrow$  RuntimeCounter[7:0]

• Write OCD Control Register (04H)—The Write OCD Control Register command writes the data that follows to the OCDCTL register. When the Flash Read Protect Option Bit is enabled, the DBGMODE bit (OCDCTL[7]) can only be set to 1, it cannot be cleared to 0 and the only method of returning the device to normal operating mode is to reset the device.

DBG  $\leftarrow$  04H DBG  $\leftarrow$  OCDCTL[7:0]

• **Read OCD Control Register (05H)**—The Read OCD Control Register command reads the value of the OCDCTL register.

```
DBG \leftarrow 05H
DBG \rightarrow OCDCTL[7:0]
```

• Write Program Counter (06H)—The Write Program Counter command writes the data that follows to the eZ8 CPU's Program Counter (PC). If the device is not in DE-BUG mode or if the Flash Read Protect Option bit is enabled, the Program Counter (PC) values are discarded.

```
DBG ← 06H
DBG ← ProgramCounter[15:8]
DBG ← ProgramCounter[7:0]
```

• **Read Program Counter (07H)**—The Read Program Counter command reads the value in the eZ8 CPU's Program Counter (PC). If the device is not in DEBUG mode or if the Flash Read Protect Option bit is enabled, this command returns FFFFH.

```
DBG \leftarrow 07H
DBG \rightarrow ProgramCounter[15:8]
DBG \rightarrow ProgramCounter[7:0]
```

• Write Register (08H)—The Write Register command writes data to the Register File. Data can be written 1–256 bytes at a time (256 bytes can be written by setting size to 0). If the device is not in DEBUG mode, the address and data values are discarded. If the Flash Read Protect Option bit is enabled, only writes to the Flash Control Registers are allowed and all other register write data values are discarded.

```
DBG \leftarrow 08H
DBG \leftarrow {4'h0,Register Address[11:8]}
DBG \leftarrow Register Address[7:0]
DBG \leftarrow Size[7:0]
DBG \leftarrow 1-256 data bytes
```



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WDFEN-Watchdog Timer Oscillator Failure Detection Enable

1 = Failure detection of Watchdog Timer oscillator is enabled

0 = Failure detection of Watchdog Timer oscillator is disabled

SCKSEL—System Clock Oscillator Select

000 = Internal precision oscillator functions as system clock at 5.53 MHz

001 = Internal precision oscillator functions as system clock at 32 kHz

010 = Crystal oscillator or external RC oscillator functions as system clock

011 = Watchdog Timer oscillator functions as system

100 = External clock signal on PB3 functions as system clock

101 = Reserved

110 = Reserved

111 = Reserved

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Figure 27 displays a recommended configuration for connection with an external fundamental-mode, parallel-resonant crystal operating at 20 MHz. Recommended 20 MHz crystal specifications are provided in Table 110. Printed circuit board layout must add no more than 4 pF of stray capacitance to either the X<sub>IN</sub> or X<sub>OUT</sub> pins. If oscillation does not occur, reduce the values of capacitors C<sub>1</sub> and C<sub>2</sub> to decrease loading.



### Figure 27. Recommended 20 MHz Crystal Oscillator Configuration

Table 110. Rec	commended Cr	ystal Osc	illator S	pecifications
----------------	--------------	-----------	-----------	---------------

Parameter	Value	Units	Comments
Frequency	20	MHz	
Resonance	Parallel		
Mode	Fundamental		
Series Resistance (R <sub>S</sub> )	60	Ω	Maximum
Load Capacitance (C <sub>L</sub> )	30	pF	Maximum
Shunt Capacitance (C <sub>0</sub> )	7	pF	Maximum
Drive Level	1	mW	Maximum



# **Opcode Maps**

A description of the opcode map data and the abbreviations are provided in Figure 30. Figure 31 and Figure 32 displays the eZ8 CPU instructions. Table 125 lists Opcode Map abbreviations.



Figure 30. Opcode Map Cell Description



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	V <sub>DD</sub> - T <sub>A</sub> = - (unless	= 2.7 V to 40 °C to + otherwis	● 3.6 V •105 °C e stated)		
Parameter	Minimum	Typical	Maximum	Units	Notes
Flash Byte Read Time	100	_	_	ns	
Flash Byte Program Time	20	_	40	μs	
Flash Page Erase Time	10	-	-	ms	
Flash Mass Erase Time	200	-	-	ms	
Writes to Single Address Before Next Erase	-	-	2		
Flash Row Program Time	-	-	8	ms	Cumulative program time for single row cannot exceed limit before next erase. This parameter is only an issue when bypassing the Flash Controller.
Data Retention	100	_	_	years	25 °C
Endurance	10,000	_	_	cycles	Program/erase cycles

### Table 132. Flash Memory Electrical Characteristics and Timing

### Table 133. Watchdog Timer Electrical Characteristics and Timing

V <sub>DD</sub> = 2.7 V to 3.6 V
T <sub>A</sub> = -40 °C to +105 °C
(unless otherwise stated)

Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions
F <sub>WDT</sub>	WDT Oscillator Frequency		10		kHz	
F <sub>WDT</sub>	WDT Oscillator Error			<u>+</u> 50	%	
T <sub>WDTCAL</sub>	WDT Calibrated Timeout	0.98	1	1.02	S	V <sub>DD</sub> = 3.3 V; T <sub>A</sub> = 30 °C
		0.70	1	1.30	S	V <sub>DD</sub> = 2.7 V to 3.6 V T <sub>A</sub> = 0 °C to 70 °C
		0.50	1	1.50	S	$V_{DD} = 2.7 V \text{ to } 3.6 V$ $T_A = -40 \text{ °C to } +105 \text{ °C}$



# Packaging

Figure 39 displays the 8-pin Plastic Dual Inline Package (PDIP) available for Z8 Encore!  $XP^{\textcircled{R}}$  F082A Series devices.



Figure 39. 8-Pin Plastic Dual Inline Package (PDIP)



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