**What is "Embedded - Microcontrollers"?**

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

**Applications of "Embedded - Microcontrollers"**

## Details

| | |
|---|---|
| Product Status | Obsolete |
| Core Processor | eZ8 |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | IrDA, UART/USART |
| Peripherals | Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT |
| Number of I/O | 25 |
| Program Memory Size | 2KB (2K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 64 x 8 |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8f021asj020ec00tr |

operational amplifier (LPO) is OFF. To use the LPO, clear the LPO bit, turning it ON. Clearing this bit might interfere with normal ADC measurements on ANA0 (the LPO output). This bit enables the amplifier even in STOP mode. If the amplifier is not required in STOP mode, disable it. Failure to perform this results in STOP mode currents greater than specified.

> **Note:** *This register is only reset during a POR sequence. Other system reset events do not affect it.*

**Table 12. Power Control Register 0 (PWRCTL0)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|---|---|
| FIELD | LPO | Reserved | | VBO | TEMP | ADC | COMP | Reserved |
| RESET | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| ADDR | F80H | | | | | | | |

LPO—Low-Power Operational Amplifier Disable
0 = LPO is enabled (this applies even in STOP mode).
1 = LPO is disabled.

Reserved—Must be 0.

VBO—Voltage Brownout Detector Disable
This bit and the VBO_AO Flash option bit must both enable the VBO for the VBO to be active.
0 = VBO Enabled
1 = VBO Disabled

TEMP—Temperature Sensor Disable
0 = Temperature Sensor Enabled
1 = Temperature Sensor Disabled

ADC—Analog-to-Digital Converter Disable
0 = Analog-to-Digital Converter Enabled
1 = Analog-to-Digital Converter Disabled

COMP—Comparator Disable
0 = Comparator is Enabled
1 = Comparator is Disabled

Reserved—Must be 0.

> **Note:** *Asserting any power control bit disables the targeted block, regardless of any enable bits contained in the target block's control registers.*

**Table 46. Shared Interrupt Select Register (IRQSS)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | PA7VS | PA6CS | Reserved | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| ADDR | FCEH | | | | | | | |

PA7VS—PA7/LVD Selection
0 = PA7 is used for the interrupt for PA7VS interrupt request.
1 = The LVD is used for the interrupt for PA7VS interrupt request.

PA6CS—PA6/Comparator Selection
0 = PA6 is used for the interrupt for PA6CS interrupt request.
1 = The Comparator is used for the interrupt for PA6CS interrupt request.

Reserved—Must be 0.

## Interrupt Control Register

The Interrupt Control (IRQCTL) register (Table 47) contains the master enable bit for all interrupts.

**Table 47. Interrupt Control Register (IRQCTL)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | IRQE | Reserved | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R | R | R | R | R | R | R |
| ADDR | FCFH | | | | | | | |

IRQE—Interrupt Request Enable
This bit is set to 1 by executing an EI (Enable Interrupts) or IRET (Interrupt Return) instruction, or by a direct register write of a 1 to this bit. It is reset to 0 by executing a DI instruction, eZ8 CPU acknowledgement of an interrupt request, Reset or by a direct register write of a 0 to this bit.
0 = Interrupts are disabled.
1 = Interrupts are enabled.

Reserved—Must be 0.

### PWM DUAL OUTPUT Mode

In PWM DUAL OUTPUT mode, the timer outputs a Pulse-Width Modulated (PWM) output signal pair (basic PWM signal and its complement) through two GPIO Port pins. The timer input is the system clock. The timer first counts up to the 16-bit PWM match value stored in the Timer PWM High and Low Byte registers. When the timer count value matches the PWM value, the Timer Output toggles. The timer continues counting until it reaches the Reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the Reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to `0001H` and counting resumes.

If the `TPOL` bit in the Timer Control register is set to 1, the Timer Output signal begins as a High (1) and transitions to a Low (0) when the timer value matches the PWM value. The Timer Output signal returns to a High (1) after the timer reaches the Reload value and is reset to `0001H`.

If the `TPOL` bit in the Timer Control register is set to 0, the Timer Output signal begins as a Low (0) and transitions to a High (1) when the timer value matches the PWM value. The Timer Output signal returns to a Low (0) after the timer reaches the Reload value and is reset to `0001H`.

The timer also generates a second PWM output signal Timer Output Complement. The Timer Output Complement is the complement of the Timer Output PWM signal. A programmable deadband delay can be configured to time delay (0 to 128 system clock cycles) PWM output transitions on these two pins from a low to a high (inactive to active). This ensures a time gap between the deassertion of one PWM output to the assertion of its complement.

Follow the steps below for configuring a timer for PWM DUAL OUTPUT mode and initiating the PWM operation:

1. Write to the Timer Control register to:
   – Disable the timer.
   – Configure the timer for PWM DUAL OUTPUT mode by writing the TMODE bits in the TxCTL1 register and the TMODEHI bit in TxCTL0 register.
   – Set the prescale value.
   – Set the initial logic level (High or Low) and PWM High/Low transition for the Timer Output alternate function.

2. Write to the Timer High and Low Byte registers to set the starting count value (typically `0001H`). This only affects the first pass in PWM mode. After the first timer reset in PWM mode, counting always begins at the reset value of `0001H`.

3. Write to the PWM High and Low Byte registers to set the PWM value.

4. Write to the PWM Control register to set the PWM dead band delay value. The deadband delay must be less than the duration of the positive phase of the PWM signal (as defined by the PWM high and low byte registers). It must also be less than the

## Watchdog Timer Refresh

When first enabled, the Watchdog Timer is loaded with the value in the Watchdog Timer Reload registers. The Watchdog Timer counts down to `000000H` unless a WDT instruction is executed by the eZ8 CPU. Execution of the WDT instruction causes the downcounter to be reloaded with the WDT Reload value stored in the Watchdog Timer Reload registers. Counting resumes following the reload operation.

When the Z8 Encore! XP® F082A Series devices are operating in DEBUG mode (using the on-chip debugger), the Watchdog Timer is continuously refreshed to prevent any Watchdog Timer time-outs.

## Watchdog Timer Time-Out Response

The Watchdog Timer times out when the counter reaches `000000H`. A time-out of the Watchdog Timer generates either an interrupt or a system reset. The WDT_RES Flash Option Bit determines the time-out response of the Watchdog Timer. For information on programming the WDT_RES Flash Option Bit, see Flash Option Bits on page 153.

### WDT Interrupt in Normal Operation

If configured to generate an interrupt when a time-out occurs, the Watchdog Timer issues an interrupt request to the interrupt controller and sets the `WDT` status bit in the Reset Status (RSTSTAT) register (see Reset Status Register on page 30). If interrupts are enabled, the eZ8 CPU responds to the interrupt request by fetching the Watchdog Timer interrupt vector and executing code from the vector address. After time-out and interrupt generation, the Watchdog Timer counter rolls over to its maximum value of `FFFFFH` and continues counting. The Watchdog Timer counter is not automatically returned to its Reload Value.

The Reset Status (RSTSTAT) register must be read before clearing the WDT interrupt. This read clears the WDT timeout Flag and prevents further WDT interrupts from immediately occurring.

### WDT Interrupt in STOP Mode

If configured to generate an interrupt when a time-out occurs and the Z8 Encore! XP F082A Series devices are in STOP mode, the Watchdog Timer automatically initiates a Stop Mode Recovery and generates an interrupt request. Both the WDT status bit and the `STOP` bit in the Reset Status (RSTSTAT) register are set to 1 following a WDT time-out in STOP mode. For more information on Stop Mode Recovery, see Reset, Stop Mode Recovery, and Low Voltage Detection on page 23.

If interrupts are enabled, following completion of the Stop Mode Recovery the eZ8 CPU responds to the interrupt request by fetching the Watchdog Timer interrupt vector and executing code from the vector address.

⚠ **Caution:** *The 24-bit WDT Reload Value must not be set to a value less than* `000004H`.

**Table 58. Watchdog Timer Reload Upper Byte Register (WDTU)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | WDTU | | | | | | | |
| RESET | 00H | | | | | | | |
| R/W | R/W* | | | | | | | |
| ADDR | FF1H | | | | | | | |
| R/W* - Read returns the current WDT count value. Write sets the appropriate Reload Value. | | | | | | | | |

WDTU—WDT Reload Upper Byte
Most-significant byte (MSB), Bits[23:16], of the 24-bit WDT reload value.

**Table 59. Watchdog Timer Reload High Byte Register (WDTH)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | WDTH | | | | | | | |
| RESET | 04H | | | | | | | |
| R/W | R/W* | | | | | | | |
| ADDR | FF2H | | | | | | | |
| R/W* - Read returns the current WDT count value. Write sets the appropriate Reload Value. | | | | | | | | |

WDTH—WDT Reload High Byte
Middle byte, Bits[15:8], of the 24-bit WDT reload value.

**Table 60. Watchdog Timer Reload Low Byte Register (WDTL)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | WDTL | | | | | | | |
| RESET | 00H | | | | | | | |
| R/W | R/W* | | | | | | | |
| ADDR | FF3H | | | | | | | |
| R/W* - Read returns the current WDT count value. Write sets the appropriate Reload Value. | | | | | | | | |

WDTL—WDT Reload Low

Least significant byte (LSB), Bits[7:0], of the 24-bit WDT reload value.
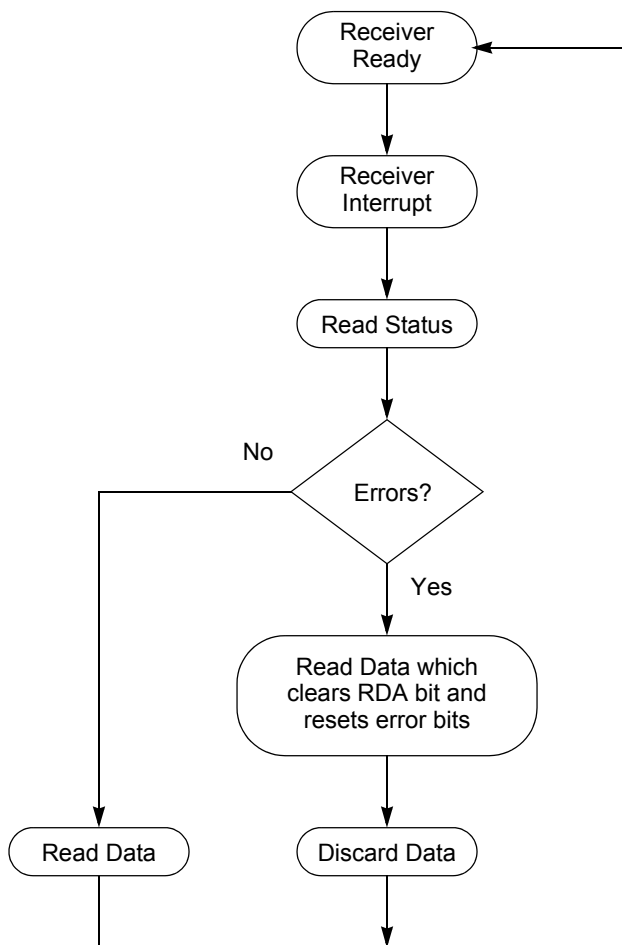
**Figure 15. UART Receiver Interrupt Service Routine Flow**

### Baud Rate Generator Interrupts

If the baud rate generator (BRG) interrupt enable is set, the UART Receiver interrupt asserts when the UART Baud Rate Generator reloads. This condition allows the Baud Rate Generator to function as an additional counter if the UART functionality is not employed.

## UART Baud Rate Generator

The UART Baud Rate Generator creates a lower frequency baud rate clock for data transmission. The input to the Baud Rate Generator is the system clock. The UART Baud Rate High and Low Byte registers combine to create a 16-bit baud rate divisor value

1001 = 1.8 V
1010–1111 = Reserved

For 8-pin devices:

000000 = 0.00 V
000001 = 0.05 V
000010 = 0.10 V
000011 = 0.15 V
000100 = 0.20 V
000101 = 0.25 V
000110 = 0.30 V
000111 = 0.35 V
001000 = 0.40 V
001001 = 0.45 V
001010 = 0.50 V
001011 = 0.55 V
001100 = 0.60 V
001101 = 0.65 V
001110 = 0.70 V
001111 = 0.75 V
010000 = 0.80 V
010001 = 0.85 V
010010 = 0.90 V
010011 = 0.95 V
010100 = 1.00 V (Default)
010101 = 1.05 V
010110 = 1.10 V
010111 = 1.15 V
011000 = 1.20 V
011001 = 1.25 V
011010 = 1.30 V
011011 = 1.35 V
011100 = 1.40 V
011101 = 1.45 V
011110 = 1.50 V
011111 = 1.55 V
100000 = 1.60 V
100001 = 1.65 V
100010 = 1.70 V
100011 = 1.75 V
100100 = 1.80 V

# Temperature Sensor

The on-chip Temperature Sensor allows you to measure temperature on the die with either the on-board ADC or on-board comparator. This block is factory calibrated for in-circuit software correction. Uncalibrated accuracy is significantly worse, therefore the temperature sensor is not recommended for uncalibrated use.

## Temperature Sensor Operation

The on-chip temperature sensor is a Proportional to Absolute Temperature (PTAT) topology. A pair of Flash option bytes contain the calibration data. The temperature sensor can be disabled by a bit in the Power Control Register 0 on page 34 to reduce power consumption.

The temperature sensor can be directly read by the ADC to determine the absolute value of its output. The temperature sensor output is also available as an input to the comparator for threshold type measurement determination. The accuracy of the sensor when used with the comparator is substantially less than when measured by the ADC.

If the temperature sensor is routed to the ADC, the ADC must be configured in unity-gain buffered mode (see Input Buffer Stage on page 129) The value read back from the ADC is a signed number, although it is always positive.

The sensor is factory-trimmed through the ADC using the external 2.0 V reference. Unless the sensor is re-trimmed for use with a different reference, it is most accurate when used with the external 2.0 V reference.

Because this sensor is an on-chip sensor it is recommended that the user account for the difference between ambient and die temperature when inferring ambient temperature conditions.

During normal operation, the die undergoes heating that causes a mismatch between the ambient temperature and that measured by the sensor. For best results, the Z8 Encore! XP® device must be placed into STOP mode for sufficient time such that the die and ambient temperatures converge (this time is dependent on the thermal design of the system). The temperature sensor measurement must then be made immediately after recovery from STOP mode.

The following equation defines the transfer function between the temperature sensor output voltage and the die temperature. This is needed for comparator threshold measurements.

$$V = 0.01 \times T + 0.65$$

where, T is the temperature in °C; V is the sensor output in volts.

value `63H` to the Flash Control register initiates the Mass Erase operation. While the Flash Controller executes the Mass Erase operation, the eZ8 CPU idles but the system clock and on-chip peripherals continue to operate. Using the On-Chip Debugger, poll the Flash Status register to determine when the Mass Erase operation is complete. When the Mass Erase is complete, the Flash Controller returns to its locked state.

## Flash Controller Bypass

The Flash Controller can be bypassed and the control signals for the Flash memory brought out to the GPIO pins. Bypassing the Flash Controller allows faster Row Programming algorithms by controlling the Flash programming signals directly.

Row programming is recommended for gang programming applications and large volume customers who do not require in-circuit initial programming of the Flash memory. Page Erase operations are also supported when the Flash Controller is bypassed.

For more information on bypassing the Flash Controller, refer to *Third-Party Flash Programming Support for Z8 Encore!® MCU Application Note (AN0117)* available for download at www.zilog.com.

## Flash Controller Behavior in DEBUG Mode

The following changes in behavior of the Flash Controller occur when the Flash Controller is accessed using the On-Chip Debugger:

- The Flash Write Protect option bit is ignored.

- The Flash Sector Protect register is ignored for programming and erase operations.

- Programming operations are not limited to the page selected in the Page Select register.

- Bits in the Flash Sector Protect register can be written to one or zero.

- The second write of the Page Select register to unlock the Flash Controller is not necessary.

- The Page Select register can be written when the Flash Controller is unlocked.

- The Mass Erase command is enabled through the Flash Control register.

⚠ **Caution:** *For security reasons, the Flash controller allows only a single page to be opened for write/erase. When writing multiple Flash pages, the flash controller must go through the unlock sequence again to select another page.*

# Flash Option Bits

Programmable Flash option bits allow user configuration of certain aspects of Z8 Encore! XP® F082A Series operation. The feature configuration data is stored in the Flash program memory and loaded into holding registers during Reset. The features available for control through the Flash Option Bits include:

- Watchdog Timer time-out response selection–interrupt or system reset

- Watchdog Timer always on (enabled at Reset)

- The ability to prevent unwanted read access to user code in Program Memory

- The ability to prevent accidental programming and erasure of all or a portion of the user code in Program Memory

- Voltage Brownout configuration-always enabled or disabled during STOP mode to reduce STOP mode power consumption

- Oscillator mode selection-for high, medium, and low power crystal oscillators, or external RC oscillator

- Factory trimming information for the internal precision oscillator and low voltage detection

- Factory calibration values for ADC, temperature sensor, and Watchdog Timer compensation

- Factory serialization and randomized lot identifier (optional)

## Operation

### Option Bit Configuration By Reset

Each time the Flash Option Bits are programmed or erased, the device must be Reset for the change to take effect. During any reset operation (System Reset, Power-On Reset, or Stop Mode Recovery), the Flash Option Bits are automatically read from the Flash Program Memory and written to Option Configuration registers. The Option Configuration registers control operation of the devices within the Z8 Encore! XP F082A Series. Option Bit control is established before the device exits Reset and the eZ8 CPU begins code execution. The Option Configuration registers are not part of the Register File and are not accessible for read or write access.

WDTCALH—Watchdog Timer Calibration High Byte
The WDTCALH and WDTCALL bytes, when loaded into the Watchdog Timer reload
registers result in a one second timeout at room temperature and 3.3 V supply voltage. To
use the Watchdog Timer calibration, user code must load WDTU with 0x00, WDTH with
WDTCALH and WDTL with WDTCALL.

**Table 98. Watchdog Calibration Low Byte at 007FH (WDTCALL)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|---|---|
| FIELD | WDTCALL | | | | | | | |
| RESET | U | U | U | U | U | U | U | U |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| ADDR | Information Page Memory 007FH | | | | | | | |
| **Note:** U = Unchanged by Reset. R/W = Read/Write. | | | | | | | | |

WDTCALL—Watchdog Timer Calibration Low Byte
The WDTCALH and WDTCALL bytes, when loaded into the Watchdog Timer reload
registers result in a one second timeout at room temperature and 3.3 V supply voltage. To
use the Watchdog Timer calibration, user code must load WDTU with 0x00, WDTH with
WDTCALH and WDTL with WDTCALL.

## Serialization Data

**Table 99. Serial Number at 001C - 001F (S_NUM)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|---|---|
| FIELD | S_NUM | | | | | | | |
| RESET | U | U | U | U | U | U | U | U |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| ADDR | Information Page Memory 001C-001F | | | | | | | |
| **Note:** U = Unchanged by Reset. R/W = Read/Write. | | | | | | | | |

S_NUM—Serial Number Byte
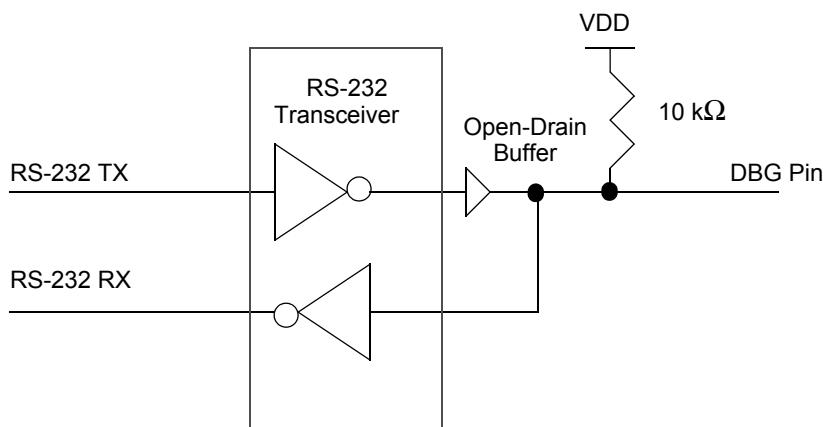The serial number is a unique four-byte binary value.

**Figure 25. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface (2)**

## DEBUG Mode

The operating characteristics of the devices in DEBUG mode are:

- The eZ8 CPU fetch unit stops, idling the eZ8 CPU, unless directed by the OCD to execute specific instructions.

- The system clock operates unless in STOP mode.

- All enabled on-chip peripherals operate unless in STOP mode.

- Automatically exits HALT mode.

- Constantly refreshes the Watchdog Timer, if enabled.

### Entering DEBUG Mode

The operating characteristics of the devices entering DEBUG mode are:

- The device enters DEBUG mode after the eZ8 CPU executes a BRK (Breakpoint) instruction.

- If the DBG pin is held Low during the final clock cycle of system reset, the part enters DEBUG mode immediately (20-/28-pin products only).

▶ **Note:** *Holding the DBG pin Low for an additional 5000 (minimum) clock cycles after reset (making sure to account for any specified frequency error if using an internal oscillator) prevents a false interpretation of an Autobaud sequence (see* OCD Auto-Baud Detector/ Generator *on page 176).*

## Table 114. Notational Shorthand

| Notation | Description | Operand | Range |
|---|---|---|---|
| b | Bit | b | b represents a value from 0 to 7 (000B to 111B). |
| cc | Condition Code | — | Refer to Condition Codes section in the *eZ8 CPU Core User Manual (UM0128)*. |
| DA | Direct Address | Addrs | Addrs. represents a number in the range of 0000H to FFFFH |
| ER | Extended Addressing Register | Reg | Reg. represents a number in the range of 000H to FFFH |
| IM | Immediate Data | #Data | Data is a number between 00H to FFH |
| Ir | Indirect Working Register | @Rn | n = 0–15 |
| IR | Indirect Register | @Reg | Reg. represents a number in the range of 00H to FFH |
| Irr | Indirect Working Register Pair | @RRp | p = 0, 2, 4, 6, 8, 10, 12, or 14 |
| IRR | Indirect Register Pair | @Reg | Reg. represents an even number in the range 00H to FEH |
| p | Polarity | p | Polarity is a single bit binary value of either 0B or 1B. |
| r | Working Register | Rn | n = 0 – 15 |
| R | Register | Reg | Reg. represents a number in the range of 00H to FFH |
| RA | Relative Address | X | X represents an index in the range of +127 to –128 which is an offset relative to the address of the next instruction |
| rr | Working Register Pair | RRp | p = 0, 2, 4, 6, 8, 10, 12, or 14 |
| RR | Register Pair | Reg | Reg. represents an even number in the range of 00H to FEH |
| Vector | Vector Address | Vector | Vector represents a number in the range of 00H to FFH |
| X | Indexed | #Index | The register or register pair to be indexed is offset by the signed Index value (#Index) in a +127 to -128 range. |

Table 115 lists additional symbols that are used throughout the Instruction Summary and Instruction Set Description sections.

**Table 121. Logical Instructions (Continued)**

| Mnemonic | Operands | Instruction |
|----------|----------|-------------|
| ORX | dst, src | Logical OR using Extended Addressing |
| XOR | dst, src | Logical Exclusive OR |
| XORX | dst, src | Logical Exclusive OR using Extended Addressing |

**Table 122. Program Control Instructions**

| Mnemonic | Operands | Instruction |
|----------|----------|-------------|
| BRK | — | On-Chip Debugger Break |
| BTJ | p, bit, src, DA | Bit Test and Jump |
| BTJNZ | bit, src, DA | Bit Test and Jump if Non-Zero |
| BTJZ | bit, src, DA | Bit Test and Jump if Zero |
| CALL | dst | Call Procedure |
| DJNZ | dst, src, RA | Decrement and Jump Non-Zero |
| IRET | — | Interrupt Return |
| JP | dst | Jump |
| JP cc | dst | Jump Conditional |
| JR | DA | Jump Relative |
| JR cc | DA | Jump Relative Conditional |
| RET | — | Return |
| TRAP | vector | Software Trap |

**Table 123. Rotate and Shift Instructions**

| Mnemonic | Operands | Instruction |
|----------|----------|-------------|
| BSWAP | dst | Bit Swap |
| RL | dst | Rotate Left |
| RLC | dst | Rotate Left through Carry |
| RR | dst | Rotate Right |
| RRC | dst | Rotate Right through Carry |

**Table 136. Low Power Operational Amplifier Electrical Characteristics**

| Symbol | Parameter | $V_{DD}$ = 2.7 V to 3.6 V $T_A$ = -40 °C to +105 °C | | | Units | Conditions |
| | | Minimum | Typical | Maximum | | |
|---|---|---|---|---|---|---|
| Av | Open loop voltage gain | | 80 | | dB | |
| GBW | Gain/Bandwidth product | | 500 | | kHz | |
| PM | Phase Margin | | 50 | | deg | Assuming 13 pF load capacitance |
| $V_{osLPO}$ | Input Offset Voltage | | $\pm1$ | $\pm4$ | mV | |
| $V_{osLPO}$ | Input Offset Voltage (Temperature Drift) | | 1 | 10 | µV/C | |
| $V_{IN}$ | Input Voltage Range | 0.3 | | Vdd - 1 | V | |
| $V_{OUT}$ | Output Voltage Range | 0.3 | | Vdd - 1 | V | $I_{OUT}$ = 45 µA |

**Table 137. Comparator Electrical Characteristics**

| Symbol | Parameter | $V_{DD}$ = 2.7 V to 3.6 V $T_A$ = -40 °C to +105 °C | | | Units | Conditions |
| | | Minimum | Typical | Maximum | | |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Input DC Offset | | 5 | | mV | |
| $V_{CREF}$ | Programmable Internal Reference Voltage | | $\pm5$ | | % | 20-/28-pin devices |
| | | | $\pm3$ | | % | 8-pin devices |
| $T_{PROP}$ | Propagation Delay | | 200 | | ns | |
| $V_{HYS}$ | Input Hysteresis | | 4 | | mV | |
| $V_{IN}$ | Input Voltage Range | $V_{SS}$ | | $V_{DD}$-1 | V | |

# Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at http://www.zilog.com/kb.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at http://support.zilog.com.