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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	23
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f022ahj020ec

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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tions as a GPIO pin. If it is not present, the debug feature is disabled until/unless another reset event occurs. For more details, see On-Chip Debugger on page 173.

Crystal Oscillator Override

For systems using a crystal oscillator, PA0 and PA1 are used to connect the crystal. When the crystal oscillator is enabled (see Oscillator Control Register Definitions on page 190), the GPIO settings are overridden and PA0 and PA1 are disabled.

5 V Tolerance

All six I/O pins on the 8-pin devices are 5 V-tolerant, unless the programmable pull-ups are enabled. If the pull-ups are enabled and inputs higher than V_{DD} are applied to these parts, excessive current flows through those pull-up devices and can damage the chip.

Note: In the 20- and 28-pin versions of this device, any pin which shares functionality with an ADC, crystal or comparator port is not 5 V-tolerant, including PA[1:0], PB[5:0] and PC[2:0]. All other signal pins are 5 V-tolerant, and can safely handle inputs higher than V_{DD} except when the programmable pull-ups are enabled.

External Clock Setup

For systems using an external TTL drive, PB3 is the clock source for 20- and 28-pin devices. In this case, configure PB3 for alternate function CLKIN. Write the Oscillator Control (OSCCTL) register (see Oscillator Control Register Definitions on page 190) such that the external oscillator is selected as the system clock. For 8-pin devices use PA1 instead of PB3.

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Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port B	PB0	Reserved		AFS1[0]: 0
		ANA0/AMPOUT	ADC Analog Input/LPO Output	AFS1[0]: 1
	PB1	Reserved		AFS1[1]: 0
		ANA1/AMPINN	ADC Analog Input/LPO Input (N)	AFS1[1]: 1
	PB2	Reserved		AFS1[2]: 0
		ANA2/AMPINP	ADC Analog Input/LPO Input (P)	AFS1[2]: 1
-	PB3	CLKIN	External Clock Input	AFS1[3]: 0
		ANA3	ADC Analog Input	AFS1[3]: 1
	PB4	Reserved		AFS1[4]: 0
		ANA7	ADC Analog Input	AFS1[4]: 1
	PB5	Reserved		AFS1[5]: 0
		VREF*	ADC Voltage Reference	AFS1[5]: 1
	PB6	Reserved		AFS1[6]: 0
		Reserved		AFS1[6]: 1
	PB7	Reserved		AFS1[7]: 0
		Reserved		AFS1[7]: 1

Table 14. Port Alternate Function Mapping (Non 8-Pin Parts) (Continued)

Note: Because there are at most two choices of alternate function for any pin of Port B, the Alternate Function Set register AFS2 is not used to select the function. Also, alternate function selection as described in Port A-D Alternate Function Sub-Registers on page 47 must also be enabled.

* VREF is available on PB5 in 28-pin products only.



function). (Push-pull output)

1 = The source current for the associated pin is disabled (open-drain mode).

Port A–D High Drive Enable Sub-Registers

The Port A–D High Drive Enable sub-register (Table 22) is accessed through the Port A–D Control register by writing 04H to the Port A–D Address register. Setting the bits in the Port A–D High Drive Enable sub-registers to 1 configures the specified port pins for high current output drive operation. The Port A–D High Drive Enable sub-register affects the pins directly and, as a result, alternate functions are also affected.

Table 22. Port A–D High Drive Enable Sub-Registers (PxHDE)

BITS	7	6	5	4	3	2	1	0		
FIELD	PHDE7	PHDE6	PHDE5	PHDE4	PHDE3	PHDE2	PHDE1	PHDE0		
RESET	0	0	0	0	0	0	0	0		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
ADDR	lf 04H i	If 04H in Port A–D Address Register, accessible through the Port A–D Control Register								

PHDE[7:0]—Port High Drive Enabled

0 = The Port pin is configured for standard output current drive.

1 = The Port pin is configured for high output current drive.

Port A–D Stop Mode Recovery Source Enable Sub-Registers

The Port A–D Stop Mode Recovery Source Enable sub-register (Table 23) is accessed through the Port A–D Control register by writing 05H to the Port A–D Address register. Setting the bits in the Port A–D Stop Mode Recovery Source Enable sub-registers to 1 configures the specified Port pins as a Stop Mode Recovery source. During STOP mode, any logic transition on a Port pin enabled as a Stop Mode Recovery source initiates Stop Mode Recovery.

Table 23. Port A–D Stop Mode Recove	ry Source Enable Sub-Registers (PxSMRE)
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BITS	7	6	5	4	3	2	1	0			
FIELD	PSMRE7	PSMRE6	PSMRE5	PSMRE4	PSMRE3	PSMRE2	PSMRE1	PSMRE0			
RESET	0	0	0	0	0	0	0	0			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
ADDR	lf 05H i	If 05H in Port A–D Address Register, accessible through the Port A–D Control Register									

PSMRE[7:0]—Port Stop Mode Recovery Source Enabled

0 = The Port pin is not configured as a Stop Mode Recovery source. Transitions on this pin



Figure 9. Timer Block Diagram

Operation

The timers are 16-bit up-counters. Minimum time-out delay is set by loading the value 0001H into the Timer Reload High and Low Byte registers and setting the prescale value to 1. Maximum time-out delay is set by loading the value 0000H into the Timer Reload High and Low Byte registers and setting the prescale value to 128. If the Timer reaches FFFFH, the timer rolls over to 0000H and continues counting.

Timer Operating Modes

The timers can be configured to operate in the following modes:

ONE-SHOT Mode

In ONE-SHOT mode, the timer counts up to the 16-bit Reload value stored in the Timer Reload High and Low byte registers. The timer input is the system clock. Upon reaching the Reload value, the timer generates an interrupt and the count value in the Timer High and Low Byte registers is reset to 0001H. The timer is automatically disabled and stops counting.

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Z8 Encore! XP[®] F082A Series

Product Specification



- Set the prescale value.
- If using the Timer Output alternate function, set the initial output level (High or Low).
- 2. Write to the Timer High and Low Byte registers to set the starting count value (usually 0001H). This action only affects the first pass in CONTINUOUS mode. After the first timer Reload in CONTINUOUS mode, counting always begins at the reset value of 0001H.
- 3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
- 4. Enable the timer interrupt (if appropriate) and set the timer interrupt priority by writing to the relevant interrupt registers.
- 5. Configure the associated GPIO port pin (if using the Timer Output function) for the Timer Output alternate function.
- 6. Write to the Timer Control register to enable the timer and initiate counting.

In CONTINUOUS mode, the system clock always provides the timer input. The timer period is given by the following equation:

CONTINUOUS Mode Time-Out Period (s) = $\frac{\text{Reload Value} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, use the ONE-SHOT mode equation to determine the first time-out period.

COUNTER Mode

In COUNTER mode, the timer counts input transitions from a GPIO port pin. The timer input is taken from the GPIO Port pin Timer Input alternate function. The TPOL bit in the Timer Control Register selects whether the count occurs on the rising edge or the falling edge of the Timer Input signal. In COUNTER mode, the prescaler is disabled.

Caution: The input frequency of the Timer Input signal must not exceed one-fourth the system clock frequency. Further, the high or low state of the input signal pulse must be no less than twice the system clock period. A shorter pulse may not be captured.

Upon reaching the Reload value stored in the Timer Reload High and Low Byte registers, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer Reload.



Follow the steps below for configuring a timer for COMPARATOR COUNTER mode and initiating the count:

- 1. Write to the Timer Control register to:
 - Disable the timer.
 - Configure the timer for COMPARATOR COUNTER mode.
 - Select either the rising edge or falling edge of the comparator output signal for the count. This also sets the initial logic level (High or Low) for the Timer Output alternate function. However, the Timer Output function is not required to be enabled.
- 2. Write to the Timer High and Low Byte registers to set the starting count value. This action only affects the first pass in COMPARATOR COUNTER mode. After the first timer Reload in COMPARATOR COUNTER mode, counting always begins at the reset value of 0001H. Generally, in COMPARATOR COUNTER mode the Timer High and Low Byte registers must be written with the value 0001H.
- 3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
- 4. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
- 5. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
- 6. Write to the Timer Control register to enable the timer.

In COMPARATOR COUNTER mode, the number of comparator output transitions since the timer start is given by the following equation:

Comparator Output Transitions = Current Count Value – Start Value

PWM SINGLE OUTPUT Mode

In PWM SINGLE OUTPUT mode, the timer outputs a Pulse-Width Modulator (PWM) output signal through a GPIO Port pin. The timer input is the system clock. The timer first counts up to the 16-bit PWM match value stored in the Timer PWM High and Low Byte registers. When the timer count value matches the PWM value, the Timer Output toggles. The timer continues counting until it reaches the Reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the Reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes.

If the TPOL bit in the Timer Control register is set to 1, the Timer Output signal begins as a High (1) and transitions to a Low (0) when the timer value matches the PWM value. The Timer Output signal returns to a High (1) after the timer reaches the Reload value and is reset to 0001H.



Follow the steps below for configuring a timer for COMPARE mode and initiating the count:

- 1. Write to the Timer Control register to:
 - Disable the timer.
 - Configure the timer for COMPARE mode.
 - Set the prescale value.
 - Set the initial logic level (High or Low) for the Timer Output alternate function, if appropriate.
- 2. Write to the Timer High and Low Byte registers to set the starting count value.
- 3. Write to the Timer Reload High and Low Byte registers to set the Compare value.
- 4. Enable the timer interrupt, if appropriate, and set the timer interrupt priority by writing to the relevant interrupt registers.
- 5. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
- 6. Write to the Timer Control register to enable the timer and initiate counting.

In COMPARE mode, the system clock always provides the timer input. The Compare time can be calculated by the following equation:

COMPARE Mode Time (s) = $\frac{(Compare Value - Start Value) \times Prescale}{System Clock Frequency (Hz)}$

GATED Mode

In GATED mode, the timer counts only when the Timer Input signal is in its active state (asserted), as determined by the TPOL bit in the Timer Control register. When the Timer Input signal is asserted, counting begins. A timer interrupt is generated when the Timer Input signal is deasserted or a timer reload occurs. To determine if a Timer Input signal deassertion generated the interrupt, read the associated GPIO input value and compare to the value stored in the TPOL bit.

The timer counts up to the 16-bit Reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. When reaching the Reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes (assuming the Timer Input signal remains asserted). Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer reset.

Follow the steps below for configuring a timer for GATED mode and initiating the count:

- 1. Write to the Timer Control register to:
 - Disable the timer.
 - Configure the timer for GATED mode.
 - Set the prescale value.



1000 = PWM DUAL OUTPUT mode 1001 = CAPTURE RESTART mode 1010 = COMPARATOR COUNTER mode

Timer 0–1 High and Low Byte Registers

The Timer 0–1 High and Low Byte (TxH and TxL) registers (Table 50 and Table 51) contain the current 16-bit timer count value. When the timer is enabled, a read from TxH causes the value in TxL to be stored in a temporary holding register. A read from TxL always returns this temporary register when the timers are enabled. When the timer is disabled, reads from TxL read the register directly.

Writing to the Timer High and Low Byte registers while the timer is enabled is not recommended. There are no temporary holding registers available for write operations, so simultaneous 16-bit writes are not possible. If either the Timer High or Low Byte registers are written during counting, the 8-bit written value is placed in the counter (High or Low Byte) at the next clock edge. The counter continues counting from the new value.

BITS	7	6	5	4	3	2	1	0			
FIELD		TH									
RESET	0	0	0	0	0	0	0	0			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
ADDR				F00H,	F08H						

Table 50. Timer 0–1 High Byte Register (TxH)

Table 51. Timer 0–1 Low Byte Register (TxL)

BITS	7	6	5	4	3	2	1	0			
FIELD		TL									
RESET	0	0	0	0	0	0	0	1			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
ADDR		F01H, F09H									

TH and TL-Timer High and Low Bytes

These 2 bytes, {TH[7:0], TL[7:0]}, contain the current 16-bit timer count value.

Timer Reload High and Low Byte Registers

The Timer 0–1 Reload High and Low Byte (TxRH and TxRL) registers (Table 52 and Table 53) store a 16-bit reload value, {TRH[7:0], TRL[7:0]}. Values written to the Timer Reload High Byte register are stored in a temporary holding register. When a write to the



Caution: *The 24-bit WDT Reload Value must not be set to a value less than* 000004H.

Table 58. Watchdog Timer Reload Upper Byte Register (WDTU)

BITS	7	6	5	4	3	2	1	0			
FIELD		WDTU									
RESET	00H										
R/W		R/W*									
ADDR	FF1H										
R/W/* - Rea	P/W* - Read returns the current WDT count value. Write sets the appropriate Reload Value										

R/W* - Read returns the current WDT count value. Write sets the appropriate Reload Value.

WDTU—WDT Reload Upper Byte

Most-significant byte (MSB), Bits[23:16], of the 24-bit WDT reload value.

Table 59. Watchdog Timer Reload High Byte Register (WDTH)

BITS	7	6	5	4	3	2	1	0				
FIELD		WDTH										
RESET	04H											
R/W				R/	W*							
ADDR	FF2H											
R/W* - Rea	R/W* - Read returns the current WDT count value. Write sets the appropriate Reload Value.											

WDTH—WDT Reload High Byte

Middle byte, Bits[15:8], of the 24-bit WDT reload value.

Table 60. Watchdog Timer Reload Low Byte Register (WDTL)

BITS	7	6	5	4	3	2	1	0				
FIELD		WDTL										
RESET	00H											
R/W				R/	W*							
ADDR	FF3H											
R/W* - Rea	R/W* - Read returns the current WDT count value. Write sets the appropriate Reload Value.											

WDTL—WDT Reload Low

Least significant byte (LSB), Bits[7:0], of the 24-bit WDT reload value.

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Universal Asynchronous Receiver/Transmitter

The universal asynchronous receiver/transmitter (UART) is a full-duplex communication channel capable of handling asynchronous data transfers. The UART uses a single 8-bit data mode with selectable parity. Features of the UART include:

- 8-bit asynchronous data transfer.
- Selectable even- and odd-parity generation and checking.
- Option of one or two STOP bits.
- Separate transmit and receive interrupts.
- Framing, parity, overrun and break detection.
- Separate transmit and receive enables.
- 16-bit baud rate generator (BRG).
- Selectable MULTIPROCESSOR (9-bit) mode with three configurable interrupt schemes.
- Baud rate generator (BRG) can be configured and used as a basic 16-bit timer.
- Driver enable (DE) output for external bus transceivers.

Architecture

The UART consists of three primary functional blocks: transmitter, receiver, and baud rate generator. The UART's transmitter and receiver function independently, but employ the same baud rate and data format. Figure 10 on page 98 displays the UART architecture.



- 3. Write to the ADC Control Register 0 to configure the ADC for continuous conversion. The bit fields in the ADC Control register may be written simultaneously:
 - Write to the ANAIN[3:0] field to select from the available analog input sources (different input pins available depending on the device).
 - Set CONT to 1 to select continuous conversion.
 - If the internal VREF must be output to a pin, set the REFEXT bit to 1. The internal voltage reference must be enabled in this case.
 - Write the REFSELL bit of the pair {REFSELH, REFSELL} to select the internal voltage reference level or to disable the internal reference. The REFSELH bit is contained in ADC Control/Status Register 1.
 - Set CEN to 1 to start the conversions.
- 4. When the first conversion in continuous operation is complete (after 5129 system clock cycles, plus the 40 cycles for power-up, if necessary), the ADC control logic performs the following operations:
 - CEN resets to 0 to indicate the first conversion is complete. CEN remains 0 for all subsequent conversions in continuous operation.
 - An interrupt request is sent to the Interrupt Controller to indicate the conversion is complete.
- 5. The ADC writes a new data result every 256 system clock cycles. For each completed conversion, the ADC control logic performs the following operations:
 - Writes the 13-bit two's complement result to {ADCD_H[7:0], ADCD L[7:3]}.
 - Sends an interrupt request to the Interrupt Controller denoting conversion complete.
- 6. To disable continuous conversion, clear the CONT bit in the ADC Control Register to 0.

Interrupts

The ADC is able to interrupt the CPU when a conversion has been completed. When the ADC is disabled, no new interrupts are asserted; however, an interrupt pending when the ADC is disabled is not cleared.

Calibration and Compensation

The Z8 Encore! XP[®] F082A Series ADC is factory calibrated for offset error and gain error, with the compensation data stored in Flash memory. Alternatively, you can perform your own calibration, storing the values into Flash themselves. Thirdly, the user code can perform a manual offset calibration during DIFFERENTIAL mode operation.

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8 KB Flash		4 KB Flash			
Program Memory	/	Program Memor	у	2 KB Flash	
	Addresses (hex)		Addresses (hex)	Address	y ses (hex)
	1FFF	0	0FFF		^ 707FF
Sector 7	1000	Sector /	0500	Sector 3	0600
	1000				05FF
Sector 6	1BFF	Sector 6	UDFF	Sector 2	0400
Seciol 6	1800	Sector 0	0000		03FF
	1755		OBEE	Sector 1	0200
Sector 5	1/FF	Sector 5	UBFF		0200 01FF
	1400		0A00	Sector 0	
	13FF		09FF		0000
Sector 4		Sector 4			
	1000		0800		
	0FFF		07FF	1 KR Elach	
Sector 3	0000	Sector 3	0600	Program Memor	v
			0600	Address	ses (hex)
Sector 2	0BFF	Sector 2	05FF		03FF
360101 2	0800		0400	Sector 1	
	0766		03FF		0200 01FF
Sector 1	0/11	Sector 1	0011	Sector 0	0
	0400		0200		0000
	03FF		01FF		- 0000
Sector 0		Sector 0			
	0000		0000		

Figure 21. Flash Memory Arrangement

Flash Information Area

The Flash information area is separate from Program Memory and is mapped to the address range FE00H to FFFFH. This area is readable but cannot be erased or overwritten. Factory trim values for the analog peripherals are stored here. Factory calibration data for the ADC is also stored here.



Flash Option Bits

Programmable Flash option bits allow user configuration of certain aspects of Z8 Encore! $XP^{\textcircled{R}}$ F082A Series operation. The feature configuration data is stored in the Flash program memory and loaded into holding registers during Reset. The features available for control through the Flash Option Bits include:

- Watchdog Timer time-out response selection-interrupt or system reset
- Watchdog Timer always on (enabled at Reset)
- The ability to prevent unwanted read access to user code in Program Memory
- The ability to prevent accidental programming and erasure of all or a portion of the user code in Program Memory
- Voltage Brownout configuration-always enabled or disabled during STOP mode to reduce STOP mode power consumption
- Oscillator mode selection-for high, medium, and low power crystal oscillators, or external RC oscillator
- Factory trimming information for the internal precision oscillator and low voltage detection
- Factory calibration values for ADC, temperature sensor, and Watchdog Timer compensation
- Factory serialization and randomized lot identifier (optional)

Operation

Option Bit Configuration By Reset

Each time the Flash Option Bits are programmed or erased, the device must be Reset for the change to take effect. During any reset operation (System Reset, Power-On Reset, or Stop Mode Recovery), the Flash Option Bits are automatically read from the Flash Program Memory and written to Option Configuration registers. The Option Configuration registers control operation of the devices within the Z8 Encore! XP F082A Series. Option Bit control is established before the device exits Reset and the eZ8 CPU begins code execution. The Option Configuration registers are not part of the Register File and are not accessible for read or write access.

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Option Bit Types

User Option Bits

The user option bits are contained in the first two bytes of program memory. User access to these bits has been provided because these locations contain application-specific device configurations. The information contained here is lost when page 0 of the program memory is erased.

Trim Option Bits

The trim option bits are contained in the information page of the Flash memory. These bits are factory programmed values required to optimize the operation of onboard analog circuitry and cannot be permanently altered. Program Memory may be erased without endangering these values. It is possible to alter working values of these bits by accessing the Trim Bit Address and Data Registers, but these working values are lost after a power loss or any other reset event.

There are 32 bytes of trim data. To modify one of these values the user code must first write a value between 00H and 1FH into the Trim Bit Address Register. The next write to the Trim Bit Data register changes the working value of the target trim data byte.

Reading the trim data requires the user code to write a value between 00H and 1FH into the Trim Bit Address Register. The next read from the Trim Bit Data register returns the working value of the target trim data byte.

The trim address range is from information address 20-3F only. The remainder of the information page is not accessible through the trim bit address and data registers.

Calibration Option Bits

The calibration option bits are also contained in the information page. These bits are factory programmed values intended for use in software correcting the device's analog performance. To read these values, the user code must employ the LDC instruction to access the information area of the address space as defined in See Flash Information Area on page 17.

Serialization Bits

As an optional feature, Zilog[®] is able to provide factory-programmed serialization. For serialized products, the individual devices are programmed with unique serial numbers. These serial numbers are binary values, four bytes in length. The numbers increase in size with each device, but gaps in the serial sequence may exist.

These serial numbers are stored in the Flash information page (see Reading the Flash Information Page on page 155 and Serialization Data on page 165 for more details) and are unaffected by mass erasure of the device's Flash memory.

Note:





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Randomized Lot Identification Bits

As an optional feature, Zilog is able to provide a factory-programmed random lot identifier. With this feature, all devices in a given production lot are programmed with the same random number. This random number is uniquely regenerated for each successive production lot and is not likely to be repeated.

The randomized lot identifier is a 32 byte binary value, stored in the Flash information page (see Reading the Flash Information Page on page 155 and Randomized Lot Identifier on page 166 for more details) and is unaffected by mass erasure of the device's Flash memory.

Reading the Flash Information Page

The following code example shows how to read data from the Flash information area.

; get value at info address 60 (FE60h) ldx FPS, #%80 ; enable access to flash info page ld R0, #%FE ld R1, #%60 ldc R2, @RR0 ; R2 now contains the calibration value

Flash Option Bit Control Register Definitions

Trim Bit Address Register

The Trim Bit Address (TRMADR) register contains the target address for an access to the trim option bits (Table 84).

BITS	7	6	5	4	3	2	1	0			
FIELD		TRMADR - Trim Bit Address (00H to 1FH)									
RESET	0	0	0	0	0	0	0	0			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
ADDR	FF6H										

Table 84. Trim Bit Address Register (TRMADR)



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DBGACK—Debug Acknowledge

This bit enables the debug acknowledge feature. If this bit is set to 1, the OCD sends a Debug Acknowledge character (FFH) to the host when a Breakpoint occurs.

0 = Debug Acknowledge is disabled.

1 = Debug Acknowledge is enabled.

Reserved—Must be 0.

RST—Reset

Setting this bit to 1 resets the Z8F04xA family device. The device goes through a normal Power-On Reset sequence with the exception that the On-Chip Debugger is not reset. This bit is automatically cleared to 0 at the end of reset.

0 = No effect.

1 = Reset the Flash Read Protect Option Bit device.

OCD Status Register

The OCD Status register reports status information about the current state of the debugger and the system.

Table 107. OCD Status Register (OCDSTAT)

BITS	7	6	5	4	3	2	1	0	
FIELD	DBG	HALT	FRPENB	Reserved					
RESET	0	0	0	0	0	0	0	0	
R/W	R	R	R	R	R	R	R	R	

DBG—Debug Status

0 = NORMAL mode

1 = DEBUG mode

HALT—HALT Mode

0 =Not in HALT mode

1 =In HALT mode

FRPENB—Flash Read Protect Option Bit Enable

0 = FRP bit enabled, that allows disabling of many OCD commands

1 = FRP bit has no effect

Reserved-Must be 0

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Table 121. Logical Instructions (Continued)

Mnemonic	Operands	Instruction
ORX	dst, src	Logical OR using Extended Addressing
XOR	dst, src	Logical Exclusive OR
XORX	dst, src	Logical Exclusive OR using Extended Addressing

Table 122. Program Control Instructions

Mnemonic	Operands	Instruction
BRK	_	On-Chip Debugger Break
BTJ	p, bit, src, DA	Bit Test and Jump
BTJNZ	bit, src, DA	Bit Test and Jump if Non-Zero
BTJZ	bit, src, DA	Bit Test and Jump if Zero
CALL	dst	Call Procedure
DJNZ	dst, src, RA	Decrement and Jump Non-Zero
IRET	_	Interrupt Return
JP	dst	Jump
JP cc	dst	Jump Conditional
JR	DA	Jump Relative
JR cc	DA	Jump Relative Conditional
RET	_	Return
TRAP	vector	Software Trap

Table 123. Rotate and Shift Instructions

Mnemonic	Operands	Instruction
BSWAP	dst	Bit Swap
RL	dst	Rotate Left
RLC	dst	Rotate Left through Carry
RR	dst	Rotate Right
RRC	dst	Rotate Right through Carry



Opcode Maps

A description of the opcode map data and the abbreviations are provided in Figure 30. Figure 31 and Figure 32 displays the eZ8 CPU instructions. Table 125 lists Opcode Map abbreviations.



Figure 30. Opcode Map Cell Description



		V _{DD} = 2.7 V to 3.6 V				
		Maximum ² Maximum ³				
Symbol	Parameter	Typical 1	Std Temp	Ext Temp	Units	Conditions
I _{DD} Stop	Supply Current in STOP Mode	0.1			μA	No peripherals enabled. All pins driven to V_{DD} or $V_{SS}.$
I _{DD} Halt	Supply Current in HALT Mode (with all peripherals disabled)	35	55	65	μA	32 kHz
		520			μA	5.5 MHz
		2.1	2.85	2.85	mA	20 MHz
I _{DD}	Supply Current in	2.8			mA	32 kHz
	ACTIVE Mode (with all peripherals disabled)	4.5	5.2	5.2	mA	5.5 MHz
		5.5	6.5	6.5	mA	10 MHz
	-	7.9	11.5	11.5	mA	20 MHz
I _{DD} WDT	Watchdog Timer Supply Current	0.9	1.0	1.1	μA	
I _{DD}	Crystal Oscillator Supply Current	40			μA	32 kHz
XTAL		230			μA	4 MHz
		760			μA	20 MHz
I _{DD} IPO	Internal Precision Oscillator Supply Current	350	500	550	μA	
I _{DD} VBO	Voltage Brownout and Low-Voltage Detect Supply Current	50			μA	For 20-/28-pin devices (VBO only); See Notes 4
						For 8-pin devices; See Notes 4
I _{DD} ADC	Analog to Digital Converter Supply Current (with External Reference)	2.8	3.1	3.2	mA	32 kHz
		3.1	3.6	3.7	mA	5.5 MHz
		3.3	3.7	3.8	mA	10 MHz
		3.7	4.2	4.3	mA	20 MHz
I _{DD} ADCRef	ADC Internal Reference Supply Current	0			μA	See Notes 4
I _{DD} CMP	Comparator supply Current	150	180	190	μA	See Notes 4

Table 128. Power Consumption

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Figure 33 displays the typical current consumption while operating with all peripherals disabled, at 30 °C, versus the system clock frequency.



Figure 33. Typical Active Mode I_{DD} Versus System Clock Frequency