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Zilog - Z8F022AHJ020SC00TR Datasheet



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Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	23
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f022ahj020sc00tr

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Address Space

The eZ8 CPU can access the following three distinct address spaces:

- 1. The Register File contains addresses for the general-purpose registers and the eZ8 CPU, peripheral, and general-purpose I/O port control registers.
- 2. The Program Memory contains addresses for all memory locations having executable code and/or data.
- 3. The Data Memory contains addresses for all memory locations that contain data only.

These three address spaces are covered briefly in the following subsections. For more information on eZ8 CPU and its address space, refer to eZ8 CPU Core User Manual (UM0128) available for download at www.zilog.com.

Register File

The Register File address space in the Z8 Encore![®] MCU is 4 KB (4096 bytes). The Register File is composed of two sections: control registers and general-purpose registers. When instructions are executed, registers defined as sources are read, and registers defined as destinations are written. The architecture of the eZ8 CPU allows all general-purpose registers to function as accumulators, address pointers, index registers, stack areas, or scratch pad memory.

The upper 256 bytes of the 4 KB Register File address space are reserved for control of the eZ8 CPU, the on-chip peripherals, and the I/O ports. These registers are located at addresses from F00H to FFFH. Some of the addresses within the 256 B control register section are reserved (unavailable). Reading from a reserved Register File address returns an undefined value. Writing to reserved Register File addresses is not recommended and can produce unpredictable results.

The on-chip RAM always begins at address 000H in the Register File address space. The Z8 Encore! XP[®] F082A Series devices contain 256 B to 1 KB of on-chip RAM. Reading from Register File addresses outside the available RAM addresses (and not within the control register address space) returns an undefined value. Writing to these Register File addresses produces no effect.

Program Memory

The eZ8 CPU supports 64 KB of Program Memory address space. The Z8 Encore! XP F082A Series devices contain 1 KB to 8 KB of on-chip Flash memory in the Program Memory address space, depending on the device. Reading from Program Memory

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Program Memory Address (Hex)	Function
Z8F022A and Z8F021A Products	
0000–0001	Flash Option Bits
0002–0003	Reset Vector
0004–0005	WDT Interrupt Vector
0006–0007	Illegal Instruction Trap
0008–0037	Interrupt Vectors*
0038–0039	Reserved
003A-003D	Oscillator Fail Trap Vectors
003E-07FF	Program Memory
Z8F012A and Z8F011A Products	
0000–0001	Flash Option Bits
0002–0003	Reset Vector
0004–0005	WDT Interrupt Vector
0006–0007	Illegal Instruction Trap
0008–0037	Interrupt Vectors*
0038–0039	Reserved
003A-003D	Oscillator Fail Trap Vectors
003E-03FF	Program Memory
* See Table 32 on page 56 for a list of the in	nterrupt vectors.

Table 5. Z8 Encore! XP F082A Series Program Memory Maps (Continued)

Data Memory

The Z8 Encore! XP F082A Series does not use the eZ8 CPU's 64 KB Data Memory address space.

Flash Information Area

Table 6 on page 18 describes the Z8 Encore! XP F082A Series Flash Information Area. This 128 B Information Area is accessed by setting bit 7 of the Flash Page Select Register to 1. When access is enabled, the Flash Information Area is mapped into the Program Memory and overlays the 128 bytes at addresses FE00H to FF7FH. When the Information Area access is enabled, all reads from these Program Memory addresses return the Infor-



Table 46. Shared Interrupt Select Register (IRQSS)

BITS	7	6	5	4	3	2	1	0
FIELD	PA7VS	PA6CS			Rese	erved		
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR				FC	EH			

PA7VS—PA7/LVD Selection

0 = PA7 is used for the interrupt for PA7VS interrupt request.

1 = The LVD is used for the interrupt for PA7VS interrupt request.

PA6CS—PA6/Comparator Selection

0 = PA6 is used for the interrupt for PA6CS interrupt request.

1 = The Comparator is used for the interrupt for PA6CS interrupt request.

Reserved—Must be 0.

Interrupt Control Register

The Interrupt Control (IRQCTL) register (Table 47) contains the master enable bit for all interrupts.

Table 47. Interrupt	Control	Register	(IRQCTL)
---------------------	---------	----------	----------

BITS	7	6	5	4	3	2	1	0
FIELD	IRQE				Reserved			
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R	R	R	R	R	R	R
ADDR				FC	FH			

IRQE—Interrupt Request Enable

This bit is set to 1 by executing an EI (Enable Interrupts) or IRET (Interrupt Return) instruction, or by a direct register write of a 1 to this bit. It is reset to 0 by executing a DI instruction, eZ8 CPU acknowledgement of an interrupt request, Reset or by a direct register write of a 0 to this bit.

- 0 = Interrupts are disabled.
- 1 = Interrupts are enabled.

Reserved—Must be 0.



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BITS	7	6	5	4	3	2	1	0
FIELD				PW	/ML			
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR				F05H,	F0DH			

Table 55. Timer 0–1 PWM Low Byte Register (TxPWML)

PWMH and PWML—Pulse-Width Modulator High and Low Bytes These two bytes, {PWMH[7:0], PWML[7:0]}, form a 16-bit value that is compared to the current 16-bit timer count. When a match occurs, the PWM output changes state. The PWM output value is set by the TPOL bit in the Timer Control Register (TxCTL1) register.

The TxPWMH and TxPWML registers also store the 16-bit captured timer value when operating in CAPTURE or CAPTURE/COMPARE modes.

















Operation

Data Format

The UART always transmits and receives data in an 8-bit data format, least-significant bit first. An even or odd parity bit can be added to the data stream. Each character begins with an active Low START bit and ends with either 1 or 2 active High STOP bits. Figure 11 and Figure 12 display the asynchronous data format employed by the UART without parity and with parity, respectively.



Receiving Data using the Interrupt-Driven Method

The UART Receiver interrupt indicates the availability of new data (as well as error conditions). Follow the steps below to configure the UART receiver for interrupt-driven operation:

- 1. Write to the UART Baud Rate High and Low Byte registers to set the acceptable baud rate.
- 2. Enable the UART pin functions by configuring the associated GPIO Port pins for alternate function operation.
- 3. Execute a DI instruction to disable interrupts.
- 4. Write to the Interrupt control registers to enable the UART Receiver interrupt and set the acceptable priority.
- 5. Clear the UART Receiver interrupt in the applicable Interrupt Request register.
- 6. Write to the UART Control 1 Register to enable Multiprocessor (9-bit) mode functions, if appropriate.
 - Set the Multiprocessor Mode Select (MPEN) to Enable MULTIPROCESSOR mode.
 - Set the Multiprocessor Mode Bits, MPMD[1:0], to select the acceptable address matching scheme.
 - Configure the UART to interrupt on received data and errors or errors only (interrupt on errors only is unlikely to be useful for Z8 Encore![®] devices without a DMA block)
- 7. Write the device address to the Address Compare Register (automatic MULTIPRO-CESSOR modes only).
- 8. Write to the UART Control 0 register to:
 - Set the receive enable bit (REN) to enable the UART for data reception
 - Enable parity, if appropriate and if multiprocessor mode is not enabled, and select either even or odd parity.
- 9. Execute an EI instruction to enable interrupts.

The UART is now configured for interrupt-driven data reception. When the UART Receiver interrupt is detected, the associated interrupt service routine (ISR) performs the following:

- 1. Checks the UART Status 0 register to determine the source of the interrupt error, break, or received data.
- 2. Reads the data from the UART Receive Data register if the interrupt was because of data available. If operating in MULTIPROCESSOR (9-bit) mode, further actions may be required depending on the MULTIPROCESSOR mode bits MPMD[1:0].



Figure 15. UART Receiver Interrupt Service Routine Flow

Baud Rate Generator Interrupts

If the baud rate generator (BRG) interrupt enable is set, the UART Receiver interrupt asserts when the UART Baud Rate Generator reloads. This condition allows the Baud Rate Generator to function as an additional counter if the UART functionality is not employed.

UART Baud Rate Generator

The UART Baud Rate Generator creates a lower frequency baud rate clock for data transmission. The input to the Baud Rate Generator is the system clock. The UART Baud Rate High and Low Byte registers combine to create a 16-bit baud rate divisor value

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#5 MSB #5 LSB

6. Add the gain correction factor to the original offset corrected value.

	#5 MSB	#5 LSB
+		
	#1 MSB	#1 LSB
=		

#6 MSB	#6 LSB
--------	--------

7. Shift the result to the right, using the sign bit determined in Step 1. This allows for the detection of computational overflow.

|--|

Output Data

The following is the output format of the corrected ADC value.

MSB	LSB
s v b a 9 8 7 6	5 4 3 2 1 0

The overflow bit in the corrected output indicates that the computed value was greater than the maximum logical value (+1023) or less than the minimum logical value (-1024). Unlike the hardware overflow bit, this is not a simple binary Flag. For a normal sample (non-overflow), the sign and the overflow bit matches. If the sign bit and overflow bit do not match, a computational overflow has occurred.

Input Buffer Stage

Many applications require the measurement of an input voltage source with a high output impedance. This ADC provides a buffered input for such situations. The drawback of the buffered input is a limitation of the input range. When using unity gain buffered mode, the input signal must be prevented from coming too close to either V_{SS} or V_{DD} . See Table 135 on page 231 for details.

This condition applies only to the input voltage level (with respect to ground) of each differential input signal. The actual differential input voltage magnitude may be less than 300 mV.

The input range of the unbuffered ADC swings from V_{SS} to V_{DD} . Input signals smaller than 300 mV must use the unbuffered input mode. If these signals do not contain low output impedances, they might require off-chip buffering.

Signals outside the allowable input range can be used without instability or device damage. Any ADC readings made outside the input range are subject to greater inaccuracy than specified.





Figure 22. Flash Controller Operation Flow Chart

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the OCD or via the Flash Controller Bypass mode are unaffected. After a bit of the Sector Protect Register has been set, it cannot be cleared except by powering down the device.

Byte Programming

The Flash Memory is enabled for byte programming after unlocking the Flash Controller and successfully enabling either Mass Erase or Page Erase. When the Flash Controller is unlocked and Mass Erase is successfully completed, all Program Memory locations are available for byte programming. In contrast, when the Flash Controller is unlocked and Page Erase is successfully completed, only the locations of the selected page are available for byte programming. An erased Flash byte contains all 1's (FFH). The programming operation can only be used to change bits from 1 to 0. To change a Flash bit (or multiple bits) from 0 to 1 requires execution of either the Page Erase or Mass Erase commands.

Byte Programming can be accomplished using the On-Chip Debugger's Write Memory command or eZ8 CPU execution of the LDC or LDCI instructions. Refer to the *eZ8 CPU User Manual* (available for download at <u>www.zilog.com</u>) for a description of the LDC and LDCI instructions. While the Flash Controller programs the Flash memory, the eZ8 CPU idles but the system clock and on-chip peripherals continue to operate. To exit programming mode and lock the Flash, write any value to the Flash Control register, except the Mass Erase or Page Erase commands.



Caution: The byte at each address of the Flash memory cannot be programmed (any bits written to 0) more than twice before an erase cycle occurs. Doing so may result in corrupted data at the target byte.

Page Erase

The Flash memory can be erased one page (512 bytes) at a time. Page Erasing the Flash memory sets all bytes in that page to the value FFH. The Flash Page Select register identifies the page to be erased. Only a page residing in an unprotected sector can be erased. With the Flash Controller unlocked and the active page set, writing the value 95h to the Flash Control register initiates the Page Erase operation. While the Flash Controller executes the Page Erase operation, the eZ8 CPU idles but the system clock and on-chip peripherals continue to operate. The eZ8 CPU resumes operation after the Page Erase operation completes. If the Page Erase operation is performed using the On-Chip Debugger, poll the Flash Status register to determine when the Page Erase operation is complete. When the Page Erase is complete, the Flash Controller returns to its locked state.

Mass Erase

The Flash memory can also be Mass Erased using the Flash Controller, but only by using the On-Chip Debugger. Mass Erasing the Flash memory sets all bytes to the value FFH. With the Flash Controller unlocked and the Mass Erase successfully enabled, writing the

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Info Page Address	Memory Address	Compensation Usage	ADC Mode	Reference Type
34	FE34	Negative Gain High Byte	Differential Unbuffered	External 2.0 V
35	FE35	Negative Gain Low Byte	Differential Unbuffered	External 2.0 V
78	FE78	Offset	Differential 1x Buffered	Internal 2.0 V
18	FE18	Positive Gain High Byte	Differential 1x Buffered	Internal 2.0 V
19	FE19	Positive Gain Low Byte	Differential 1x Buffered	Internal 2.0 V
36	FE36	Negative Gain High Byte	Differential 1x Buffered	Internal 2.0 V
37	FE37	Negative Gain Low Byte	Differential 1x Buffered	Internal 2.0 V
7B	FE7B	Offset	Differential 1x Buffered	External 2.0 V
1A	FE1A	Positive Gain High Byte	Differential 1x Buffered	External 2.0 V
1B	FE1B	Positive Gain Low Byte	Differential 1x Buffered	External 2.0 V
38	FE38	Negative Gain High Byte	Differential 1x Buffered	External 2.0 V
39	FE39	Negative Gain Low Byte	Differential 1x Buffered	External 2.0 V

Table 94. ADC Calibration Data Location (Continued)

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WDTCALH—Watchdog Timer Calibration High Byte The WDTCALH and WDTCALL bytes, when loaded into the Watchdog Timer reload registers result in a one second timeout at room temperature and 3.3 V supply voltage. To use the Watchdog Timer calibration, user code must load WDTU with 0x00, WDTH with WDTCALH and WDTL with WDTCALL.

Table 98. Watchdog Calibration Low Byte at 007FH (WDTCALL)

BITS	7	6	5	4	3	2	1	0	
FIELD	WDTCALL								
RESET	U	U	U	U	U	U	U		
R/W	R/W	R/W	R/W	R/W	R/W				
ADDR	Information Page Memory 007FH								
Note: U =	Unchanged b	v Reset. R/W	= Read/Write	e.					

WDTCALL—Watchdog Timer Calibration Low Byte

The WDTCALH and WDTCALL bytes, when loaded into the Watchdog Timer reload registers result in a one second timeout at room temperature and 3.3 V supply voltage. To use the Watchdog Timer calibration, user code must load WDTU with 0x00, WDTH with WDTCALH and WDTL with WDTCALL.

Serialization Data

Table 99. Serial Number at 001C - 001F (S_NUM)

BITS	7	6	5	4	3	2	1	0	
FIELD	S_NUM								
RESET	U	U	U	U	U	U	U		
R/W	R/W R/W R/W R/W R/W R/W							R/W	
ADDR	Information Page Memory 001C-001F								
Note: U =	Unchanged b	y Reset. R/W	= Read/Write).					

S NUM—Serial Number Byte

The serial number is a unique four-byte binary value.

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Debug Command	Command Byte	Enabled when NOT in DEBUG mode?	Disabled by Flash Read Protect Option Bit
Write Register	08H	_	Only writes of the Flash Memory Control registers are allowed. Additionally, only the Mass Erase command is allowed to be written to the Flash Control register.
Read Register	09H	_	Disabled
Write Program Memory	0AH	_	Disabled
Read Program Memory	0BH	_	Disabled
Write Data Memory	0CH	_	Yes
Read Data Memory	0DH	_	-
Read Program Memory CRC	0EH	_	-
Reserved	0FH	_	-
Step Instruction	10H	_	Disabled
Stuff Instruction	11H	_	Disabled
Execute Instruction	12H	_	Disabled
Reserved	13H–FFH	_	_

In the following bulleted list of OCD Commands, data and commands sent from the host to the On-Chip Debugger are identified by 'DBG \leftarrow Command/Data'. Data sent from the On-Chip Debugger back to the host is identified by 'DBG \rightarrow Data'

• **Read OCD Revision (00H)**—The Read OCD Revision command determines the version of the On-Chip Debugger. If OCD commands are added, removed, or changed, this revision number changes.

```
DBG \leftarrow 00H
DBG \rightarrow OCDRev[15:8] (Major revision number)
DBG \rightarrow OCDRev[7:0] (Minor revision number)
```

• **Read OCD Status Register (02H)**—The Read OCD Status Register command reads the OCDSTAT register.

```
DBG \leftarrow 02H
DBG \rightarrow OCDSTAT[7:0]
```

• **Read Runtime Counter (03H)**—The Runtime Counter counts system clock cycles in between Breakpoints. The 16-bit Runtime Counter counts up from 0000H and stops at the maximum count of FFFFH. The Runtime Counter is overwritten during the



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Assembly Language Syntax

For proper instruction execution, eZ8 CPU assembly language syntax requires that the operands be written as 'destination, source'. After assembly, the object code usually has the operands in the order 'source, destination', but ordering is opcode-dependent. The following instruction examples illustrate the format of some basic assembly instructions and the resulting object code produced by the assembler. This binary format must be followed if manual program coding is preferred or if you intend to implement your own assembler.

Example 1: If the contents of Registers 43H and 08H are added and the result is stored in 43H, the assembly syntax and resulting object code is:

Table 112. Assembly Language Syntax Example 1

Assembly Language Code	ADD	43H,	08H	(ADD dst, src)
Object Code	04	08	43	(OPC src, dst)

Example 2: In general, when an instruction format requires an 8-bit register address, that address can specify any register location in the range 0–255 or, using Escaped Mode Addressing, a Working Register R0–R15. If the contents of Register 43H and Working Register R8 are added and the result is stored in 43H, the assembly syntax and resulting object code is:

Table 113. Assembly Language Syntax Example 2

Assembly Language Code	ADD	43H,	R8	(ADD dst, src)
Object Code	04	E8	43	(OPC src, dst)

See the device-specific Product Specification to determine the exact register file range available. The register file size varies, depending on the device type.

eZ8 CPU Instruction Notation

In the eZ8 CPU Instruction Summary and Description sections, the operands, condition codes, status flags, and address modes are represented by a notational shorthand that is described in Table 114.

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Table 126. Absolute Maximum Ratings (Continued)

Parameter	Minimum Maximun	n Units	Notes
28-pin Packages Maximum Ratings at 0 °C to 70 °C			
Total power dissipation	450	mW	
Maximum current into V_{DD} or out of V_{SS}	125	mA	

Operating temperature is specified in DC Characteristics.

This voltage applies to all pins except the following: V_{DD}, AV_{DD}, pins supporting analog input (Port B[5:0], Port C[2:0]) and pins supporting the crystal oscillator (PA0 and PA1). On the 8-pin packages, this applies to all pins but V_{DD}.

2. This voltage applies to pins on the 20-/28-pin packages supporting analog input (Port B[5:0], Port C[2:0]) and pins supporting the crystal oscillator (PA0 and PA1).

DC Characteristics

Table 127 lists the DC characteristics of the Z8 Encore! $XP^{\mathbb{R}}$ F082A Series products. All voltages are referenced to V_{SS} , the primary system ground.

Table 127. DC Characteristics	
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		T _A = -40 °C to +105 °C (unless otherwise specified)						
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions		
V _{DD}	Supply Voltage	2.7	_	3.6	V			
V _{IL1}	Low Level Input Voltage	-0.3	-	0.3*V _{DD}	V			
V _{IH1}	High Level Input Voltage	0.7*V _{DD}	_	5.5	V	For all input pins without analog or oscillator function. For all signal pins on the 8-pin devices. Programmable pull-ups must also be disabled.		
V _{IH2}	High Level Input Voltage	0.7*V _{DD}	_	V _{DD} +0.3	V	For those pins with analog or oscillator function (20-/28-pin devices only), or when programmable pull-ups are enabled.		
V _{OL1}	Low Level Output Voltage	-	-	0.4	V	I _{OL} = 2 mA; V _{DD} = 3.0 V High Output Drive disabled.		
V _{OH1}	High Level Output Voltage	2.4	-	-	V	I _{OH} = -2 mA; V _{DD} = 3.0 V High Output Drive disabled.		

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		V _{DD} T _A = (unless	= 3.0 V to 0 °C to + otherwis	3.6 V 70 °C e stated)				
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions		
	Single-Shot Conversion Time	-	5129	_	System clock cycles	All measurements but temperature sensor		
			10258			Temperature sensor measurement		
	Continuous Conversion Time	-	256	_	System clock cycles	All measurements but temperature sensor		
			512			Temperature sensor measurement		
	Signal Input Bandwidth	-	10		kHz	As defined by -3 dB point		
R _S	Analog Source Impedance ⁴	-	-	10	kΩ	In unbuffered mode		
				500	kΩ	In buffered modes		
Zin	Input Impedance	-	150		kΩ	In unbuffered mode at 20 $\rm MHz^5$		
		10	_		MΩ	In buffered modes		
Vin	Input Voltage Range	0		V _{DD}	V	Unbuffered Mode		
		0.3		V _{DD} -1.1	V	Buffered Modes		
					Note:	These values define the range over which the ADC performs within spec; exceeding these values does not cause damage or instability; see DC Characteristics on page 222 for absolute pin voltage limits		

Table 135. Analog-to-Digital Converter Electrical Characteristics and Timing (Continued)

Notes

- 1. Analog source impedance affects the ADC offset voltage (because of pin leakage) and input settling time.
- 2. Devices are factory calibrated at V_{DD} = 3.3 V and T_A = +30 °C, so the ADC is maximally accurate under these conditions.
- 3. LSBs are defined assuming 10-bit resolution.
- 4. This is the maximum recommended resistance seen by the ADC input pin.
- 5. The input impedance is inversely proportional to the system clock frequency.



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Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP [®] F082A	Serie	s with 1	KB Fla	sh							
Standard Temperature	: 0 °C	to 70 °C									
Z8F011APB020SC	1 KB	256 B	16 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F011AQB020SC	1 KB	256 B	16 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F011ASB020SC	1 KB	256 B	16 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F011ASH020SC	1 KB	256 B	16 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F011AHH020SC	1 KB	256 B	16 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F011APH020SC	1 KB	256 B	16 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F011ASJ020SC	1 KB	256 B	16 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F011AHJ020SC	1 KB	256 B	16 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F011APJ020SC	1 KB	256 B	16 B	25	19	2	0	1	1	0	PDIP 28-pin package
Extended Temperature	∋: -40 °	°C to 105	5 °C								
Z8F011APB020EC	1 KB	256 B	16 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F011AQB020EC	1 KB	256 B	16 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F011ASB020EC	1 KB	256 B	16 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F011ASH020EC	1 KB	256 B	16 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F011AHH020EC	1 KB	256 B	16 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F011APH020EC	1 KB	256 B	16 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F011ASJ020EC	1 KB	256 B	16 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F011AHJ020EC	1 KB	256 B	16 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F011APJ020EC	1 KB	256 B	16 B	25	19	2	0	1	1	0	PDIP 28-pin package
Replace C with G for Lead	I-Free F	ackaging									