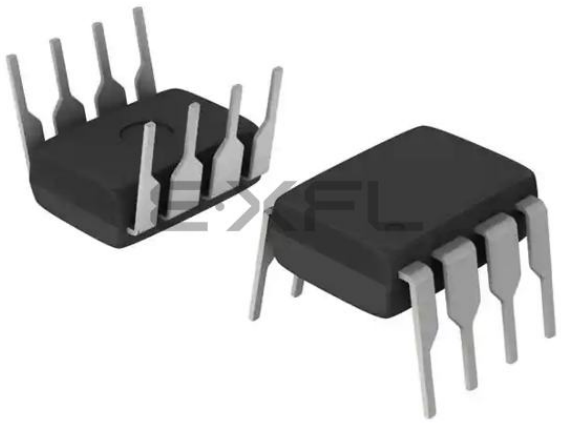

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	6
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f022apb020ec

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- On-Chip Debugger (OCD)
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- 2.7 V to 3.6 V operating voltage
- 8-, 20-, and 28-pin packages
- 0 °C to +70 °C and -40 °C to +105 °C for operating temperature ranges

Part Selection Guide

Table 1 on page 3 identifies the basic features and package styles available for each device within the Z8 Encore! XP® F082A Series product line.

Table 32. Trap and Interrupt Vectors in Order of Priority (Continued)

Priority	Program Memory Vector Address	Interrupt or Trap Source
	0034H	Port C Pin 1, both input edges
Lowest	0036H	Port C Pin 0, both input edges
	0038H	Reserved

Architecture

Figure 8 displays the interrupt controller block diagram.

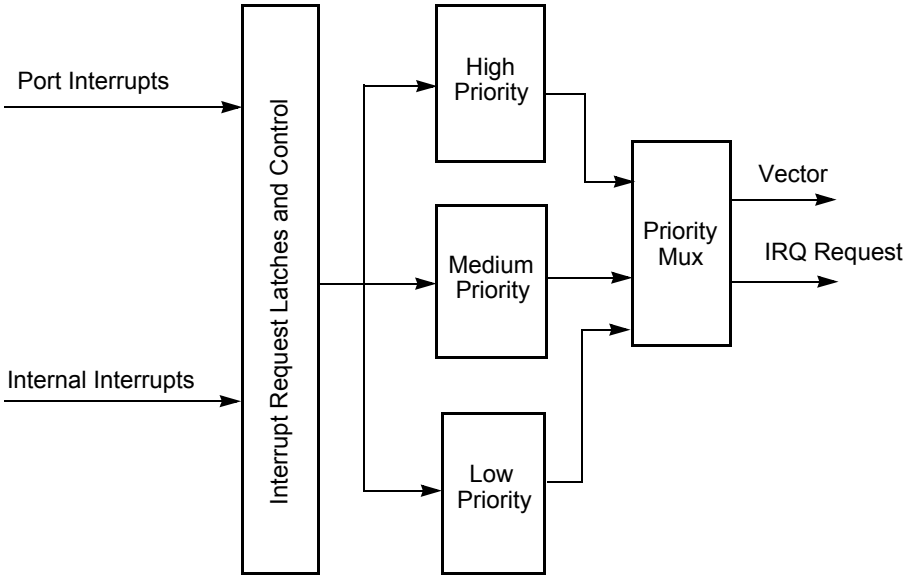

Figure 8. Interrupt Controller Block Diagram

Operation

Master Interrupt Enable

The master interrupt enable bit (IRQE) in the Interrupt Control register globally enables and disables interrupts.

Follow the steps below for configuring a timer for CAPTURE mode and initiating the count:

1. Write to the Timer Control register to:
   - Disable the timer.
   - Configure the timer for CAPTURE mode.
   - Set the prescale value.
   - Set the Capture edge (rising or falling) for the Timer Input.
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
4. Clear the Timer PWM High and Low Byte registers to 0000H. Clearing these registers allows the software to determine if interrupts were generated by either a capture event or a reload. If the PWM High and Low Byte registers still contain 0000H after the interrupt, the interrupt was generated by a Reload.
5. Enable the timer interrupt, if appropriate, and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input capture and reload events. If appropriate, configure the timer interrupt to be generated only at the input capture event or the reload event by setting TICONFIG field of the TxCTL0 register.
6. Configure the associated GPIO port pin for the Timer Input alternate function.
7. Write to the Timer Control register to enable the timer and initiate counting.

In CAPTURE mode, the elapsed time from timer start to Capture event can be calculated using the following equation:

$$\text{Capture Elapsed Time (s)} = \frac{(\text{Capture Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

CAPTURE RESTART Mode

In CAPTURE RESTART mode, the current timer count value is recorded when the acceptable external Timer Input transition occurs. The Capture count value is written to the Timer PWM High and Low Byte Registers. The timer input is the system clock. The TPOL bit in the Timer Control register determines if the Capture occurs on a rising edge or a falling edge of the Timer Input signal. When the Capture event occurs, an interrupt is generated and the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. The INPCAP bit in TxCTL0 register is set to indicate the timer interrupt is because of an input capture event.

If no Capture event occurs, the timer counts up to the 16-bit Compare value stored in the Timer Reload High and Low Byte registers. Upon reaching the Reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to

CAPTURE RESTART mode
0 = Count is captured on the rising edge of the Timer Input signal.
1 = Count is captured on the falling edge of the Timer Input signal.

COMPARATOR COUNTER mode
When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload. Also:

0 = Count is captured on the rising edge of the comparator output.
1 = Count is captured on the falling edge of the comparator output.

Caution: *When the Timer Output alternate function TxOUT on a GPIO port pin is enabled, TxOUT changes to whatever state the TPOL bit is in.The timer does not need to be enabled for that to happen. Also, the Port data direction sub register is not needed to be set to output on TxOUT. Changing the TPOL bit with the timer enabled and running does not immediately change the TxOUT.*

PRES—Prescale value
The timer input clock is divided by 2^{PRES}, where PRES can be set from 0 to 7. The prescaler is reset each time the Timer is disabled. This reset ensures proper clock division each time the Timer is restarted.

000 = Divide by 1
001 = Divide by 2
010 = Divide by 4
011 = Divide by 8
100 = Divide by 16
101 = Divide by 32
110 = Divide by 64
111 = Divide by 128

TMODE—Timer mode
This field along with the TMODEHI bit in TxCTL0 register determines the operating mode of the timer. TMODEHI is the most significant bit of the Timer mode selection value. The entire operating mode bits are expressed as {TMODEHI, TMODE[2:0]}. The TMODEHI is bit 7 of the TxCTL0 register while TMODE[2:0] is the lower 3 bits of the TxCTL1 register.

0000 = ONE-SHOT mode
0001 = CONTINUOUS mode
0010 = COUNTER mode
0011 = PWM SINGLE OUTPUT mode
0100 = CAPTURE mode
0101 = COMPARE mode
0110 = GATED mode
0111 = CAPTURE/COMPARE mode

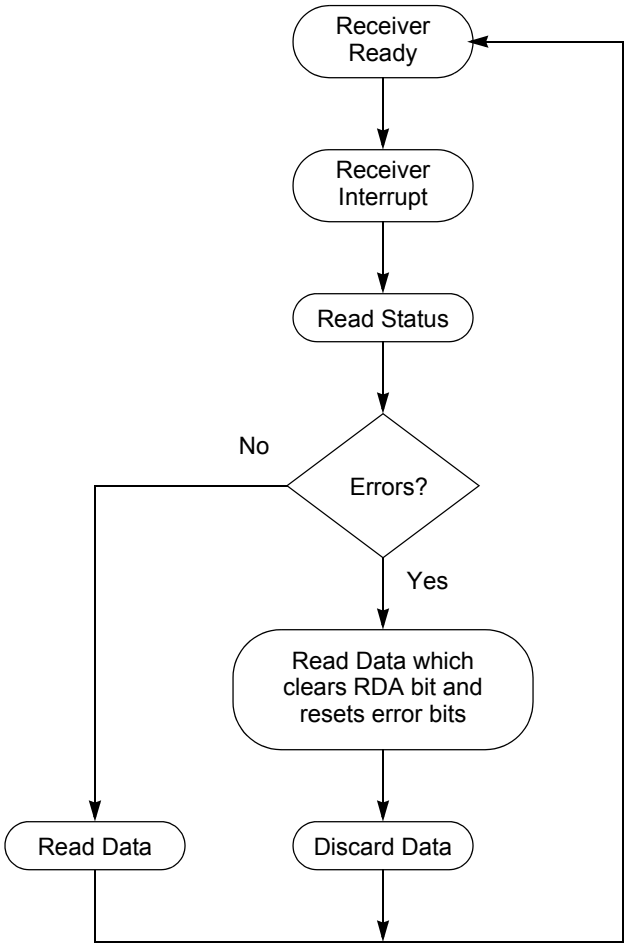

Figure 15. UART Receiver Interrupt Service Routine Flow

Baud Rate Generator Interrupts

If the baud rate generator (BRG) interrupt enable is set, the UART Receiver interrupt asserts when the UART Baud Rate Generator reloads. This condition allows the Baud Rate Generator to function as an additional counter if the UART functionality is not employed.

UART Baud Rate Generator

The UART Baud Rate Generator creates a lower frequency baud rate clock for data transmission. The input to the Baud Rate Generator is the system clock. The UART Baud Rate High and Low Byte registers combine to create a 16-bit baud rate divisor value

3. Write to the ADC Control Register 0 to configure the ADC for continuous conversion. The bit fields in the ADC Control register may be written simultaneously:
   - Write to the ANAIN[3:0] field to select from the available analog input sources (different input pins available depending on the device).
   - Set CONT to 1 to select continuous conversion.
   - If the internal VREF must be output to a pin, set the REFEXT bit to 1. The internal voltage reference must be enabled in this case.
   - Write the REFSELL bit of the pair {REFSELH, REFSELL} to select the internal voltage reference level or to disable the internal reference. The REFSELH bit is contained in ADC Control/Status Register 1.
   - Set CEN to 1 to start the conversions.
4. When the first conversion in continuous operation is complete (after 5129 system clock cycles, plus the 40 cycles for power-up, if necessary), the ADC control logic performs the following operations:
   - CEN resets to 0 to indicate the first conversion is complete. CEN remains 0 for all subsequent conversions in continuous operation.
   - An interrupt request is sent to the Interrupt Controller to indicate the conversion is complete.
5. The ADC writes a new data result every 256 system clock cycles. For each completed conversion, the ADC control logic performs the following operations:
   - Writes the 13-bit two's complement result to {ADCD_H[7:0], ADCD_L[7:3]}.
   - Sends an interrupt request to the Interrupt Controller denoting conversion complete.
6. To disable continuous conversion, clear the CONT bit in the ADC Control Register to 0.

Interrupts

The ADC is able to interrupt the CPU when a conversion has been completed. When the ADC is disabled, no new interrupts are asserted; however, an interrupt pending when the ADC is disabled is not cleared.

Calibration and Compensation

The Z8 Encore! XP® F082A Series ADC is factory calibrated for offset error and gain error, with the compensation data stored in Flash memory. Alternatively, you can perform your own calibration, storing the values into Flash themselves. Thirdly, the user code can perform a manual offset calibration during DIFFERENTIAL mode operation.

#5 MSB	#5 LSB

6. Add the gain correction factor to the original offset corrected value.

#5 MSB	#5 LSB

+

#1 MSB	#1 LSB

=

#6 MSB	#6 LSB

7. Shift the result to the right, using the sign bit determined in Step 1. This allows for the detection of computational overflow.

S->	#6 MSB	#6 LSB

Output Data

The following is the output format of the corrected ADC value.

MSB	LSB
s v b a 9 8 7 6	5 4 3 2 1 0 - -

The overflow bit in the corrected output indicates that the computed value was greater than the maximum logical value (+1023) or less than the minimum logical value (-1024). Unlike the hardware overflow bit, this is not a simple binary Flag. For a normal sample (non-overflow), the sign and the overflow bit matches. If the sign bit and overflow bit do not match, a computational overflow has occurred.

Input Buffer Stage

Many applications require the measurement of an input voltage source with a high output impedance. This ADC provides a buffered input for such situations. The drawback of the buffered input is a limitation of the input range. When using unity gain buffered mode, the input signal must be prevented from coming too close to either V_{SS} or V_{DD}. See Table 135 on page 231 for details.

This condition applies only to the input voltage level (with respect to ground) of each differential input signal. The actual differential input voltage magnitude may be less than 300 mV.

The input range of the unbuffered ADC swings from V_{SS} to V_{DD}. Input signals smaller than 300 mV must use the unbuffered input mode. If these signals do not contain low output impedances, they might require off-chip buffering.

Signals outside the allowable input range can be used without instability or device damage. Any ADC readings made outside the input range are subject to greater inaccuracy than specified.

Low Power Operational Amplifier

Overview

The LPO is a general-purpose low power operational amplifier. Each of the three ports of the amplifier is accessible from the package pins. The LPO contains only one pin configuration: ANA0 is the output/feedback node, ANA1 is the inverting input and ANA2 is the non-inverting input.

Operation

To use the LPO, it must be enabled in the Power Control Register 0 (PWRCTL0). The default state of the LPO is OFF. To use the LPO, the LPO bit must be cleared, turning it ON (Power Control Register 0 (PWRCTL0) on page 35). When making normal ADC measurements on ANA0 (measurements not involving the LPO output), the LPO bit must be OFF. Turning the LPO bit ON interferes with normal ADC measurements.

Warning: *The LPO bit enables the amplifier even in STOP mode. If the amplifier is not required in STOP mode, disable it. Failing to perform this results in STOP mode currents higher than necessary.*

As with other ADC measurements, any pins used for analog purposes must be configured as such in the GPIO registers (see Port A–D Alternate Function Sub-Registers on page 47).

LPO output measurements are made on ANA0, as selected by the ANAIN[3:0] bits of ADC Control Register 0. It is also possible to make single-ended measurements on ANA1 and ANA2 while the amplifier is enabled, which is often useful for determining offset conditions. Differential measurements between ANA0 and ANA2 may be useful for noise cancellation purposes.

If the LPO output is routed to the ADC, then the BUFFMODE[2:0] bits of ADC Control/Status Register 1 must also be configured for unity-gain buffered operation. Sampling the LPO in an unbuffered mode is not recommended.

When either input is overdriven, the amplifier output saturates at the positive or negative supply voltage. No instability results.

Temperature Sensor Calibration Data

Table 95. Temperature Sensor Calibration High Byte at 003A (TSCALH)

BITS	7	6	5	4	3	2	1	0
FIELD	TSCALH							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	Information Page Memory 003A							

Note: U = Unchanged by Reset. R/W = Read/Write.

TSCALH – Temperature Sensor Calibration High Byte

The TSCALH and TSCALL bytes combine to form the 12-bit temperature sensor offset calibration value. For more details, see Temperature Sensor Operation on page 139.

Table 96. Temperature Sensor Calibration Low Byte at 003B (TSCALL)

BITS	7	6	5	4	3	2	1	0
FIELD	TSCALL							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	Information Page Memory 003B							

Note: U = Unchanged by Reset. R/W = Read/Write.

TSCALL – Temperature Sensor Calibration Low Byte

The TSCALH and TSCALL bytes combine to form the 12-bit temperature sensor offset calibration value. For usage details, see Temperature Sensor Operation on page 139.

Watchdog Timer Calibration Data

Table 97. Watchdog Calibration High Byte at 007EH (WDTCALH)

BITS	7	6	5	4	3	2	1	0
FIELD	WDTCALH							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	Information Page Memory 007EH							

Note: U = Unchanged by Reset. R/W = Read/Write.

The Auto-Baud Detector/Generator is clocked by the system clock. The minimum baud rate is the system clock frequency divided by 512. For optimal operation with asynchronous datastreams, the maximum recommended baud rate is the system clock frequency divided by 8. The maximum possible baud rate for asynchronous datastreams is the system clock frequency divided by 4, but this theoretical maximum is possible only for low noise designs with clean signals. Table 105 lists minimum and recommended maximum baud rates for sample crystal frequencies.

Table 105. OCD Baud-Rate Limits

System Clock Frequency (MHz)	Recommended Maximum Baud Rate (Kbps)	Recommended Standard PC Baud Rate (bps)	Minimum Baud Rate (Kbps)
20.0	2500.0	1,843,200	39
1.0	125.0	115,200	1.95
0.032768 (32 kHz)	4.096	2,400	0.064

If the OCD receives a Serial Break (nine or more continuous bits Low) the Auto-Baud Detector/Generator resets. Reconfigure the Auto-Baud Detector/Generator by sending 80H.

OCD Serial Errors

The On-Chip Debugger can detect any of the following error conditions on the DBG pin:

- Serial Break (a minimum of nine continuous bits Low)
- Framing Error (received Stop bit is Low)
- Transmit Collision (OCD and host simultaneous transmission detected by the OCD)

When the OCD detects one of these errors, it aborts any command currently in progress, transmits a four character long Serial Break back to the host, and resets the Auto-Baud Detector/Generator. A Framing Error or Transmit Collision may be caused by the host sending a Serial Break to the OCD. Because of the open-drain nature of the interface, returning a Serial Break break back to the host only extends the length of the Serial Break if the host releases the Serial Break early.

The host transmits a Serial Break on the DBG pin when first connecting to the Z8 Encore! XP F082A Series devices or when recovering from an error. A Serial Break from the host resets the Auto-Baud Generator/Detector but does not reset the OCD Control register. A Serial Break leaves the device in DEBUG mode if that is the current mode. The OCD is held in Reset until the end of the Serial Break when the DBG pin returns

```
DBG ← Size[15:8]
DBG ← Size[7:0]
DBG ← 1-65536 data bytes
```

- **Read Data Memory (0DH)**—The Read Data Memory command reads from Data Memory. This command is equivalent to the LDE and LDEI instructions. Data can be read 1 to 65536 bytes at a time (65536 bytes can be read by setting size to 0). If the device is not in DEBUG mode, this command returns FFH for the data.

```
DBG ← 0DH
DBG ← Data Memory Address[15:8]
DBG ← Data Memory Address[7:0]
DBG ← Size[15:8]
DBG ← Size[7:0]
DBG → 1-65536 data bytes
```

- **Read Program Memory CRC (0EH)**—The Read Program Memory CRC command computes and returns the Cyclic Redundancy Check (CRC) of Program Memory using the 16-bit CRC-CCITT polynomial. If the device is not in DEBUG mode, this command returns FFFFH for the CRC value. Unlike most other OCD Read commands, there is a delay from issuing of the command until the OCD returns the data. The OCD reads the Program Memory, calculates the CRC value, and returns the result. The delay is a function of the Program Memory size and is approximately equal to the system clock period multiplied by the number of bytes in the Program Memory.

```
DBG ← 0EH
DBG → CRC[15:8]
DBG → CRC[7:0]
```

- **Step Instruction (10H)**—The Step Instruction command steps one assembly instruction at the current Program Counter (PC) location. If the device is not in DEBUG mode or the Flash Read Protect Option bit is enabled, the OCD ignores this command.

```
DBG ← 10H
```

- **Stuff Instruction (11H)**—The Stuff Instruction command steps one assembly instruction and allows specification of the first byte of the instruction. The remaining 0-4 bytes of the instruction are read from Program Memory. This command is useful for stepping over instructions where the first byte of the instruction has been overwritten by a Breakpoint. If the device is not in DEBUG mode or the Flash Read Protect Option bit is enabled, the OCD ignores this command.

```
DBG ← 11H
DBG ← opcode[7:0]
```

- **Execute Instruction (12H)**—The Execute Instruction command allows sending an entire instruction to be executed to the eZ8 CPU. This command can also step over Breakpoints. The number of bytes to send for the instruction depends on the opcode.

Figure 27 displays a recommended configuration for connection with an external fundamental-mode, parallel-resonant crystal operating at 20 MHz. Recommended 20 MHz crystal specifications are provided in Table 110. Printed circuit board layout must add no more than 4 pF of stray capacitance to either the X_{IN} or X_{OUT} pins. If oscillation does not occur, reduce the values of capacitors C_1 and C_2 to decrease loading.

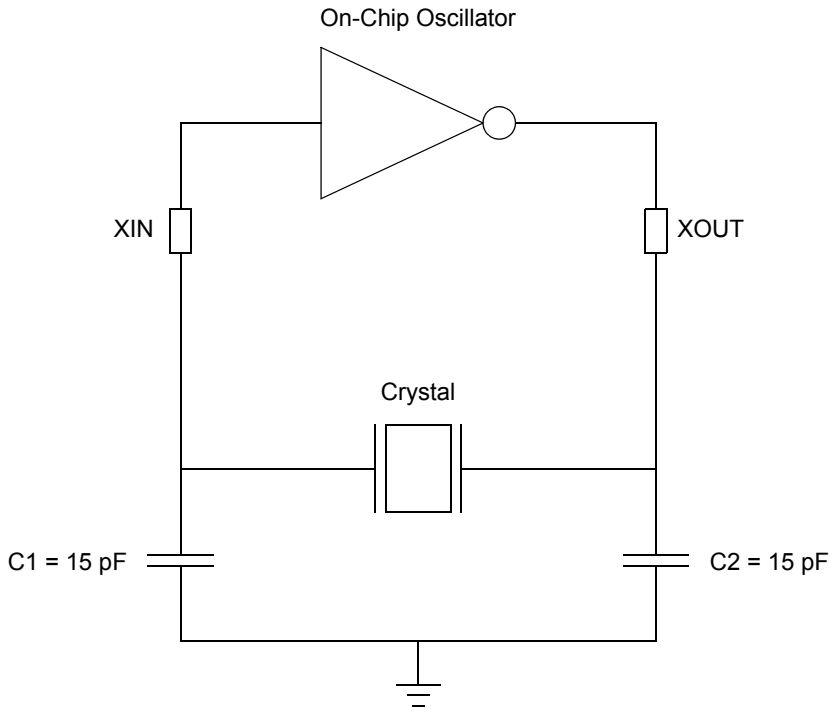

Figure 27. Recommended 20 MHz Crystal Oscillator Configuration

Table 110. Recommended Crystal Oscillator Specifications

Parameter	Value	Units	Comments
Frequency	20	MHz	
Resonance	Parallel		
Mode	Fundamental		
Series Resistance (R_S)	60	Ω	Maximum
Load Capacitance (C_L)	30	pF	Maximum
Shunt Capacitance (C_0)	7	pF	Maximum
Drive Level	1	mW	Maximum

Electrical Characteristics

The data in this chapter is pre-qualification and pre-characterization and is subject to change. Additional electrical characteristics may be found in the individual chapters.

Absolute Maximum Ratings

Stresses greater than those listed in Table 126 may cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, tie unused inputs to one of the supply voltages (V_{DD} or V_{SS}).

Table 126. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	-40	+105	°C	
Storage temperature	-65	+150	°C	
Voltage on any pin with respect to V_{SS}	-0.3	+5.5	V	1
	-0.3	+3.9	V	2
Voltage on V_{DD} pin with respect to V_{SS}	-0.3	+3.6	V	
Maximum current on input and/or inactive output pin	-5	+5	µA	
Maximum output current from active output pin	-25	+25	mA	
8-pin Packages Maximum Ratings at 0 °C to 70 °C				
Total power dissipation		220	mW	
Maximum current into V_{DD} or out of V_{SS}		60	mA	
20-pin Packages Maximum Ratings at 0 °C to 70 °C				
Total power dissipation		430	mW	
Maximum current into V_{DD} or out of V_{SS}		120	mA	

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP® F082A Series with 4 KB Flash											
Standard Temperature: 0 °C to 70 °C											
Z8F041APB020SC	4 KB	1 KB	128 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F041AQB020SC	4 KB	1 KB	128 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F041ASB020SC	4 KB	1 KB	128 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F041ASH020SC	4 KB	1 KB	128 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F041AHH020SC	4 KB	1 KB	128 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F041APH020SC	4 KB	1 KB	128 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F041ASJ020SC	4 KB	1 KB	128 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F041AHJ020SC	4 KB	1 KB	128 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F041APJ020SC	4 KB	1 KB	128 B	25	19	2	0	1	1	0	PDIP 28-pin package
Extended Temperature: -40 °C to 105 °C											
Z8F041APB020EC	4 KB	1 KB	128 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F041AQB020EC	4 KB	1 KB	128 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F041ASB020EC	4 KB	1 KB	128 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F041ASH020EC	4 KB	1 KB	128 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F041AHH020EC	4 KB	1 KB	128 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F041APH020EC	4 KB	1 KB	128 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F041ASJ020EC	4 KB	1 KB	128 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F041AHJ020EC	4 KB	1 KB	128 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F041APJ020EC	4 KB	1 KB	128 B	25	19	2	0	1	1	0	PDIP 28-pin package
Replace C with G for Lead-Free Packaging											

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP® F082A Series with 1 KB Flash, 10-Bit Analog-to-Digital Converter											
Standard Temperature: 0 °C to 70 °C											
Z8F012APB020SC	1 KB	256 B	16 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F012AQB020SC	1 KB	256 B	16 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F012ASB020SC	1 KB	256 B	16 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F012ASH020SC	1 KB	256 B	16 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F012AHH020SC	1 KB	256 B	16 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F012APH020SC	1 KB	256 B	16 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F012ASJ020SC	1 KB	256 B	16 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F012AHJ020SC	1 KB	256 B	16 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F012APJ020SC	1 KB	256 B	16 B	23	20	2	8	1	1	1	PDIP 28-pin package
Extended Temperature: -40 °C to 105 °C											
Z8F012APB020EC	1 KB	256 B	16 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F012AQB020EC	1 KB	256 B	16 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F012ASB020EC	1 KB	256 B	16 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F012ASH020EC	1 KB	256 B	16 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F012AHH020EC	1 KB	256 B	16 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F012APH020EC	1 KB	256 B	16 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F012ASJ020EC	1 KB	256 B	16 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F012AHJ020EC	1 KB	256 B	16 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F012APJ020EC	1 KB	256 B	16 B	23	20	2	8	1	1	1	PDIP 28-pin package
Replace C with G for Lead-Free Packaging											

Index

Symbols

Numerics

A

B

C