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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f041ahh020ec">https://www.e-xfl.com/product-detail/zilog/z8f041ahh020ec</a>

**Table 7. Register File Address Map (Continued)**

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
F0B	Timer 1 Reload Low Byte	T1RL	FF	88
F0C	Timer 1 PWM High Byte	T1PWMH	00	88
F0D	Timer 1 PWM Low Byte	T1PWML	00	89
F0E	Timer 1 Control 0	T1CTL0	00	83
F0F	Timer 1 Control 1	T1CTL1	00	84
F10–F6F	Reserved	—	XX	
<b>UART</b>				
F40	UART Transmit/Receive Data Registers	TXD, RXD	XX	113
F41	UART Status 0 Register	U0STAT0	00	111
F42	UART Control 0 Register	U0CTL0	00	108
F43	UART Control 1 Register	U0CTL1	00	108
F44	UART Status 1 Register	U0STAT1	00	112
F45	UART Address Compare Register	U0ADDR	00	114
F46	UART Baud Rate High Byte Register	U0BRH	FF	114
F47	UART Baud Rate Low Byte Register	U0BRL	FF	114
<b>Analog-to-Digital Converter (ADC)</b>				
F70	ADC Control 0	ADCCTL0	00	130
F71	ADC Control 1	ADCCTL1	80	130
F72	ADC Data High Byte	ADCD_H	XX	133
F73	ADC Data Low Bits	ADCD_L	XX	133
F74–F7F	Reserved	—	XX	
<b>Low Power Control</b>				
F80	Power Control 0	PWRCTL0	80	35
F81	Reserved	—	XX	
<b>LED Controller</b>				
F82	LED Drive Enable	LEDEN	00	52
F83	LED Drive Level High Byte	LEDLVLH	00	53
F84	LED Drive Level Low Byte	LEDLVLL	00	54
F85	Reserved	—	XX	
<b>Oscillator Control</b>				
F86	Oscillator Control	OSCCTL	A0	190
F87–F8F	Reserved	—	XX	
<b>Comparator 0</b>				
F90	Comparator 0 Control	CMP0	14	136
XX=Undefined				

**Table 11. Reset Status Register (RSTSTAT)**

BITS	7	6	5	4	3	2	1	0
FIELD	POR	STOP	WDT	EXT	Reserved			LVD
RESET	See descriptions below			0	0	0	0	0
R/W	R	R	R	R	R	R	R	R
ADDR	FF0H							

Reset or Stop Mode Recovery Event	POR	STOP	WDT	EXT
Power-On Reset	1	0	0	0
Reset using RESET pin assertion	0	0	0	1
Reset using Watchdog Timer time-out	0	0	1	0
Reset using the On-Chip Debugger (OCTCTL[1] set to 1)	1	0	0	0
Reset from STOP Mode using DBG Pin driven Low	1	0	0	0
Stop Mode Recovery using GPIO pin transition	0	1	0	0
Stop Mode Recovery using Watchdog Timer time-out	0	1	1	0

**POR**—Power-On Reset Indicator

If this bit is set to 1, a Power-On Reset event occurs. This bit is reset to 0 if a WDT time-out or Stop Mode Recovery occurs. This bit is also reset to 0 when the register is read.

**STOP**—Stop Mode Recovery Indicator

If this bit is set to 1, a Stop Mode Recovery occurs. If the STOP and WDT bits are both set to 1, the Stop Mode Recovery occurs because of a WDT time-out. If the STOP bit is 1 and the WDT bit is 0, the Stop Mode Recovery was not caused by a WDT time-out. This bit is reset by a Power-On Reset or a WDT time-out that occurred while not in STOP mode. Reading this register also resets this bit.

**WDT**—Watchdog Timer Time-Out Indicator

If this bit is set to 1, a WDT time-out occurs. A POR resets this pin. A Stop Mode Recovery from a change in an input pin also resets this bit. Reading this register resets this bit. This read must occur before clearing the WDT interrupt.

**EXT**—External Reset Indicator

If this bit is set to 1, a Reset initiated by the external RESET pin occurs. A Power-On Reset or a Stop Mode Recovery from a change in an input pin resets this bit. Reading this register resets this bit.

**Reserved**—Must be 0.

**LVD**—Low Voltage Detection Indicator

If this bit is set to 1 the current state of the supply voltage is below the low voltage detection threshold. This value is not latched but is a real-time indicator of the supply voltage level.

# Interrupt Controller

The interrupt controller on the Z8 Encore! XP F082A Series products prioritizes the interrupt requests from the on-chip peripherals and the GPIO port pins. The features of interrupt controller include:

- 20 possible interrupt sources with 18 unique interrupt vectors:
  - Twelve GPIO port pin interrupt sources (two interrupt vectors are shared).
  - Eight on-chip peripheral interrupt sources (two interrupt vectors are shared).
- Flexible GPIO interrupts:
  - Eight selectable rising and falling edge GPIO interrupts.
  - Four dual-edge interrupts.
- Three levels of individually programmable interrupt priority.
- Watchdog Timer and LVD can be configured to generate an interrupt.
- Supports vectored as well as polled interrupts

Interrupt requests (IRQs) allow peripheral devices to suspend CPU operation in an orderly manner and force the CPU to start an interrupt service routine (ISR). Usually this interrupt service routine is involved with the exchange of data, status information, or control information between the CPU and the interrupting peripheral. When the service routine is completed, the CPU returns to the operation from which it was interrupted.

The eZ8 CPU supports both vectored and polled interrupt handling. For polled interrupts, the interrupt controller has no effect on operation. For more information on interrupt servicing by the eZ8 CPU, refer to *eZ8 CPU Core User Manual (UM0128)* available for download at [www.zilog.com](http://www.zilog.com).

## Interrupt Vector Listing

Table 32 on page 56 lists all of the interrupts available in order of priority. The interrupt vector is stored with the most-significant byte (MSB) at the even Program Memory address and the least-significant byte (LSB) at the following odd Program Memory address.

► **Note:** *Some port interrupts are not available on the 8- and 20-pin packages. The ADC interrupt is unavailable on devices not containing an ADC.*

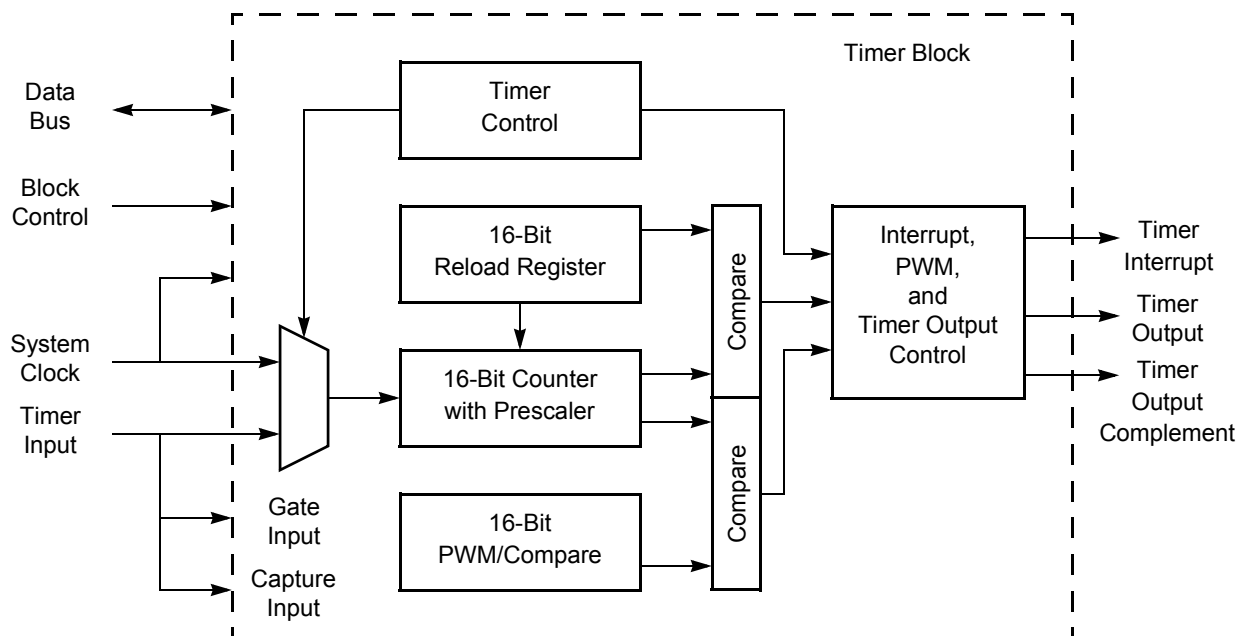


Figure 9. Timer Block Diagram

## Operation

The timers are 16-bit up-counters. Minimum time-out delay is set by loading the value 0001H into the Timer Reload High and Low Byte registers and setting the prescale value to 1. Maximum time-out delay is set by loading the value 0000H into the Timer Reload High and Low Byte registers and setting the prescale value to 128. If the Timer reaches FFFFH, the timer rolls over to 0000H and continues counting.

## Timer Operating Modes

The timers can be configured to operate in the following modes:

### ONE-SHOT Mode

In ONE-SHOT mode, the timer counts up to the 16-bit Reload value stored in the Timer Reload High and Low byte registers. The timer input is the system clock. Upon reaching the Reload value, the timer generates an interrupt and the count value in the Timer High and Low Byte registers is reset to 0001H. The timer is automatically disabled and stops counting.

### WDT Reset in Normal Operation

If configured to generate a Reset when a time-out occurs, the Watchdog Timer forces the device into the System Reset state. The WDT status bit in the Reset Status (RSTSTAT) register is set to 1. For more information on system reset, see [Reset, Stop Mode Recovery, and Low Voltage Detection](#) on page 23.

### WDT Reset in STOP Mode

If configured to generate a Reset when a time-out occurs and the device is in STOP mode, the Watchdog Timer initiates a Stop Mode Recovery. Both the WDT status bit and the STOP bit in the Reset Status (RSTSTAT) register are set to 1 following WDT time-out in STOP mode.

## Watchdog Timer Reload Unlock Sequence

Writing the unlock sequence to the Watchdog Timer (WDTCTL) Control register address unlocks the three Watchdog Timer Reload Byte registers (WDTU, WDTM, and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL register address produce no effect on the bits in the WDTCTL register. The locking mechanism prevents spurious writes to the Reload registers. Follow the steps below to unlock the Watchdog Timer Reload Byte registers (WDTU, WDTM, and WDTL) for write access.

1. Write 55H to the Watchdog Timer Control register (WDTCTL).
2. Write AAH to the Watchdog Timer Control register (WDTCTL).
3. Write the Watchdog Timer Reload Upper Byte register (WDTU) with the desired time-out value.
4. Write the Watchdog Timer Reload High Byte register (WDTM) with the desired time-out value.
5. Write the Watchdog Timer Reload Low Byte register (WDTL) with the desired time-out value.

All three Watchdog Timer Reload registers must be written in the order just listed. There must be no other register writes between each of these operations. If a register write occurs, the lock state machine resets and no further writes can occur unless the sequence is restarted. The value in the Watchdog Timer Reload registers is loaded into the counter when the Watchdog Timer is first enabled and every time a WDT instruction is executed.

## Watchdog Timer Calibration

Due to its extremely low operating current, the Watchdog Timer oscillator is somewhat inaccurate. This variation can be corrected using the calibration data stored in the Flash Information Page (see [Table 97](#) and [Table 98](#) on page 165). Loading these values into the

## UART Address Compare Register

The UART Address Compare (UxADDR) register stores the multi-node network address of the UART (see [Table 67](#)). When the MPMD[1] bit of UART Control Register 0 is set, all incoming address bytes are compared to the value stored in the Address Compare register. Receive interrupts and RDA assertions only occur in the event of a match.

**Table 67. UART Address Compare Register (U0ADDR)**

BITS	7	6	5	4	3	2	1	0
FIELD	COMP_ADDR							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F45H							

COMP\_ADDR—Compare Address  
This 8-bit value is compared to incoming address bytes.

## UART Baud Rate High and Low Byte Registers

The UART Baud Rate High (UxBRH) and Low Byte (UxBRL) registers ([Table 68](#) and [Table 69](#)) combine to create a 16-bit baud rate divisor value (BRG[15:0]) that sets the data transmission rate (baud rate) of the UART.

**Table 68. UART Baud Rate High Byte Register (U0BRH)**

BITS	7	6	5	4	3	2	1	0
FIELD	BRH							
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F46H							

**Table 69. UART Baud Rate Low Byte Register (U0BRL)**

BITS	7	6	5	4	3	2	1	0
FIELD	BRL							
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F47H							

**Table 77. Flash Code Protection Using the Flash Option Bits**

<b>FWP</b>	<b>Flash Code Protection Description</b>
0	Programming and erasing disabled for all of Flash Program Memory. In user code programming, Page Erase, and Mass Erase are all disabled. Mass Erase is available through the On-Chip Debugger.
1	Programming, Page Erase, and Mass Erase are enabled for all of Flash Program Memory.

### Flash Code Protection Using the Flash Controller

At Reset, the Flash Controller locks to prevent accidental program or erasure of the Flash memory. To program or erase the Flash memory, first write the Page Select Register with the target page. Unlock the Flash Controller by making two consecutive writes to the Flash Control register with the values 73H and 8CH, sequentially. The Page Select Register must be rewritten with the target page. If the two Page Select writes do not match, the controller reverts to a locked state. If the two writes match, the selected page becomes active. See [Figure 22](#) on page 144 for details.

After unlocking a specific page, you can enable either Page Program or Erase. Writing the value 95H causes a Page Erase only if the active page resides in a sector that is not protected. Any other value written to the Flash Control register locks the Flash Controller. Mass Erase is not allowed in the user code but only in through the Debug Port.

After unlocking a specific page, you can also write to any byte on that page. After a byte is written, the page remains unlocked, allowing for subsequent writes to other bytes on the same page. Further writes to the Flash Control Register cause the active page to revert to a locked state.

### Sector Based Flash Protection

The final protection mechanism is implemented on a per-sector basis. The Flash memories of Z8 Encore!<sup>®</sup> devices are divided into at most 8 sectors. A sector is 1/8 of the total size of the Flash memory, unless this value is smaller than the page size, in which case the sector and page sizes are equal.

The Sector Protect register controls the protection state of each Flash sector. This register is shared with the Page Select Register. It is accessed by writing 73H followed by 5EH to the Flash controller. The next write to the Flash Control Register targets the Sector Protect Register.

The Sector Protect Register is initialized to 0 on reset, putting each sector into an unprotected state. When a bit in the Sector Protect Register is written to 1, the corresponding sector is no longer written or erased by the CPU. External Flash programming through

**Flash Program Memory Address 0001H****Table 87. Flash Options Bits at Program Memory Address 0001H**

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved			XTLDIS	Reserved			
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	Program Memory 0001H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Reserved—Must be 1.

XTLDIS—State of Crystal Oscillator at Reset.

► **Note:** *This bit only enables the crystal oscillator. Its selection as system clock must be done manually.*

*0 = Crystal oscillator is enabled during reset, resulting in longer reset timing*

*1 = Crystal oscillator is disabled during reset, resulting in shorter reset timing*



**Warning:** *Programming the XTLDIS bit to zero on 8-pin versions of this device prevents any further communication via the debug pin. This is due to the fact that the XIN and DBG functions are shared on pin 2 of this package. Do not program this bit to zero on 8-pin devices unless no further debugging or Flash programming is required.*

**Trim Bit Address Space**

All available Trim bit addresses and their functions are listed in [Table 88](#) through [Table 92](#).

**Trim Bit Address 0000H****Table 88. Trim Options Bits at Address 0000H**

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	Information Page Memory 0020H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Reserved—Altering this register may result in incorrect device operation.

resides in working register R0. The bit fields of this status byte are defined in [Table 103](#). The contents of the status byte are undefined for write operations to illegal addresses. Also, user code must pop the address and data bytes off the stack.

The write routine uses 13 bytes of stack space in addition to the two bytes of address and data pushed by the user. Sufficient memory must be available for this stack usage.

Because of the Flash memory architecture, NVDS writes exhibit a non-uniform execution time. In general, a write takes 251  $\mu$ s (assuming a 20 MHz system clock). Every 400 to 500 writes, however, a maintenance operation is necessary. In this rare occurrence, the write takes up to 61 ms to complete. Slower system clock speeds result in proportionally higher execution times.

NVDS byte writes to invalid addresses (those exceeding the NVDS array size) have no effect. Illegal write operations have a 2  $\mu$ s execution time.

**Table 103. Write Status Byte**

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved				RCPY	PF	AWE	DWE
DEFAULT VALUE	0	0	0	0	0	0	0	0

Reserved—Must be 0.

RCPY—Recopy Subroutine Executed

A recopy subroutine was executed. These operations take significantly longer than a normal write operation.

PF—Power Failure Indicator

A power failure or system reset occurred during the most recent attempted write to the NVDS array.

AW—Address Write Error

An address byte failure occurred during the most recent attempted write to the NVDS array.

DWE—Data Write Error

A data byte failure occurred during the most recent attempted write to the NVDS array.

## Byte Read

To read a byte from the NVDS array, user code must first push the address onto the stack. User code issues a CALL instruction to the address of the byte-read routine (0x1000). At the return from the sub-routine, the read byte resides in working register R0, and the read status byte resides in working register R1. The contents of the status byte are undefined for

**Table 104. NVDS Read Time (Continued)**

<b>Operation</b>	<b>Minimum Latency</b>	<b>Maximum Latency</b>
Read (128 byte array)	883	7609
Write (16 byte array)	4973	5009
Write (64 byte array)	4971	5013
Write (128 byte array)	4984	5023
Illegal Read	43	43
Illegal Write	31	31

If NVDS read performance is critical to your software architecture, there are some things you can do to optimize your code for speed, listed in order from most helpful to least helpful:

- Periodically refresh all addresses that are used. The optimal use of NVDS in terms of speed is to rotate the writes evenly among all addresses planned to use, bringing all reads closer to the minimum read time. Because the minimum read time is much less than the write time, however, actual speed benefits are not always realized.
- Use as few unique addresses as possible: this helps to optimize the impact of refreshing as well as minimize the requirement for it.

If the device is not in DEBUG mode or the Flash Read Protect Option bit is enabled, this command reads and discards one byte.

DBG ← 12H

DBG ← 1-5 byte opcode

## On-Chip Debugger Control Register Definitions

### OCD Control Register

The OCD Control register controls the state of the On-Chip Debugger. This register is used to enter or exit DEBUG mode and to enable the BRK instruction. It can also reset the Z8 Encore! XP<sup>®</sup> F082A Series device.

A reset and stop function can be achieved by writing 81H to this register. A reset and go function can be achieved by writing 41H to this register. If the device is in DEBUG mode, a run function can be implemented by writing 40H to this register.

**Table 106. OCD Control Register (OCDCTL)**

BITS	7	6	5	4	3	2	1	0
FIELD	DBGMODE	BRKEN	DBGACK	Reserved				RST
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R	R	R	R	R/W

#### DBGMODE—DEBUG Mode

The device enters DEBUG mode when this bit is 1. When in DEBUG mode, the eZ8 CPU stops fetching new instructions. Clearing this bit causes the eZ8 CPU to restart. This bit is automatically set when a BRK instruction is decoded and Breakpoints are enabled. If the Flash Read Protect Option Bit is enabled, this bit can only be cleared by resetting the device. It cannot be written to 0.

0 = The Z8 Encore! XP F082A Series device is operating in NORMAL mode.

1 = The Z8 Encore! XP F082A Series device is in DEBUG mode.

#### BRKEN—Breakpoint Enable

This bit controls the behavior of the BRK instruction (opcode 00H). By default, Breakpoints are disabled and the BRK instruction behaves similar to an NOP instruction. If this bit is 1, when a BRK instruction is decoded, the DBGMODE bit of the OCDCTL register is automatically set to 1.

0 = Breakpoints are disabled.

1 = Breakpoints are enabled.

Table 124. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
XOR dst, src	dst ← dst XOR src	r	r	B2	–	*	*	0	–	–	2	3
		r	lr	B3							2	4
		R	R	B4							3	3
		R	IR	B5							3	4
		R	IM	B6							3	3
		IR	IM	B7							3	4
XORX dst, src	dst ← dst XOR src	ER	ER	B8	–	*	*	0	–	–	4	3
		ER	IM	B9							4	3
Flags Notation:	* = Value is a function of the result of the operation. – = Unaffected X = Undefined				0 = Reset to 0 1 = Set to 1							

**Table 125. Opcode Map Abbreviations**

<b>Abbreviation</b>	<b>Description</b>	<b>Abbreviation</b>	<b>Description</b>
b	Bit position	IRR	Indirect Register Pair
cc	Condition code	p	Polarity (0 or 1)
X	8-bit signed index or displacement	r	4-bit Working Register
DA	Destination address	R	8-bit register
ER	Extended Addressing register	r1, R1, Ir1, Irr1, IR1, rr1, RR1, IRR1, ER1	Destination address
IM	Immediate data value	r2, R2, Ir2, Irr2, IR2, rr2, RR2, IRR2, ER2	Source address
Ir	Indirect Working Register	RA	Relative
IR	Indirect register	rr	Working Register Pair
Irr	Indirect Working Register Pair	RR	Register Pair

**Table 128. Power Consumption**

<b>V<sub>DD</sub> = 2.7 V to 3.6 V</b>						
<b>Symbol</b>	<b>Parameter</b>	<b>Typical<sup>1</sup></b>	<b>Maximum<sup>2</sup> Maximum<sup>3</sup></b>		<b>Units</b>	<b>Conditions</b>
			<b>Std Temp</b>	<b>Ext Temp</b>		
I <sub>DD</sub> Stop	Supply Current in STOP Mode	0.1			μA	No peripherals enabled. All pins driven to V <sub>DD</sub> or V <sub>SS</sub> .
I <sub>DD</sub> Halt	Supply Current in HALT Mode (with all peripherals disabled)	35	55	65	μA	32 kHz
		520			μA	5.5 MHz
		2.1	2.85	2.85	mA	20 MHz
I <sub>DD</sub>	Supply Current in ACTIVE Mode (with all peripherals disabled)	2.8			mA	32 kHz
		4.5	5.2	5.2	mA	5.5 MHz
		5.5	6.5	6.5	mA	10 MHz
		7.9	11.5	11.5	mA	20 MHz
I <sub>DD</sub> WDT	Watchdog Timer Supply Current	0.9	1.0	1.1	μA	
I <sub>DD</sub> XTAL	Crystal Oscillator Supply Current	40			μA	32 kHz
		230			μA	4 MHz
		760			μA	20 MHz
I <sub>DD</sub> IPO	Internal Precision Oscillator Supply Current	350	500	550	μA	
I <sub>DD</sub> VBO	Voltage Brownout and Low-Voltage Detect Supply Current	50			μA	For 20-/28-pin devices (VBO only); See <a href="#">Notes 4</a> For 8-pin devices; See <a href="#">Notes 4</a>
I <sub>DD</sub> ADC	Analog to Digital Converter Supply Current (with External Reference)	2.8	3.1	3.2	mA	32 kHz
		3.1	3.6	3.7	mA	5.5 MHz
		3.3	3.7	3.8	mA	10 MHz
		3.7	4.2	4.3	mA	20 MHz
I <sub>DD</sub> ADCRef	ADC Internal Reference Supply Current	0			μA	See <a href="#">Notes 4</a>
I <sub>DD</sub> CMP	Comparator supply Current	150	180	190	μA	See <a href="#">Notes 4</a>

**Table 128. Power Consumption (Continued)**

$V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$						
Maximum <sup>2</sup> Maximum <sup>3</sup>						
Symbol	Parameter	Typical <sup>1</sup>	Std Temp	Ext Temp	Units	Conditions
$I_{DD}$ LPO	Low-Power Operational Amplifier Supply Current	3	5	5	$\mu\text{A}$	Driving a high-impedance load
$I_{DD}$ TS	Temperature Sensor Supply Current	60			$\mu\text{A}$	See <a href="#">Notes 4</a>
$I_{DD}$ BG	Band Gap Supply Current	320	480	500	$\mu\text{A}$	For 20-/28-pin devices
						For 8-pin devices

**Notes**

1. Typical conditions are defined as  $V_{DD} = 3.3 \text{ V}$  and  $+30 \text{ }^{\circ}\text{C}$ .
2. Standard temperature is defined as  $T_A = 0 \text{ }^{\circ}\text{C}$  to  $+70 \text{ }^{\circ}\text{C}$ ; these values not tested in production for worst case behavior, but are derived from product characterization and provided for design guidance only.
3. Extended temperature is defined as  $T_A = -40 \text{ }^{\circ}\text{C}$  to  $+105 \text{ }^{\circ}\text{C}$ ; these values not tested in production for worst case behavior, but are derived from product characterization and provided for design guidance only.
4. For this block to operate, the bandgap circuit is automatically turned on and must be added to the total supply current. This bandgap current is only added once, regardless of how many peripherals are using it.

Figure 40 displays the 8-pin Small Outline Integrated Circuit package (SOIC) available for the Z8 Encore! XP<sup>®</sup> F082A Series devices.

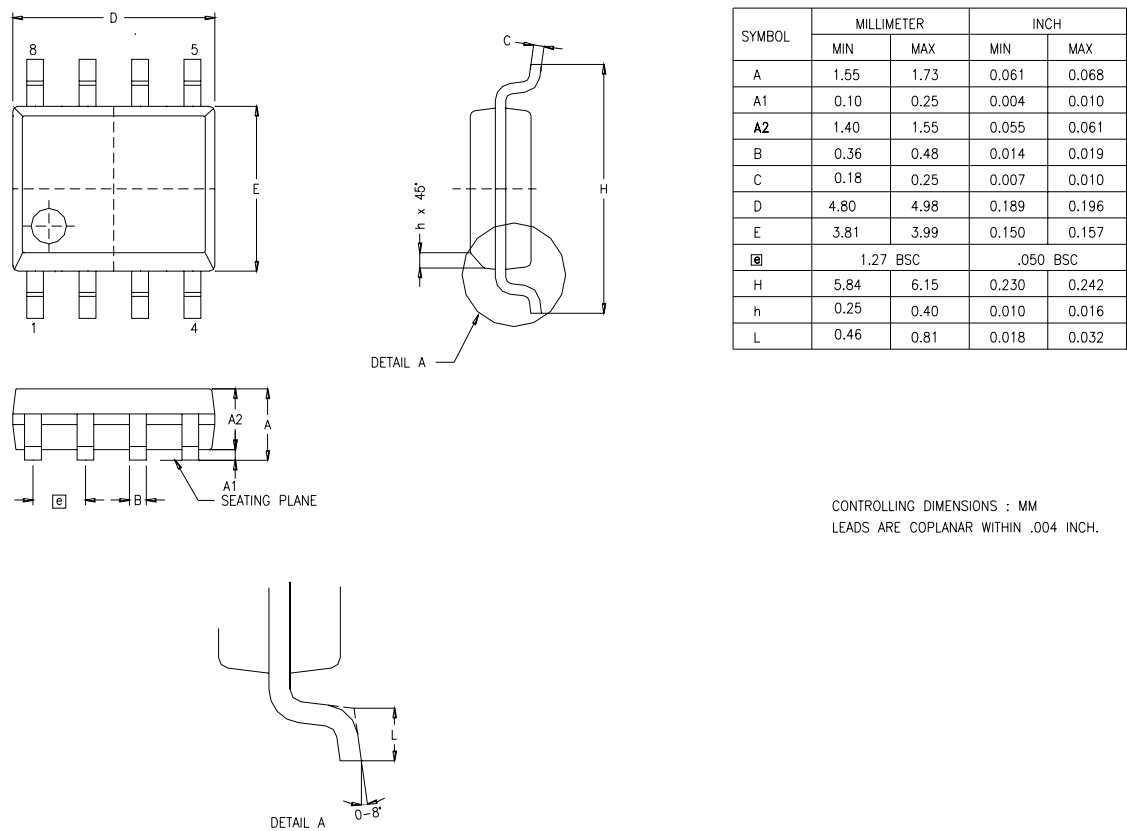


Figure 40. 8-Pin Small Outline Integrated Circuit Package (SOIC)

Figure 41 displays the 8-pin Quad Flat No-Lead package (QFN)/MLF-S available for the Z8 Encore! XP F082A Series devices. This package has a footprint identical to that of the 8-pin SOIC, but with a lower profile.

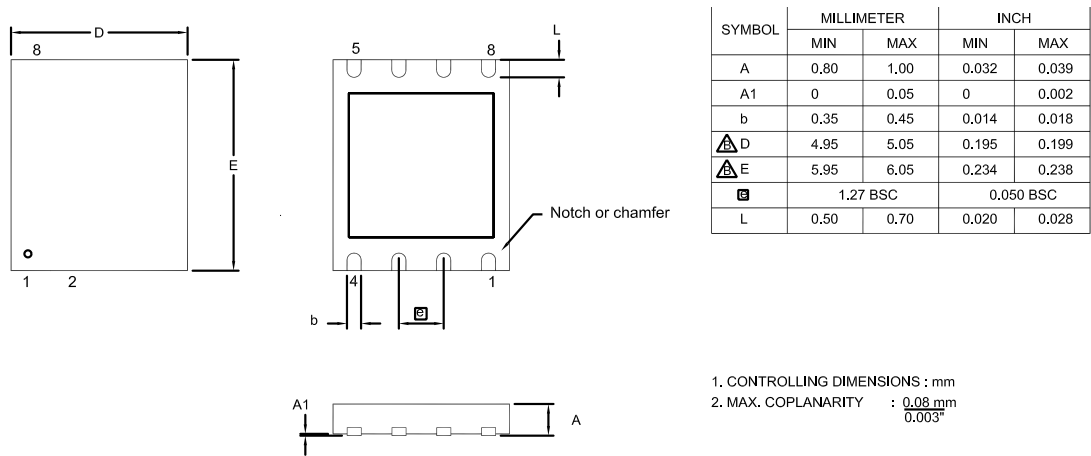


Figure 41. 8-Pin Quad Flat No-Lead Package (QFN)/MLF-S

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
<b>Z8 Encore! XP<sup>®</sup> F082A Series with 4 KB Flash, 10-Bit Analog-to-Digital Converter</b>											
<b>Standard Temperature: 0 °C to 70 °C</b>											
Z8F042APB020SC	4 KB	1 KB	128 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F042AQB020SC	4 KB	1 KB	128 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F042ASB020SC	4 KB	1 KB	128 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F042ASH020SC	4 KB	1 KB	128 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F042AHH020SC	4 KB	1 KB	128 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F042APH020SC	4 KB	1 KB	128 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F042ASJ020SC	4 KB	1 KB	128 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F042AHJ020SC	4 KB	1 KB	128 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F042APJ020SC	4 KB	1 KB	128 B	23	20	2	8	1	1	1	PDIP 28-pin package
<b>Extended Temperature: -40 °C to 105 °C</b>											
Z8F042APB020EC	4 KB	1 KB	128 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F042AQB020EC	4 KB	1 KB	128 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F042ASB020EC	4 KB	1 KB	128 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F042ASH020EC	4 KB	1 KB	128 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F042AHH020EC	4 KB	1 KB	128 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F042APH020EC	4 KB	1 KB	128 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F042ASJ020EC	4 KB	1 KB	128 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F042AHJ020EC	4 KB	1 KB	128 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F042APJ020EC	4 KB	1 KB	128 B	23	20	2	8	1	1	1	PDIP 28-pin package
Replace C with G for Lead-Free Packaging											

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
<b>Z8 Encore! XP<sup>®</sup> F082A Series with 2 KB Flash, 10-Bit Analog-to-Digital Converter</b>											
<b>Standard Temperature: 0 °C to 70 °C</b>											
Z8F022APB020SC	2 KB	512 B	64 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F022AQB020SC	2 KB	512 B	64 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F022ASB020SC	2 KB	512 B	64 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F022ASH020SC	2 KB	512 B	64 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F022AHH020SC	2 KB	512 B	64 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F022APH020SC	2 KB	512 B	64 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F022ASJ020SC	2 KB	512 B	64 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F022AHJ020SC	2 KB	512 B	64 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F022APJ020SC	2 KB	512 B	64 B	23	20	2	8	1	1	1	PDIP 28-pin package
<b>Extended Temperature: -40 °C to 105 °C</b>											
Z8F022APB020EC	2 KB	512 B	64 B	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F022AQB020EC	2 KB	512 B	64 B	6	14	2	4	1	1	1	QFN 8-pin package
Z8F022ASB020EC	2 KB	512 B	64 B	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F022ASH020EC	2 KB	512 B	64 B	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F022AHH020EC	2 KB	512 B	64 B	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F022APH020EC	2 KB	512 B	64 B	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F022ASJ020EC	2 KB	512 B	64 B	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F022AHJ020EC	2 KB	512 B	64 B	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F022APJ020EC	2 KB	512 B	64 B	23	20	2	8	1	1	1	PDIP 28-pin package
Replace C with G for Lead-Free Packaging											

## Part Number Suffix Designations

Z8 F 04 2A S H 020 S C

### Environmental Flow

C = Standard Plastic Packaging Compound  
G = Green Plastic Packaging Compound

### Temperature Range

S = Standard, 0 °C to 70 °C  
E = Extended, -40 °C to +105 °C

### Speed

020 = 20 MHz

### Pin Count

B = 8  
H = 20  
J = 28

### Package

H = SSOP  
P = PDIP  
Q = QFN  
S = SOIC

### Device Type

2A = Contains Advanced Analog Peripherals  
1A = Does Not Contain Advanced Analog Peripherals

### Memory Size

08 = 8 KB Flash, 1 KB RAM, 0 B NVDS  
04 = 4 KB Flash, 1 KB RAM, 128 B NVDS  
02 = 2 KB Flash, 512 B RAM, 64 B NVDS  
01 = 1 KB Flash, 256 B RAM, 16 B NVDS

### Memory Type

F = Flash

### Device Family

Z8 = Zilog's 8-Bit Microcontroller