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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f041ahh020sc

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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- Up to thirteen 5 V-tolerant input pins
- Up to 8 ports capable of direct LED drive with no current limit resistor required
- On-Chip Debugger (OCD)
- Voltage Brownout (VBO) protection
- Programmable low battery detection (LVD) (8-pin devices only)
- Bandgap generated precision voltage references available for the ADC, comparator, VBO, and LVD
- Power-On Reset (POR)
- 2.7 V to 3.6 V operating voltage
- 8-, 20-, and 28-pin packages
- 0 °C to +70 °C and -40 °C to +105 °C for operating temperature ranges

Part Selection Guide

Table 1 on page 3 identifies the basic features and package styles available for each device within the Z8 Encore! $XP^{\ensuremath{\mathbb{R}}}$ F082A Series product line.



Block Diagram

Figure 1 displays the block diagram of the architecture of the Z8 Encore! XP[®] F082A Series devices.



Figure 1. Z8 Encore! XP F082A Series Block Diagram



Low-Power Operational Amplifier

The optional low-power operational amplifier (LPO) is a general-purpose amplifier primarily targeted for current sense applications. The LPO output may be routed internally to the ADC or externally to a pin.

Internal Precision Oscillator

The internal precision oscillator (IPO) is a trimmable clock source that requires no external components.

Temperature Sensor

The optional temperature sensor produces an analog output proportional to the device temperature. This signal can be sent to either the ADC or the analog comparator.

Analog Comparator

The analog comparator compares the signal at an input pin with either an internal programmable voltage reference or a second input pin. The comparator output can be used to drive either an output pin or to generate an interrupt.

External Crystal Oscillator

The crystal oscillator circuit provides highly accurate clock frequencies with the use of an external crystal, ceramic resonator or RC network.

Low Voltage Detector

The low voltage detector (LVD) is able to generate an interrupt when the supply voltage drops below a user-programmable level. The LVD is available on 8-pin devices only.

On-Chip Debugger

The Z8 Encore! XP[®] F082A Series products feature an integrated on-chip debugger (OCD) accessed via a single-pin interface. The OCD provides a rich-set of debugging capabilities, such as reading and writing registers, programming Flash memory, setting breakpoints, and executing code.

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Program Memory Address (Hex)	Function
Z8F022A and Z8F021A Products	
0000–0001	Flash Option Bits
0002–0003	Reset Vector
0004–0005	WDT Interrupt Vector
0006–0007	Illegal Instruction Trap
0008–0037	Interrupt Vectors*
0038–0039	Reserved
003A-003D	Oscillator Fail Trap Vectors
003E-07FF	Program Memory
Z8F012A and Z8F011A Products	
0000–0001	Flash Option Bits
0002–0003	Reset Vector
0004–0005	WDT Interrupt Vector
0006–0007	Illegal Instruction Trap
0008–0037	Interrupt Vectors*
0038–0039	Reserved
003A-003D	Oscillator Fail Trap Vectors
003E-03FF	Program Memory
* See Table 32 on page 56 for a list of the in	nterrupt vectors.

Table 5. Z8 Encore! XP F082A Series Program Memory Maps (Continued)

Data Memory

The Z8 Encore! XP F082A Series does not use the eZ8 CPU's 64 KB Data Memory address space.

Flash Information Area

Table 6 on page 18 describes the Z8 Encore! XP F082A Series Flash Information Area. This 128 B Information Area is accessed by setting bit 7 of the Flash Page Select Register to 1. When access is enabled, the Flash Information Area is mapped into the Program Memory and overlays the 128 bytes at addresses FE00H to FF7FH. When the Information Area access is enabled, all reads from these Program Memory addresses return the Infor-

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vector address. Following Stop Mode Recovery, the STOP bit in the Reset Status (RSTSTAT) Register is set to 1. Table 10 lists the Stop Mode Recovery sources and resulting actions. The text following provides more detailed information about each of the Stop Mode Recovery sources.

Operating Mode	Stop Mode Recovery Source	Action	
STOP mode	Watchdog Timer time-out when configured for Reset	Stop Mode Recovery	
	Watchdog Timer time-out when configured for interrupt	Stop Mode Recovery followed by interrupt (if interrupts are enabled)	
	Data transition on any GPIO Port pin enabled as a Stop Mode Recovery source	Stop Mode Recovery	
	Assertion of external RESET Pin	System Reset	
	Debug Pin driven Low	System Reset	

Table 10. Stop Mode Recovery Sources and Resulting Action

Stop Mode Recovery Using Watchdog Timer Time-Out

If the Watchdog Timer times out during STOP mode, the device undergoes a Stop Mode Recovery sequence. In the Reset Status (RSTSTAT) register, the WDT and STOP bits are set to 1. If the Watchdog Timer is configured to generate an interrupt upon time-out and the Z8 Encore! XP F082A Series device is configured to respond to interrupts, the eZ8 CPU services the Watchdog Timer interrupt request following the normal Stop Mode Recovery sequence.

Stop Mode Recovery Using a GPIO Port Pin Transition

Each of the GPIO Port pins may be configured as a Stop Mode Recovery input source. On any GPIO pin enabled as a Stop Mode Recovery source, a change in the input pin value (from High to Low or from Low to High) initiates Stop Mode Recovery.

Note: The SMR pulses shorter than specified does not trigger a recovery (see Table 131 on page 229). When this happens, the STOP bit in the Reset Status (RSTSTAT) register is set to 1.

Caution: In STOP mode, the GPIO Port Input Data registers (PxIN) are disabled. The Port Input Data registers record the Port transition only if the signal stays on the Port pin through the end of the Stop Mode Recovery delay. As a result, short pulses on the Port pin can





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Set 1 Sub-Registers on page 50, GPIO Alternate Functions on page 38, and Port A–D Alternate Function Set 2 Sub-Registers on page 51. See GPIO Alternate Functions on page 38 to determine the alternate function associated with each port pin.

Caution:

Do not enable alternate functions for GPIO port pins for which there is no associated alternate function. Failure to follow this guideline can result in unpredictable operation.

Table 20. F	Port A–D	Alternate	Function	Sub-Regis	ters (Px	AF)

BITS	7	6	5	4	3	2	1	0				
FIELD	AF7	AF6	AF5	AF4	AF3	AF2	AF1	AF0				
RESET	00H (Ports A–C); 01H (Port D); 04H (Port A of 8-pin device)											
R/W		R/W										
ADDR	lf 02H i	n Port A–D /	Address Reg	gister, acces	sible throug	n the Port A-	–D Control F	≀egister				

AF[7:0]—Port Alternate Function enabled

0 = The port pin is in normal mode and the DDx bit in the Port A–D Data Direction sub-register determines the direction of the pin.

1 = The alternate function selected through Alternate Function Set sub-registers is enabled. Port pin operation is controlled by the alternate function.

Port A–D Output Control Sub-Registers

The Port A–D Output Control sub-register (Table 21) is accessed through the Port A–D Control register by writing 03H to the Port A–D Address register. Setting the bits in the Port A–D Output Control sub-registers to 1 configures the specified port pins for opendrain operation. These sub-registers affect the pins directly and, as a result, alternate functions are also affected.

Table 21. Port A–D Output Control Sub-Registers (PxOC)

BITS	7	6	5	4	3	2	1	0
FIELD	POC7	POC6	POC5	POC4	POC3	POC2	POC1	POC0
RESET			001	H (Ports A-C	;); 01H (Port	D)		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	lf 03H i	n Port A–D /	Address Reg	gister, acces	sible throug	n the Port A-	-D Control F	Register

POC[7:0]—Port Output Control

These bits function independently of the alternate function bit and always disable the drains if set to 1.

0 = The source current is enabled for any output mode (unless overridden by the alternate



function). (Push-pull output)

1 = The source current for the associated pin is disabled (open-drain mode).

Port A–D High Drive Enable Sub-Registers

The Port A–D High Drive Enable sub-register (Table 22) is accessed through the Port A–D Control register by writing 04H to the Port A–D Address register. Setting the bits in the Port A–D High Drive Enable sub-registers to 1 configures the specified port pins for high current output drive operation. The Port A–D High Drive Enable sub-register affects the pins directly and, as a result, alternate functions are also affected.

Table 22. Port A–D High Drive Enable Sub-Registers (PxHDE)

BITS	7	6	5	4	3	2	1	0
FIELD	PHDE7	PHDE6	PHDE5	PHDE4	PHDE3	PHDE2	PHDE1	PHDE0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	lf 04H i	n Port A–D	Address Reg	gister, acces	sible throug	h the Port A-	-D Control F	Register

PHDE[7:0]—Port High Drive Enabled

0 = The Port pin is configured for standard output current drive.

1 = The Port pin is configured for high output current drive.

Port A–D Stop Mode Recovery Source Enable Sub-Registers

The Port A–D Stop Mode Recovery Source Enable sub-register (Table 23) is accessed through the Port A–D Control register by writing 05H to the Port A–D Address register. Setting the bits in the Port A–D Stop Mode Recovery Source Enable sub-registers to 1 configures the specified Port pins as a Stop Mode Recovery source. During STOP mode, any logic transition on a Port pin enabled as a Stop Mode Recovery source initiates Stop Mode Recovery.

Table 23. Port A–D Stop Mode Recove	ry Source Enable Sub-Registers (PxSMRE)
-------------------------------------	---

BITS	7	6	5	4	3	2	1	0		
FIELD	PSMRE7	PSMRE6	PSMRE5	PSMRE4	PSMRE3	PSMRE2	PSMRE1	PSMRE0		
RESET	0	0	0	0	0	0	0	0		
R/W	R/W	R/W R/W R/W R/W R/W R/W R/W								
ADDR	lf 05H i	n Port A–D	Address Reg	gister, acces	sible throug	n the Port A-	-D Control F	Register		

PSMRE[7:0]—Port Stop Mode Recovery Source Enabled

0 = The Port pin is not configured as a Stop Mode Recovery source. Transitions on this pin



Table 39. IRQ1 Enable and Priority Encoding

IRQ1ENH[x]	IRQ1ENL[x]	Priority	Description
0	0	Disabled	Disabled
0	1	Level 1	Low
1	0	Level 2	Medium
1	1	Level 3	High

where x indicates the register bits from 0–7.

Table 40. IRQ1 Enable High Bit Register (IRQ1ENH)

BITS	7	6	5	4	3	2	1	0
FIELD	PA7VENH	PA6CENH	PA5ENH	PA4ENH	PA3ENH	PA2ENH	PA1ENH	PA0ENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR				FC	4H			

PA7VENH—Port A Bit[7] or LVD Interrupt Request Enable High Bit PA6CENH—Port A Bit[7] or Comparator Interrupt Request Enable High Bit PAxENH—Port A Bit[x] Interrupt Request Enable High Bit

See Shared Interrupt Select (IRQSS) register for selection of either the LVD or the comparator as the interrupt source.

Table 41. IRQ1 Enable Low Bit Register (IRQ1ENL)

BITS	7	6	5	4	3	2	1	0
FIELD	PA7VENL	PA6CENL	PA5ENL	PA4ENL	PA3ENL	PA2ENL	PA1ENL	PA0ENL
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR				FC	5H			

PA7VENL—Port A Bit[7] or LVD Interrupt Request Enable Low Bit PA6CENL—Port A Bit[6] or Comparator Interrupt Request Enable Low Bit PAxENL—Port A Bit[x] Interrupt Request Enable Low Bit



Reserved—Must be 0.

C3ENL—Port C3 Interrupt Request Enable Low Bit C2ENL—Port C2 Interrupt Request Enable Low Bit C1ENL—Port C1 Interrupt Request Enable Low Bit C0ENL—Port C0 Interrupt Request Enable Low Bit

Interrupt Edge Select Register

The Interrupt Edge Select (IRQES) register (Table 45) determines whether an interrupt is generated for the rising edge or falling edge on the selected GPIO Port A input pin.

Table 45. Interrupt Edge Select Register (IRQES)

BITS	7	6	5	4	3	2	1	0
FIELD	IES7	IES6	IES5	IES4	IES3	IES2	IES1	IES0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FCDH							

IES*x*—Interrupt Edge Select *x*

0 = An interrupt request is generated on the falling edge of the PAx input.

1 = An interrupt request is generated on the rising edge of the PAx input.

where *x* indicates the specific GPIO Port pin number (0 through 7).

Shared Interrupt Select Register

The Shared Interrupt Select (IRQSS) register (Table 46) determines the source of the PADxS interrupts. The Shared Interrupt Select register selects between Port A and alternate sources for the individual interrupts.

Because these shared interrupts are edge-triggered, it is possible to generate an interrupt just by switching from one shared source to another. For this reason, an interrupt must be disabled before switching between sources.



Follow the steps below for configuring a timer for COMPARE mode and initiating the count:

- 1. Write to the Timer Control register to:
 - Disable the timer.
 - Configure the timer for COMPARE mode.
 - Set the prescale value.
 - Set the initial logic level (High or Low) for the Timer Output alternate function, if appropriate.
- 2. Write to the Timer High and Low Byte registers to set the starting count value.
- 3. Write to the Timer Reload High and Low Byte registers to set the Compare value.
- 4. Enable the timer interrupt, if appropriate, and set the timer interrupt priority by writing to the relevant interrupt registers.
- 5. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
- 6. Write to the Timer Control register to enable the timer and initiate counting.

In COMPARE mode, the system clock always provides the timer input. The Compare time can be calculated by the following equation:

COMPARE Mode Time (s) = $\frac{(Compare Value - Start Value) \times Prescale}{System Clock Frequency (Hz)}$

GATED Mode

In GATED mode, the timer counts only when the Timer Input signal is in its active state (asserted), as determined by the TPOL bit in the Timer Control register. When the Timer Input signal is asserted, counting begins. A timer interrupt is generated when the Timer Input signal is deasserted or a timer reload occurs. To determine if a Timer Input signal deassertion generated the interrupt, read the associated GPIO input value and compare to the value stored in the TPOL bit.

The timer counts up to the 16-bit Reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. When reaching the Reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes (assuming the Timer Input signal remains asserted). Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer reset.

Follow the steps below for configuring a timer for GATED mode and initiating the count:

- 1. Write to the Timer Control register to:
 - Disable the timer.
 - Configure the timer for GATED mode.
 - Set the prescale value.



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3.579545 MHz System Clock						
Acceptable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)			
1250.0	N/A	N/A	N/A			
625.0	N/A	N/A	N/A			
250.0	1	223.72	-10.51			
115.2	2	111.9	-2.90			
57.6	4	55.9	-2.90			
38.4	6	37.3	-2.90			
19.2	12	18.6	-2.90			
9.60	23	9.73	1.32			
4.80	47	4.76	-0.83			
2.40	93	2.41	0.23			
1.20	186	1.20	0.23			
0.60	373	0.60	-0.04			
0.30	746	0.30	-0.04			
-						

Table 70. UART Baud Rates (Continued)

1.8432 MHz System Clock						
Acceptable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)			
1250.0	N/A	N/A	N/A			
625.0	N/A	N/A	N/A			
250.0	N/A	N/A	N/A			
115.2	1	115.2	0.00			
57.6	2	57.6	0.00			
38.4	3	38.4	0.00			
19.2	6	19.2	0.00			
9.60	12	9.60	0.00			
4.80	24	4.80	0.00			
2.40	48	2.40	0.00			
1.20	96	1.20	0.00			
0.60	192	0.60	0.00			
0.30	384	0.30	0.00			

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WDTCALH—Watchdog Timer Calibration High Byte The WDTCALH and WDTCALL bytes, when loaded into the Watchdog Timer reload registers result in a one second timeout at room temperature and 3.3 V supply voltage. To use the Watchdog Timer calibration, user code must load WDTU with 0x00, WDTH with WDTCALH and WDTL with WDTCALL.

Table 98. Watchdog Calibration Low Byte at 007FH (WDTCALL)

BITS	7	6	5	4	3	2	1	0
FIELD	WDTCALL							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	Information Page Memory 007FH							
Note: U = Unchanged by Reset. R/W = Read/Write.								

WDTCALL—Watchdog Timer Calibration Low Byte

The WDTCALH and WDTCALL bytes, when loaded into the Watchdog Timer reload registers result in a one second timeout at room temperature and 3.3 V supply voltage. To use the Watchdog Timer calibration, user code must load WDTU with 0x00, WDTH with WDTCALH and WDTL with WDTCALL.

Serialization Data

Table 99. Serial Number at 001C - 001F (S_NUM)

BITS	7	6	5	4	3	2	1	0
FIELD	S_NUM							
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	Information Page Memory 001C-001F							
Note: U = Unchanged by Reset. R/W = Read/Write.								

S NUM—Serial Number Byte

The serial number is a unique four-byte binary value.

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Debug Command	Command Byte	Enabled when NOT in DEBUG mode?	Disabled by Flash Read Protect Option Bit
Write Register	08H	_	Only writes of the Flash Memory Control registers are allowed. Additionally, only the Mass Erase command is allowed to be written to the Flash Control register.
Read Register	09H	_	Disabled
Write Program Memory	0AH	_	Disabled
Read Program Memory	0BH	_	Disabled
Write Data Memory	0CH	_	Yes
Read Data Memory	0DH	_	-
Read Program Memory CRC	0EH	_	-
Reserved	0FH	_	-
Step Instruction	10H	_	Disabled
Stuff Instruction	11H	_	Disabled
Execute Instruction	12H	_	Disabled
Reserved	13H–FFH	_	_

In the following bulleted list of OCD Commands, data and commands sent from the host to the On-Chip Debugger are identified by 'DBG \leftarrow Command/Data'. Data sent from the On-Chip Debugger back to the host is identified by 'DBG \rightarrow Data'

• **Read OCD Revision (00H)**—The Read OCD Revision command determines the version of the On-Chip Debugger. If OCD commands are added, removed, or changed, this revision number changes.

```
DBG \leftarrow 00H
DBG \rightarrow OCDRev[15:8] (Major revision number)
DBG \rightarrow OCDRev[7:0] (Minor revision number)
```

• **Read OCD Status Register (02H)**—The Read OCD Status Register command reads the OCDSTAT register.

```
DBG \leftarrow 02H
DBG \rightarrow OCDSTAT[7:0]
```

• **Read Runtime Counter (03H)**—The Runtime Counter counts system clock cycles in between Breakpoints. The 16-bit Runtime Counter counts up from 0000H and stops at the maximum count of FFFFH. The Runtime Counter is overwritten during the

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eZ8 CPU Instruction Set

Assembly Language Programming Introduction

The eZ8 CPU assembly language provides a means for writing an application program without concern for actual memory addresses or machine instruction formats. A program written in assembly language is called a source program. Assembly language allows the use of symbolic addresses to identify memory locations. It also allows mnemonic codes (opcodes and operands) to represent the instructions themselves. The opcodes identify the instruction while the operands represent memory locations, registers, or immediate data values.

Each assembly language program consists of a series of symbolic commands called statements. Each statement can contain labels, operations, operands and comments.

Labels can be assigned to a particular instruction step in a source program. The label identifies that step in the program as an entry point for use by other instructions.

The assembly language also includes assembler directives that supplement the machine instruction. The assembler directives, or pseudo-ops, are not translated into a machine instruction. Rather, the pseudo-ops are interpreted as directives that control or assist the assembly process.

The source program is processed (assembled) by the assembler to obtain a machine language program called the object code. The object code is executed by the eZ8 CPU. An example segment of an assembly language program is detailed in the following example.

Assembly Language Source Program Example

JP START	; Everything after the semicolon is a comment.
START:	; A label called 'START'. The first instruction (JP START) in this ; example causes program execution to jump to the point within the ; program where the START label occurs.
LD R4, R7	; A Load (LD) instruction with two operands. The first operand, ; Working Register R4, is the destination. The second operand, ; Working Register R7, is the source. The contents of R7 is ; written into R4.
LD 234H, #%01	; Another Load (LD) instruction with two operands. ; The first operand, Extended Mode Register Address 234H, ; identifies the destination. The second operand, Immediate Data
	; value 01H, is the source. The value 01H is written into the ; Register at address 234H.

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Abbreviation	Description	Abbreviation	Description
b	Bit position	IRR	Indirect Register Pair
СС	Condition code	р	Polarity (0 or 1)
X	8-bit signed index or displacement	r	4-bit Working Register
DA	Destination address	R	8-bit register
ER	Extended Addressing register	r1, R1, Ir1, Irr1, IR1, rr1, RR1, IRR1, ER1	Destination address
IM	Immediate data value	r2, R2, Ir2, Irr2, IR2, rr2, RR2, IRR2, ER2	Source address
Ir	Indirect Working Register	RA	Relative
IR	Indirect register	rr	Working Register Pair
Irr	Indirect Working Register Pair	RR	Register Pair

Table 125. Opcode Map Abbreviations



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Figure 43 displays the 20-pin Small Outline Integrated Circuit Package (SOIC) available for the Z8 Encore! XP F082A Series devices.

Figure 43. 20-Pin Small Outline Integrated Circuit Package (SOIC)

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Note: ZILOG supplies both options for production. Component layout PCB design should cover bigger option 01.

Figure 45. 28-Pin Plastic Dual Inline Package (PDIP)