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Zilog - Z8F042AHH020EC00TR Datasheet



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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f042ahh020ec00tr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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and as long as four. A reset pulse three clock cycles in duration might trigger a reset; a pulse four cycles in duration always triggers a reset.

While the $\overline{\text{RESET}}$ input pin is asserted Low, the Z8 Encore! XP[®] F082A Series devices remain in the Reset state. If the $\overline{\text{RESET}}$ pin is held Low beyond the System Reset timeout, the device exits the Reset state on the system clock rising edge following $\overline{\text{RESET}}$ pin deassertion. Following a System Reset initiated by the external $\overline{\text{RESET}}$ pin, the EXT status bit in the Reset Status (RSTSTAT) register is set to 1.

External Reset Indicator

During System Reset or when enabled by the GPIO logic (see Port A–D Control Registers on page 46), the RESET pin functions as an open-drain (active Low) reset mode indicator in addition to the input functionality. This reset output feature allows a Z8 Encore! XP F082A Series device to reset other components to which it is connected, even if that reset is caused by internal sources such as POR, VBO or WDT events.

After an internal reset event occurs, the internal circuitry begins driving the RESET pin Low. The RESET pin is held Low by the internal circuitry until the appropriate delay listed in Table 8 has elapsed.

On-Chip Debugger Initiated Reset

A Power-On Reset can be initiated using the On-Chip Debugger by setting the RST bit in the OCD Control register. The On-Chip Debugger block is not reset but the rest of the chip goes through a normal system reset. The RST bit automatically clears during the system reset. Following the system reset the POR bit in the Reset Status (RSTSTAT) register is set.

Stop Mode Recovery

STOP mode is entered by execution of a STOP instruction by the eZ8 CPU. See Low-Power Modes on page 33 for detailed STOP mode information. During Stop Mode Recovery (SMR), the CPU is held in reset for 66 IPO cycles if the crystal oscillator is disabled or 5000 cycles if it is enabled. The SMR delay (see Table 131 on page 229) T_{SMR} , also includes the time required to start up the IPO.

Stop Mode Recovery does not affect on-chip registers other than the Watchdog Timer Control register (WDTCTL) and the Oscillator Control register (OSCCTL). After any Stop Mode Recovery, the IPO is enabled and selected as the system clock. If another system clock source is required, the Stop Mode Recovery code must reconfigure the oscillator control block such that the correct system clock source is enabled and selected.

The eZ8 CPU fetches the Reset vector at Program Memory addresses 0002H and 0003H and loads that value into the Program Counter. Program execution begins at the Reset

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PA0 and PA6 contain two different timer functions, a timer input and a complementary timer output. Both of these functions require the same GPIO configuration, the selection between the two is based on the timer mode. See Timers on page 69 for more details.



Caution: For pin with multiple alternate functions, it is recommended to write to the AFS1 and AFS2 sub-registers before enabling the alternate function via the AF sub-register. This prevents spurious transitions through unwanted alternate function modes.

Direct LED Drive

The Port C pins provide a current sinked output capable of driving an LED without requiring an external resistor. The output sinks current at programmable levels of 3 mA, 7 mA, 13 mA and 20 mA. This mode is enabled through the Alternate Function sub-register AFS1 and is programmable through the LED control registers. The LED Drive Enable (LEDEN) register turns on the drivers. The LED Drive Level (LEDLVLH and LEDLVLL) registers select the sink current.

For correct function, the LED anode must be connected to V_{DD} and the cathode to the GPIO pin. Using all Port C pins in LED drive mode with maximum current may result in excessive total current. See Electrical Characteristics on page 221 for the maximum total current for the applicable package.

Shared Reset Pin

On the 20- and 28-pin devices, the PD0 pin shares function with a bi-directional reset pin. Unlike all other I/O pins, this pin does not default to GPIO function on power-up. This pin acts as a bi-directional reset until the software re-configures it. The PD0 pin is output-only when in GPIO mode.

On the 8-pin product versions, the reset pin is shared with PA2, but the pin is not limited to output-only when in GPIO mode.



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Caution: If PA2 on the 8-pin product is reconfigured as an input, ensure that no external stimulus drives the pin low during any reset sequence. Since PA2 returns to its RESET alternate function during system resets, driving it Low holds the chip in a reset state until the pin is released.

Shared Debug Pin

On the 8-pin version of this device only, the Debug pin shares function with the PA0 GPIO pin. This pin performs as a general purpose input pin on power-up, but the debug logic monitors this pin during the reset sequence to determine if the unlock sequence occurs. If the unlock sequence is present, the debug function is unlocked and the pin no longer func-



Table 31. LED Drive Level Low Register (LEDLVLL)

BITS	7	6	5	4	3	2	1	0
FIELD		LEDLVLL[7:0]						
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR		F84H						

LEDLVLL[7:0]—LED Level Low Bit

{LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin.

00 = 3 mA01 = 7 mA10 = 13 mA

11 = 20 mA



IRQ2 Enable High and Low Bit Registers

Table 42 describes the priority control for IRQ2. The IRQ2 Enable High and Low Bit registers (Table 43 and Table 44) form a priority encoded enabling for interrupts in the Interrupt Request 2 register.

IRQ2ENH[x]	IRQ2ENL[x]	Priority	Description
0	0	Disabled	Disabled
0	1	Level 1	Low
1	0	Level 2	Medium
1	1	Level 3	High

Table 42. IRQ2 Enable and Priority Encoding

where x indicates the register bits from 0–7.

Table 43. IRQ2 Enable High Bit Register (IRQ2ENH)

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved			C3ENH	C2ENH	C1ENH	C0ENH	
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W R/W <th>R/W</th>					R/W	
ADDR				FC	7H			

Reserved—Must be 0.

C3ENH—Port C3 Interrupt Request Enable High Bit C2ENH—Port C2 Interrupt Request Enable High Bit C1ENH—Port C1 Interrupt Request Enable High Bit C0ENH—Port C0 Interrupt Request Enable High Bit

Table 44. IRQ2 Enable Low Bit Register (IRQ2ENL)

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved			C3ENL	C2ENL	C1ENL	C0ENL	
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR				FC	:8H			





- 4. Enable the timer interrupt, if appropriate, and set the timer interrupt priority by writing to the relevant interrupt registers.By default, the timer interrupt are generated for both input capture and reload events. If appropriate, configure the timer interrupt to be generated only at the input capture event or the reload event by setting TICONFIG field of the TxCTL0 register.
- 5. Configure the associated GPIO port pin for the Timer Input alternate function.
- 6. Write to the Timer Control register to enable the timer.
- 7. Counting begins on the first appropriate transition of the Timer Input signal. No interrupt is generated by this first edge.

In CAPTURE/COMPARE mode, the elapsed time from timer start to Capture event can be calculated using the following equation:

Capture Elapsed Time (s) = $\frac{(Capture Value - Start Value) \times Prescale}{System Clock Frequency (Hz)}$

Reading the Timer Count Values

The current count value in the timers can be read while counting (enabled). This capability has no effect on timer operation. When the timer is enabled and the Timer High Byte register is read, the contents of the Timer Low Byte register are placed in a holding register. A subsequent read from the Timer Low Byte register returns the value in the holding register. This operation allows accurate reads of the full 16-bit timer count value while enabled. When the timers are not enabled, a read from the Timer Low Byte register returns the actual value in the counter.

Timer Pin Signal Operation

Timer Output is a GPIO Port pin alternate function. The Timer Output is toggled every time the counter is reloaded.

The Timer Input can be used as a selectable counting source. It shares the same pin as the complementary timer output. When selected by the GPIO Alternate Function Registers, this pin functions as a timer input in all modes except for the DUAL PWM OUTPUT mode. For this mode, there is no timer input available.



Caution: *The 24-bit WDT Reload Value must not be set to a value less than* 000004H.

Table 58. Watchdog Timer Reload Upper Byte Register (WDTU)

BITS	7	6	5	4	3	2	1	0
FIELD		WDTU						
RESET		00H						
R/W		R/W*						
ADDR	FF1H							
R/W/* - Rea	R/W* - Read returns the current WDT count value. Write sets the appropriate Reload Value							

R/W* - Read returns the current WDT count value. Write sets the appropriate Reload Value.

WDTU—WDT Reload Upper Byte

Most-significant byte (MSB), Bits[23:16], of the 24-bit WDT reload value.

Table 59. Watchdog Timer Reload High Byte Register (WDTH)

BITS	7	6	5	4	3	2	1	0
FIELD		WDTH						
RESET		04H						
R/W	R/W*							
ADDR	FF2H							
R/W* - Read returns the current WDT count value. Write sets the appropriate Reload Value.								

WDTH—WDT Reload High Byte

Middle byte, Bits[15:8], of the 24-bit WDT reload value.

Table 60. Watchdog Timer Reload Low Byte Register (WDTL)

BITS	7	6	5	4	3	2	1	0
FIELD		WDTL						
RESET		00H						
R/W		R/W*						
ADDR	FF3H							
R/W* - Read returns the current WDT count value. Write sets the appropriate Reload Value.								

WDTL—WDT Reload Low

Least significant byte (LSB), Bits[7:0], of the 24-bit WDT reload value.

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Driver Enable is an active High signal that envelopes the entire transmitted data frame including parity and Stop bits as displayed in Figure 14. The Driver Enable signal asserts when a byte is written to the UART Transmit Data register. The Driver Enable signal asserts at least one UART bit period and no greater than two UART bit periods before the Start bit is transmitted. This allows a setup time to enable the transceiver. The Driver Enable signal deasserts one system clock period after the final Stop bit is transmitted. This one system clock delay allows both time for data to clear the transceiver before disabling it, as well as the ability to determine if another character follows the current character. In the event of back to back characters (new data must be written to the Transmit Data Register before the previous character is completely transmitted) the DE signal is not deasserted between characters. The DEPOL bit in the UART Control Register 1 sets the polarity of the Driver Enable signal.



Figure 14. UART Driver Enable Signal Timing (shown with 1 Stop Bit and Parity)

The Driver Enable to Start bit setup time is calculated as follows:

$$\left(\frac{1}{\text{Baud Rate (Hz)}}\right) \le \text{DE to Start Bit Setup Time (s)} \le \left(\frac{2}{\text{Baud Rate (Hz)}}\right)$$

UART Interrupts

The UART features separate interrupts for the transmitter and the receiver. In addition, when the UART primary functionality is disabled, the Baud Rate Generator can also function as a basic timer with interrupt capability.

Transmitter Interrupts

The transmitter generates a single interrupt when the Transmit Data Register Empty bit (TDRE) is set to 1. This indicates that the transmitter is ready to accept new data for transmission. The TDRE interrupt occurs after the Transmit shift register has shifted the first bit of data out. The Transmit Data register can now be written with the next character to

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(BRG[15:0]) that sets the data transmission rate (baud rate) of the UART. The UART data rate is calculated using the following equation:

UART Data Rate (bits/s) = $\frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Baud Rate Divisor Value}}$

When the UART is disabled, the Baud Rate Generator functions as a basic 16-bit timer with interrupt on time-out. Follow the steps below to configure the Baud Rate Generator as a timer with interrupt on time-out:

- 1. Disable the UART by clearing the REN and TEN bits in the UART Control 0 register to 0.
- 2. Load the acceptable 16-bit count value into the UART Baud Rate High and Low Byte registers.
- 3. Enable the Baud Rate Generator timer function and associated interrupt by setting the BRGCTL bit in the UART Control 1 register to 1.

When configured as a general purpose timer, the interrupt interval is calculated using the following equation:

Interrupt Interval(s) = System Clock Period (s) \times BRG[15:0]

UART Control Register Definitions

The UART control registers support the UART and the associated Infrared Encoder/ Decoders. For more information on infrared operation, see Infrared Encoder/Decoder on page 117.

UART Control 0 and Control 1 Registers

The UART Control 0 (UxCTL0) and Control 1 (UxCTL1) registers (Table 61 and Table 62) configure the properties of the UART's transmit and receive operations. The UART Control registers must not be written while the UART is enabled.

BITS	7	6	5	4	3	2	1	0
FIELD	TEN	REN	CTSE	PEN	PSEL	SBRK	STOP	LBEN
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR				F4	2H			

Table 61. UART Control 0 Register (U0CTL0)

TEN—Transmit Enable

This bit enables or disables the transmitter. The enable is also controlled by the $\overline{\text{CTS}}$ signal



MPMD[1:0]—MULTIPROCESSOR Mode

If MULTIPROCESSOR (9-bit) mode is enabled,

00 = The UART generates an interrupt request on all received bytes (data and address).

01 = The UART generates an interrupt request only on received address bytes.

10 = The UART generates an interrupt request when a received address byte matches the value stored in the Address Compare Register and on all successive data bytes until an address mismatch occurs.

11 = The UART generates an interrupt request on all received data bytes for which the most recent address byte matched the value in the Address Compare Register.

MPEN—MULTIPROCESSOR (9-bit) Enable

This bit is used to enable MULTIPROCESSOR (9-bit) mode.

0 = Disable MULTIPROCESSOR (9-bit) mode.

1 = Enable MULTIPROCESSOR (9-bit) mode.

MPBT—Multiprocessor Bit Transmit

This bit is applicable only when MULTIPROCESSOR (9-bit) mode is enabled. The 9th bit is used by the receiving device to determine if the data byte contains address or data information.

0 = Send a 0 in the multiprocessor bit location of the data stream (data byte).

1 = Send a 1 in the multiprocessor bit location of the data stream (address byte).

DEPOL—Driver Enable Polarity

0 = DE signal is Active High.

1 = DE signal is Active Low.

BRGCTL—Baud Rate Control

This bit causes an alternate UART behavior depending on the value of the REN bit in the UART Control 0 Register.

When the UART receiver is **not** enabled (REN=0), this bit determines whether the Baud Rate Generator issues interrupts.

0 = Reads from the Baud Rate High and Low Byte registers return the BRG Reload Value 1 = The Baud Rate Generator generates a receive interrupt when it counts down to 0. Reads from the Baud Rate High and Low Byte registers return the current BRG count value.

When the UART receiver is enabled (REN=1), this bit allows reads from the Baud Rate Registers to return the BRG count value instead of the Reload Value.

0 = Reads from the Baud Rate High and Low Byte registers return the BRG Reload Value. 1 = Reads from the Baud Rate High and Low Byte registers return the current BRG count value. Unlike the Timers, there is no mechanism to latch the Low Byte when the High Byte is read.

RDAIRQ—Receive Data Interrupt Enable

0 = Received data and receiver errors generates an interrupt request to the Interrupt Controller.

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Option Bit Types

User Option Bits

The user option bits are contained in the first two bytes of program memory. User access to these bits has been provided because these locations contain application-specific device configurations. The information contained here is lost when page 0 of the program memory is erased.

Trim Option Bits

The trim option bits are contained in the information page of the Flash memory. These bits are factory programmed values required to optimize the operation of onboard analog circuitry and cannot be permanently altered. Program Memory may be erased without endangering these values. It is possible to alter working values of these bits by accessing the Trim Bit Address and Data Registers, but these working values are lost after a power loss or any other reset event.

There are 32 bytes of trim data. To modify one of these values the user code must first write a value between 00H and 1FH into the Trim Bit Address Register. The next write to the Trim Bit Data register changes the working value of the target trim data byte.

Reading the trim data requires the user code to write a value between 00H and 1FH into the Trim Bit Address Register. The next read from the Trim Bit Data register returns the working value of the target trim data byte.

The trim address range is from information address 20-3F only. The remainder of the information page is not accessible through the trim bit address and data registers.

Calibration Option Bits

The calibration option bits are also contained in the information page. These bits are factory programmed values intended for use in software correcting the device's analog performance. To read these values, the user code must employ the LDC instruction to access the information area of the address space as defined in See Flash Information Area on page 17.

Serialization Bits

As an optional feature, Zilog[®] is able to provide factory-programmed serialization. For serialized products, the individual devices are programmed with unique serial numbers. These serial numbers are binary values, four bytes in length. The numbers increase in size with each device, but gaps in the serial sequence may exist.

These serial numbers are stored in the Flash information page (see Reading the Flash Information Page on page 155 and Serialization Data on page 165 for more details) and are unaffected by mass erasure of the device's Flash memory.

Note:

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The Auto-Baud Detector/Generator is clocked by the system clock. The minimum baud rate is the system clock frequency divided by 512. For optimal operation with asynchronous datastreams, the maximum recommended baud rate is the system clock frequency divided by 8. The maximum possible baud rate for asynchronous datastreams is the system clock frequency divided by 4, but this theoretical maximum is possible only for low noise designs with clean signals. Table 105 lists minimum and recommended maximum baud rates for sample crystal frequencies.

System Clock Frequency (MHz)	Recommended Maximum Baud Rate (Kbps)	Recommended Standard PC Baud Rate (bps)	Minimum Baud Rate (Kbps)
20.0	2500.0	1,843,200	39
1.0	125.0	115,200	1.95
0.032768 (32 kHz)	4.096	2,400	0.064

Table 105. OCD Baud-Rate Limits

If the OCD receives a Serial Break (nine or more continuous bits Low) the Auto-Baud Detector/Generator resets. Reconfigure the Auto-Baud Detector/Generator by sending 80H.

OCD Serial Errors

The On-Chip Debugger can detect any of the following error conditions on the DBG pin:

- Serial Break (a minimum of nine continuous bits Low)
- Framing Error (received Stop bit is Low)
- Transmit Collision (OCD and host simultaneous transmission detected by the OCD)

When the OCD detects one of these errors, it aborts any command currently in progress, transmits a four character long Serial Break back to the host, and resets the Auto-Baud Detector/Generator. A Framing Error or Transmit Collision may be caused by the host sending a Serial Break to the OCD. Because of the open-drain nature of the interface, returning a Serial Break break back to the host only extends the length of the Serial Break if the host releases the Serial Break early.

The host transmits a Serial Break on the DBG pin when first connecting to the Z8 Encore! XP F082A Series devices or when recovering from an error. A Serial Break from the host resets the Auto-Baud Generator/Detector but does not reset the OCD Control register. A Serial Break leaves the device in DEBUG mode if that is the current mode. The OCD is held in Reset until the end of the Serial Break when the DBG pin returns



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Figure 29 displays the typical (3.3 V and 25 °C) oscillator frequency as a function of the capacitor (C in pF) employed in the RC network assuming a 45 K Ω external resistor. For very small values of C, the parasitic capacitance of the oscillator XIN pin and the printed circuit board must be included in the estimation of the oscillator frequency.

It is possible to operate the RC oscillator using only the parasitic capacitance of the package and printed circuit board. To minimize sensitivity to external parasitics, external capacitance values in excess of 20 pF are recommended.



Figure 29. Typical RC Oscillator Frequency as a Function of the External Capacitance with a 45 k Ω Resistor

Caution:

When using the external RC oscillator mode, the oscillator can stop oscillating if the power supply drops below 2.7 V, but before the power supply drops to the Voltage Brownout threshold. The oscillator resumes oscillation when the supply voltage exceeds 2.7 V.

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Table 114. Notational Shorthand

Notation	Description	Operand	Range
b	Bit	b	b represents a value from 0 to 7 (000B to 111B).
CC	Condition Code	—	Refer to Condition Codes section in the <i>eZ8 CPU Core User Manual (UM0128)</i> .
DA	Direct Address	Addrs	Addrs. represents a number in the range of 0000H to FFFFH
ER	Extended Addressing Register	Reg	Reg. represents a number in the range of 000H to FFFH
IM	Immediate Data	#Data	Data is a number between 00H to FFH
lr	Indirect Working Register	@Rn	n = 0–15
IR	Indirect Register	@Reg	Reg. represents a number in the range of 00H to FFH
Irr	Indirect Working Register Pair	@RRp	p = 0, 2, 4, 6, 8, 10, 12, or 14
IRR	Indirect Register Pair	@Reg	Reg. represents an even number in the range 00H to FEH
р	Polarity	р	Polarity is a single bit binary value of either 0B or 1B.
r	Working Register	Rn	n = 0 – 15
R	Register	Reg	Reg. represents a number in the range of 00H to FFH
RA	Relative Address	Х	X represents an index in the range of +127 to – 128 which is an offset relative to the address of the next instruction
rr	Working Register Pair	RRp	p = 0, 2, 4, 6, 8, 10, 12, or 14
RR	Register Pair	Reg	Reg. represents an even number in the range of 00H to FEH
Vector	Vector Address	Vector	Vector represents a number in the range of 00H to FFH
X	Indexed	#Index	The register or register pair to be indexed is offset by the signed Index value (#Index) in a +127 to -128 range.

Table 115 lists additional symbols that are used throughout the Instruction Summary and Instruction Set Description sections.



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Table 115. Additional Symbols

Symbol	Definition
dst	Destination Operand
SrC	Source Operand
@	Indirect Address Prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flags Register
RP	Register Pointer
#	Immediate Operand Prefix
В	Binary Number Suffix
%	Hexadecimal Number Prefix
Н	Hexadecimal Number Suffix

Assignment of a value is indicated by an arrow. For example,

 $dst \leftarrow dst + src$

indicates the source data is added to the destination data and the result is stored in the destination location.

eZ8 CPU Instruction Classes

eZ8 CPU instructions can be divided functionally into the following groups:

- Arithmetic
- Bit Manipulation
- Block Transfer
- CPU Control
- Load
- Logical
- Program Control
- Rotate and Shift

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Assembly Mnemonic	Symbolic Operation	Addres	Address Mode		Flags					Fetch	Instr.	
		dst	src	(Hex)	С	Ζ	S	۷	D	Н	Cycles	Cycles
HALT	Halt Mode			7F	_	_	_	_	-	_	1	2
INC dst	$dst \gets dst + 1$	R		20	-	*	*	_	-	_	2	2
		IR		21	-						2	3
		r		0E-FE	-						1	2
INCW dst	$dst \gets dst + 1$	RR		A0	-	*	*	*	-	-	2	5
		IRR		A1	-						2	6
IRET	$\begin{array}{l} FLAGS \leftarrow @SP \\ SP \leftarrow SP + 1 \\ PC \leftarrow @SP \\ SP \leftarrow SP + 2 \\ IRQCTL[7] \leftarrow 1 \end{array}$			BF	*	*	*	*	*	*	1	5
JP dst	$PC \gets dst$	DA		8D	-	_	-	-	-	-	3	2
		IRR		C4	-						2	3
JP cc, dst	if cc is true PC \leftarrow dst	DA		0D-FD	_	_	-	-	-	-	3	2
JR dst	$PC \gets PC + X$	DA		8B	_	_	_	_	-	_	2	2
JR cc, dst	if cc is true PC \leftarrow PC + X	DA		0B-FB	-	-	-	_	-	-	2	2
LD dst, rc	$dst \gets src$	r	IM	0C-FC	-	-	-	-	-	-	2	2
		r	X(r)	C7	-						3	3
		X(r)	r	D7	-						3	4
		r	lr	E3	-						2	3
		R	R	E4	-						3	2
		R	IR	E5	-						3	4
		R	IM	E6	-						3	2
		IR	IM	E7	-						3	3
		lr	r	F3	-						2	3
		IR	R	F5	-						3	3
Flags Notation:	* = Value is a functior – = Unaffected X = Undefined	of the result	of the o	peration.	0 = 1 =	Re Se	set t to	to (1)			

Table 124. eZ8 CPU Instruction Summary (Continued)

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Figure 33 displays the typical current consumption while operating with all peripherals disabled, at 30 °C, versus the system clock frequency.



Figure 33. Typical Active Mode I_{DD} Versus System Clock Frequency



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General Purpose I/O Port Output Timing

Figure 35 and Table 140 provide timing information for GPIO Port pins.



Figure 35. GPIO Port Output Timing

			Delay (ns)				
Parameter	Abbreviation	-	Minimum	Maximum			
GPIO Port p	bins						
T ₁	XIN Rise to Port Output Valid Delay		_	15			
T ₂	XIN Rise to Port Output Hold Time		2	_			

Table 140. GPIO Port Output Timing

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Figure 43 displays the 20-pin Small Outline Integrated Circuit Package (SOIC) available for the Z8 Encore! XP F082A Series devices.

Figure 43. 20-Pin Small Outline Integrated Circuit Package (SOIC)