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Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f081ahj020sc

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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Register Map

Table 7 provides the address map for the Register File of the Z8 Encore! XP[®] F082A Series devices. Not all devices and package styles in the Z8 Encore! XP F082A Series support the ADC, or all of the GPIO Ports. Consider registers for unimplemented peripherals as Reserved.

Table 7. Register File Address Map

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
General-Purpo	se RAM			
Z8F082A/Z8F08	31A Devices			
000–3FF	General-Purpose Register File RAM		XX	
400–EFF	Reserved	_	XX	
Z8F042A/Z8F04	IA Devices			
000–3FF	General-Purpose Register File RAM		XX	
400–EFF	Reserved	—	XX	
Z8F022A/Z8F02	21A Devices			
000–1FF	General-Purpose Register File RAM	_	XX	
200–EFF	Reserved	_	XX	
Z8F012A/Z8F0	I1A Devices			
000–0FF	General-Purpose Register File RAM	_	XX	
100–EFF	Reserved	—	XX	
Timer 0				
F00	Timer 0 High Byte	ТОН	00	87
F01	Timer 0 Low Byte	TOL	01	87
F02	Timer 0 Reload High Byte	TORH	FF	88
F03	Timer 0 Reload Low Byte	TORL	FF	88
F04	Timer 0 PWM High Byte	T0PWMH	00	88
F05	Timer 0 PWM Low Byte	TOPWML	00	89
F06	Timer 0 Control 0	T0CTL0	00	83
F07	Timer 0 Control 1	T0CTL1	00	84
Timer 1				
F08	Timer 1 High Byte	T1H	00	87
F09	Timer 1 Low Byte	T1L	01	87
F0A	Timer 1 Reload High Byte	T1RH	FF	88
XX=Undefined				

vector address. Following Stop Mode Recovery, the STOP bit in the Reset Status (RSTSTAT) Register is set to 1. Table 10 lists the Stop Mode Recovery sources and resulting actions. The text following provides more detailed information about each of the Stop Mode Recovery sources.

Operating Mode	Stop Mode Recovery Source	Action
STOP mode	Watchdog Timer time-out when configured for Reset	Stop Mode Recovery
	Watchdog Timer time-out when configured for interrupt	Stop Mode Recovery followed by interrupt (if interrupts are enabled)
	Data transition on any GPIO Port pin enabled as a Stop Mode Recovery source	Stop Mode Recovery
	Assertion of external RESET Pin	System Reset
	Debug Pin driven Low	System Reset

Table 10. Stop Mode Recovery Sources and Resulting Action

Stop Mode Recovery Using Watchdog Timer Time-Out

If the Watchdog Timer times out during STOP mode, the device undergoes a Stop Mode Recovery sequence. In the Reset Status (RSTSTAT) register, the WDT and STOP bits are set to 1. If the Watchdog Timer is configured to generate an interrupt upon time-out and the Z8 Encore! XP F082A Series device is configured to respond to interrupts, the eZ8 CPU services the Watchdog Timer interrupt request following the normal Stop Mode Recovery sequence.

Stop Mode Recovery Using a GPIO Port Pin Transition

Each of the GPIO Port pins may be configured as a Stop Mode Recovery input source. On any GPIO pin enabled as a Stop Mode Recovery source, a change in the input pin value (from High to Low or from Low to High) initiates Stop Mode Recovery.

Note: The SMR pulses shorter than specified does not trigger a recovery (see Table 131 on page 229). When this happens, the STOP bit in the Reset Status (RSTSTAT) register is set to 1.

Caution: In STOP mode, the GPIO Port Input Data registers (PxIN) are disabled. The Port Input Data registers record the Port transition only if the signal stays on the Port pin through the end of the Stop Mode Recovery delay. As a result, short pulses on the Port pin can



LEDEN[7:0]—LED Drive Enable These bits determine which Port C pins are connected to an internal current sink. 0 = Tristate the Port C pin. 1= Enable controlled current sink on the Port C pin.

LED Drive Level High Register

The LED Drive Level registers contain two control bits for each Port C pin (Table 30). These two bits select between four programmable drive levels. Each pin is individually programmable.

Table 30. LED Drive Level High Register (LEDLVLH)

BITS	7	6	5	4	3	2	1	0		
FIELD		LEDLVLH[7:0]								
RESET	0	0	0	0	0	0	0	0		
R/W	R/W	R/W R/W R/W R/W R/W R/W R/W								
ADDR				F8	3H					

LEDLVLH[7:0]—LED Level High Bit

{LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin.

00 = 3 mA 01= 7 mA 10= 13 mA 11= 20 mA

LED Drive Level Low Register

The LED Drive Level registers contain two control bits for each Port C pin (Table 31). These two bits select between four programmable drive levels. Each pin is individually programmable.



IRQ2 Enable High and Low Bit Registers

Table 42 describes the priority control for IRQ2. The IRQ2 Enable High and Low Bit registers (Table 43 and Table 44) form a priority encoded enabling for interrupts in the Interrupt Request 2 register.

IRQ2ENH[x]	IRQ2ENL[x]	Priority	Description
0	0	Disabled	Disabled
0	1	Level 1	Low
1	0	Level 2	Medium
1	1	Level 3	High

Table 42. IRQ2 Enable and Priority Encoding

where x indicates the register bits from 0–7.

Table 43. IRQ2 Enable High Bit Register (IRQ2ENH)

BITS	7	6	5	4	3	2	1	0
FIELD		Rese	erved		C3ENH	C2ENH	C1ENH	C0ENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W R/W R/W R/W R/W R/W R/W						R/W	R/W
ADDR				FC	7H			

Reserved—Must be 0.

C3ENH—Port C3 Interrupt Request Enable High Bit C2ENH—Port C2 Interrupt Request Enable High Bit C1ENH—Port C1 Interrupt Request Enable High Bit C0ENH—Port C0 Interrupt Request Enable High Bit

Table 44. IRQ2 Enable Low Bit Register (IRQ2ENL)

BITS	7	6	5	4	3	2	1	0
FIELD		Rese	erved		C3ENL	C2ENL	C1ENL	C0ENL
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR				FC	:8H			



110 = 64 cycles delay 111 = 128 cycles delay

INPCAP—Input Capture Event

This bit indicates if the most recent timer interrupt is caused by a Timer Input Capture Event.

0 = Previous timer interrupt is not a result of Timer Input Capture Event

1 = Previous timer interrupt is a result of Timer Input Capture Event

Timer 0–1 Control Register 1

The Timer 0–1 Control (TxCTL1) registers enable/disable the timers, set the prescaler value, and determine the timer operating mode (Table 49).

Table 49. Timer 0–1 Control Register 1 (TxCTL1)

BITS	7	6	5	4	3	2	1	0
FIELD	TEN	TPOL		PRES			TMODE	
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR				F07H,	F0FH			

TEN-Timer Enable

0 = Timer is disabled.

1 = Timer enabled to count.

TPOL—Timer Input/Output Polarity

Operation of this bit is a function of the current operating mode of the timer.

ONE-SHOT mode

When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

CONTINUOUS mode

When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

COUNTER mode

If the timer is enabled the Timer Output signal is complemented after timer reload.

0 = Count occurs on the rising edge of the Timer Input signal.

1 = Count occurs on the falling edge of the Timer Input signal.



1000 = PWM DUAL OUTPUT mode 1001 = CAPTURE RESTART mode 1010 = COMPARATOR COUNTER mode

Timer 0–1 High and Low Byte Registers

The Timer 0–1 High and Low Byte (TxH and TxL) registers (Table 50 and Table 51) contain the current 16-bit timer count value. When the timer is enabled, a read from TxH causes the value in TxL to be stored in a temporary holding register. A read from TxL always returns this temporary register when the timers are enabled. When the timer is disabled, reads from TxL read the register directly.

Writing to the Timer High and Low Byte registers while the timer is enabled is not recommended. There are no temporary holding registers available for write operations, so simultaneous 16-bit writes are not possible. If either the Timer High or Low Byte registers are written during counting, the 8-bit written value is placed in the counter (High or Low Byte) at the next clock edge. The counter continues counting from the new value.

BITS	7	6	5	4	3	2	1	0		
FIELD	TH									
RESET	0	0	0	0	0	0	0	0		
R/W	R/W	R/W R/W R/W R/W R/W R/W R/W								
ADDR				F00H,	F08H					

Table 50. Timer 0–1 High Byte Register (TxH)

Table 51. Timer 0–1 Low Byte Register (TxL)

BITS	7	6	5	4	3	2	1	0				
FIELD		TL										
RESET	0	0	0	0	0	0	0	1				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
ADDR				F01H,	F01H, F09H							

TH and TL—Timer High and Low Bytes

These 2 bytes, {TH[7:0], TL[7:0]}, contain the current 16-bit timer count value.

Timer Reload High and Low Byte Registers

The Timer 0–1 Reload High and Low Byte (TxRH and TxRL) registers (Table 52 and Table 53) store a 16-bit reload value, {TRH[7:0], TRL[7:0]}. Values written to the Timer Reload High Byte register are stored in a temporary holding register. When a write to the

send. This action provides 7 bit periods of latency to load the Transmit Data register before the Transmit shift register completes shifting the current character. Writing to the UART Transmit Data register clears the TDRE bit to 0.

Receiver Interrupts

The receiver generates an interrupt when any of the following occurs:

- A data byte is received and is available in the UART Receive Data register. This interrupt can be disabled independently of the other receiver interrupt sources. The received data interrupt occurs after the receive character has been received and placed in the Receive Data register. To avoid an overrun error, software must respond to this received data available condition before the next character is completely received.
- · |

Note: In MULTIPROCESSOR mode (MPEN = 1), the receive data interrupts are dependent on the multiprocessor configuration and the most recent address byte.

- A break is received.
- An overrun is detected.
- A data framing error is detected.

UART Overrun Errors

When an overrun error condition occurs the UART prevents overwriting of the valid data currently in the Receive Data register. The Break Detect and Overrun status bits are not displayed until after the valid data has been read.

After the valid data has been read, the UART Status 0 register is updated to indicate the overrun condition (and Break Detect, if applicable). The RDA bit is set to 1 to indicate that the Receive Data register contains a data byte. However, because the overrun error occurred, this byte may not contain valid data and must be ignored. The BRKD bit indicates if the overrun was caused by a break condition on the line. After reading the status byte indicating an overrun error, the Receive Data register must be read again to clear the error bits is the UART Status 0 register. Updates to the Receive Data register occur only when the next data word is received.

UART Data and Error Handling Procedure

Figure 15 displays the recommended procedure for use in UART receiver interrupt service routines.



Figure 15. UART Receiver Interrupt Service Routine Flow

Baud Rate Generator Interrupts

If the baud rate generator (BRG) interrupt enable is set, the UART Receiver interrupt asserts when the UART Baud Rate Generator reloads. This condition allows the Baud Rate Generator to function as an additional counter if the UART functionality is not employed.

UART Baud Rate Generator

The UART Baud Rate Generator creates a lower frequency baud rate clock for data transmission. The input to the Baud Rate Generator is the system clock. The UART Baud Rate High and Low Byte registers combine to create a 16-bit baud rate divisor value

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UART Address Compare Register

The UART Address Compare (UxADDR) register stores the multi-node network address of the UART (see Table 67). When the MPMD[1] bit of UART Control Register 0 is set, all incoming address bytes are compared to the value stored in the Address Compare register. Receive interrupts and RDA assertions only occur in the event of a match.

Table 67. UART Address Compare Register (U0ADDR)

BITS	7	6	5	4	3	2	1	0	
FIELD	COMP_ADDR								
RESET	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ADDR				F4	5H				

COMP_ADDR—Compare Address

This 8-bit value is compared to incoming address bytes.

UART Baud Rate High and Low Byte Registers

The UART Baud Rate High (UxBRH) and Low Byte (UxBRL) registers (Table 68 and Table 69) combine to create a 16-bit baud rate divisor value (BRG[15:0]) that sets the data transmission rate (baud rate) of the UART.

Table 68. UART Baud Rate High Byte Register (U0BRH)

BITS	7	6	5	4	3	2	1	0						
FIELD	BRH													
RESET	1 1		1	1	1	1	1	1						
R/W	R/W R/W R/W R/W R/W R/W R/W													
ADDR	F46H													

Table 69. UART Baud Rate Low Byte Register (U0BRL)

BITS	7	6	5	4	3	2	1	0						
FIELD	BRL													
RESET	1	1 1		1 1		1	1	1						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W							
ADDR	F47H													

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Caution: Although the ADC can be used without the gain and offset compensation, it does exhibit non-unity gain. Designing the ADC with sub-unity gain reduces noise across the ADC range but requires the ADC results to be scaled by a factor of 8/7.

ADC Compensation Details

High efficiency assembly code that performs this compensation is available for download on <u>www.zilog.com</u>. The following is a bit-specific description of the ADC compensation process used by this code.

The following data bit definitions are used:

0-9, a-f = bit indices in hexadecimal

s = sign bit

v = overflow bit

- = unused

Input Data

			MS	SΒ								LS	В				
ន	b	a	9	8	7	6	5	4	3	2	1	0	-	-	v	(ADC)	ADC Output Word; if $v = 1$, the data is invalid
								S	6	5	4	3	2	1	0		Offset Correction Byte
s	s	s	s	s	7	6	5	4	3	2	1	0	0	0	0	(Offset)	Offset Byte shifted to align
						-						-	-	-	-		with ADC data
ទ	е	d	С	b	a	9	8	7	6	5	4	3	2	1	0	(Gain)	Gain Correction Word
								<u></u>								1	
]	
L								Į								J	
																7	

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ANAIN[3:0]—Analog Input Select

These bits select the analog input for conversion. Not all Port pins in this list are available in all packages for the Z8 Encore! XP[®] F082A Series. For information on port pins available with each package style, see Pin Description on page 9. Do not enable unavailable analog inputs. Usage of these bits changes depending on the buffer mode selected in ADC Control/Status Register 1.

For the reserved values, all input switches are disabled to avoid leakage or other undesirable operation. ADC samples taken with reserved bit settings are undefined.

SINGLE-ENDED:

- 0000 = ANA0 (transimpedance amp output when enabled)
- 0001 = ANA1 (transimpedance amp inverting input)
- 0010 = ANA2 (transimpedance amp non-inverting input)
- 0011 = ANA3
- 0100 = ANA4
- 0101 = ANA5
- 0110 = ANA6
- 0111 = ANA7
- 1000 = Reserved
- 1001 = Reserved
- 1010 = Reserved
- 1011 = Reserved
- 1100 = Hold transimpedance input nodes (ANA1 and ANA2) to ground.
- 1101 = Reserved
- 1110 = Temperature Sensor.
- 1111 = Reserved.

DIFFERENTIAL (non-inverting input and inverting input respectively):

- 0000 = ANA0 and ANA1 0001 = ANA2 and ANA3 0010 = ANA4 and ANA5 0011 = ANA1 and ANA0 0100 = ANA3 and ANA2 0101 = ANA5 and ANA4 0110 = ANA6 and ANA5 0111 = ANA0 and ANA5 1011 = ANA0 and ANA3 1001 = ANA0 and ANA3 1001 = ANA0 and ANA4 1010 = ANA0 and ANA5 1011 = Reserved 1100 = Reserved 1101 = Reserved1101 = Reserved
- 1111 = Manual Offset Calibration Mode

BITS	7	6	5 4		3	2	1	0					
FIELD	INFO_EN	PAGE											
RESET	0	0	0	0 0		0	0	0					
R/W	R/W	R/W R/W R/W R/W R/W											
ADDR	FF9H												

Table 80. Flash Page Select Register (FPS)

INFO_EN—Information Area Enable

0 = Information Area us not selected.

1 = Information Area is selected. The Information Area is mapped into the Program Memory address space at addresses FE00H through FFFFH.

PAGE—Page Select

This 7-bit field identifies the Flash memory page for Page Erase and page unlocking. Program Memory Address[15:9] = PAGE[6:0]. For the Z8F08xx devices, the upper 3 bits must be zero. For the Z8F04xx devices, the upper 4 bits must be zero. For Z8F02xx devices, the upper 5 bits must always be 0. For the Z8F01xx devices, the upper 6 bits must always be 0.

Flash Sector Protect Register

The Flash Sector Protect (FPROT) register is shared with the Flash Page Select Register. When the Flash Control Register is written with 73H followed by 5EH, the next write to this address targets the Flash Sector Protect Register. In all other cases, it targets the Flash Page Select Register.

This register selects one of the 8 available Flash memory sectors to be protected. The reset state of each Sector Protect bit is an unprotected state. After a sector is protected by setting its corresponding register bit, it cannot be unprotected (the register bit cannot be cleared) without powering down the device.

R/W

R/W

R/W

BITS	7	6	5	4	3	2	1
FIELD	SPROT7	SPROT6	SPROT5	SPROT4	SPROT3	SPROT2	SPROT1
RESET	0	0	0	0	0	0	0

R/W

FF9H

R/W

Table 81. Flash Sector Protect Register (FPROT)

R/W

R/W

ADDR

R/W

0

SPROT0

0

R/W

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Option Bit Types

User Option Bits

The user option bits are contained in the first two bytes of program memory. User access to these bits has been provided because these locations contain application-specific device configurations. The information contained here is lost when page 0 of the program memory is erased.

Trim Option Bits

The trim option bits are contained in the information page of the Flash memory. These bits are factory programmed values required to optimize the operation of onboard analog circuitry and cannot be permanently altered. Program Memory may be erased without endangering these values. It is possible to alter working values of these bits by accessing the Trim Bit Address and Data Registers, but these working values are lost after a power loss or any other reset event.

There are 32 bytes of trim data. To modify one of these values the user code must first write a value between 00H and 1FH into the Trim Bit Address Register. The next write to the Trim Bit Data register changes the working value of the target trim data byte.

Reading the trim data requires the user code to write a value between 00H and 1FH into the Trim Bit Address Register. The next read from the Trim Bit Data register returns the working value of the target trim data byte.

The trim address range is from information address 20-3F only. The remainder of the information page is not accessible through the trim bit address and data registers.

Calibration Option Bits

The calibration option bits are also contained in the information page. These bits are factory programmed values intended for use in software correcting the device's analog performance. To read these values, the user code must employ the LDC instruction to access the information area of the address space as defined in See Flash Information Area on page 17.

Serialization Bits

As an optional feature, Zilog[®] is able to provide factory-programmed serialization. For serialized products, the individual devices are programmed with unique serial numbers. These serial numbers are binary values, four bytes in length. The numbers increase in size with each device, but gaps in the serial sequence may exist.

These serial numbers are stored in the Flash information page (see Reading the Flash Information Page on page 155 and Serialization Data on page 165 for more details) and are unaffected by mass erasure of the device's Flash memory.

Note:



High. Because of the open-drain nature of the DBG pin, the host can send a Serial Break to the OCD even if the OCD is transmitting a character.

OCD Unlock Sequence (8-Pin Devices Only)

Because of pin-sharing on the 8-pin device, an unlock sequence must be performed to access the DBG pin. If this sequence is not completed during a system reset, then the PA0/DBG pin functions only as a GPIO pin.

The following sequence unlocks the DBG pin:

- 1. Hold PA2/RESET Low.
- 2. Wait 5ms for the internal reset sequence to complete.
- 3. Send the following bytes serially to the debug pin:

```
DBG \leftarrow 80H (autobaud)
DBG \leftarrow EBH
DBG \leftarrow 5AH
DBG \leftarrow 70H
DBG \leftarrow CDH (32-bit unlock key)
```

4. Release PA2/RESET. The PA0/DBG pin is now identical in function to that of the DBG pin on the 20-/28-pin device. To enter DEBUG mode, re-autobaud and write 80H to the OCD control register (see On-Chip Debugger Commands on page 179).

Caution: Between Step 3 and Step 4, there is an interval during which the 8-pin device is neither in RESET nor DEBUG mode. If a device has been erased or has not yet been programmed, all program memory bytes contain FFH. The CPU interprets this as an illegal instruction, so some irregular behavior can occur before entering DEBUG mode, and the register values after entering DEBUG mode differs from their specified reset values. However, none of these irregularities prevent programming the Flash memory. Before beginning system debug, it is recommended that some legal code be programmed into the 8-pin device, and that a RESET occurs.

Breakpoints

Execution Breakpoints are generated using the BRK instruction (opcode 00H). When the eZ8 CPU decodes a BRK instruction, it signals the On-Chip Debugger. If Breakpoints are enabled, the OCD enters DEBUG mode and idles the eZ8 CPU. If Breakpoints are not enabled, the OCD ignores the BRK signal and the BRK instruction operates as an NOP instruction.

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Figure 29 displays the typical (3.3 V and 25 °C) oscillator frequency as a function of the capacitor (C in pF) employed in the RC network assuming a 45 K Ω external resistor. For very small values of C, the parasitic capacitance of the oscillator XIN pin and the printed circuit board must be included in the estimation of the oscillator frequency.

It is possible to operate the RC oscillator using only the parasitic capacitance of the package and printed circuit board. To minimize sensitivity to external parasitics, external capacitance values in excess of 20 pF are recommended.



Figure 29. Typical RC Oscillator Frequency as a Function of the External Capacitance with a 45 k Ω Resistor

Caution:

When using the external RC oscillator mode, the oscillator can stop oscillating if the power supply drops below 2.7 V, but before the power supply drops to the Voltage Brownout threshold. The oscillator resumes oscillation when the supply voltage exceeds 2.7 V.

Internal Precision Oscillator

The internal precision oscillator (IPO) is designed for use without external components. You can either manually trim the oscillator for a non-standard frequency or use the automatic factory-trimmed version to achieve a 5.53 MHz frequency. IPO features include:

- On-chip RC oscillator that does not require external components
- Output frequency of either 5.53 MHz or 32.8 kHz (contains both a fast and a slow mode)
- Trimmed through Flash option bits with user override
- Elimination of crystals or ceramic resonators in applications where very high timing accuracy is not required

Operation

An 8-bit trimming register, incorporated into the design, compensates for absolute variation of oscillator frequency. Once trimmed the oscillator frequency is stable and does not require subsequent calibration. Trimming is performed during manufacturing and is not necessary for you to repeat unless a frequency other than 5.53 MHz (fast mode) or 32.8 kHz (slow mode) is required. This trimming is done at +30 °C and a supply voltage of 3.3 V, so accuracy of this operating point is optimal.

If not used, the IPO can be disabled by the Oscillator Control register (see Oscillator Control Register Definitions on page 190).

By default, the oscillator frequency is set by the factory trim value stored in the write-protected Flash information page. However, the user code can override these trim values as described in Trim Bit Address Space on page 158.

Select one of two frequencies for the oscillator: 5.53 MHz and 32.8 kHz, using the OSCSEL bits in the Oscillator Control on page 187.



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Ordering Information

Order the Z8 Encore! XP[®] F082A Series from Zilog[®], using the following part numbers. For more information on ordering, please consult your local Zilog sales office. The Zilog website (<u>www.zilog.com</u>) lists all regional offices and provides additional Z8 Encore! XP product information.

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP [®] F082/	A Serie	s with 8	KB Fla	ash, 1	0-Bit	Ana	log-t	o-Dig	ital C	onv	rerter
Standard Temperature: 0 °C to 70°C											
Z8F082APB020SC	8 KB	1 KB	0	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F082AQB020SC	8 KB	1 KB	0	6	14	2	4	1	1	1	QFN 8-pin package
Z8F082ASB020SC	8 KB	1 KB	0	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F082ASH020SC	8 KB	1 KB	0	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F082AHH020SC	8 KB	1 KB	0	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F082APH020SC	8 KB	1 KB	0	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F082ASJ020SC	8 KB	1 KB	0	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F082AHJ020SC	8 KB	1 KB	0	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F082APJ020SC	8 KB	1 KB	0	23	20	2	8	1	1	1	PDIP 28-pin package
Extended Temperatur	e: -40 °	C to 105	°C								
Z8F082APB020EC	8 KB	1 KB	0	6	14	2	4	1	1	1	PDIP 8-pin package
Z8F082AQB020EC	8 KB	1 KB	0	6	14	2	4	1	1	1	QFN 8-pin package
Z8F082ASB020EC	8 KB	1 KB	0	6	14	2	4	1	1	1	SOIC 8-pin package
Z8F082ASH020EC	8 KB	1 KB	0	17	20	2	7	1	1	1	SOIC 20-pin package
Z8F082AHH020EC	8 KB	1 KB	0	17	20	2	7	1	1	1	SSOP 20-pin package
Z8F082APH020EC	8 KB	1 KB	0	17	20	2	7	1	1	1	PDIP 20-pin package
Z8F082ASJ020EC	8 KB	1 KB	0	23	20	2	8	1	1	1	SOIC 28-pin package
Z8F082AHJ020EC	8 KB	1 KB	0	23	20	2	8	1	1	1	SSOP 28-pin package
Z8F082APJ020EC	8 KB	1 KB	0	23	20	2	8	1	1	1	PDIP 28-pin package
Replace C with G for Lead-Free Packaging											