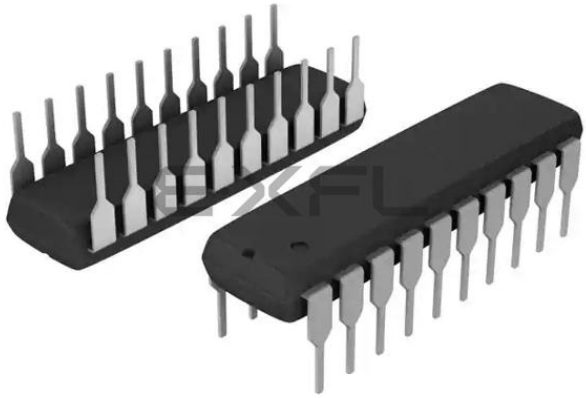


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f081aph020sc

Low-Power Operational Amplifier

The optional low-power operational amplifier (LPO) is a general-purpose amplifier primarily targeted for current sense applications. The LPO output may be routed internally to the ADC or externally to a pin.

Internal Precision Oscillator

The internal precision oscillator (IPO) is a trimmable clock source that requires no external components.

Temperature Sensor

The optional temperature sensor produces an analog output proportional to the device temperature. This signal can be sent to either the ADC or the analog comparator.

Analog Comparator

The analog comparator compares the signal at an input pin with either an internal programmable voltage reference or a second input pin. The comparator output can be used to drive either an output pin or to generate an interrupt.

External Crystal Oscillator

The crystal oscillator circuit provides highly accurate clock frequencies with the use of an external crystal, ceramic resonator or RC network.

Low Voltage Detector

The low voltage detector (LVD) is able to generate an interrupt when the supply voltage drops below a user-programmable level. The LVD is available on 8-pin devices only.

On-Chip Debugger

The Z8 Encore! XP® F082A Series products feature an integrated on-chip debugger (OCD) accessed via a single-pin interface. The OCD provides a rich-set of debugging capabilities, such as reading and writing registers, programming Flash memory, setting breakpoints, and executing code.

Table 3. Pin Characteristics (20- and 28-pin Devices) (Continued)

Symbol Mnemonic	Direction	Reset Direction	Active Low or Active High	Tristate Output	Internal Pull-up or Pull-down	Schmitt-Trigger Input	Open Drain Output	5 V Tolerance
PC[7:0]	I/O	I	N/A	Yes	Programmable Pull-up	Yes	Yes, Programmable	PC[7:3] unless pullups enabled
RESET/PD0	I/O	I/O (defaults to $\overline{\text{RESET}}$)	Low (in Reset mode)	Yes (PD0 only)	Programmable for PD0; always on for $\overline{\text{RESET}}$	Yes	Programmable for PD0; always on for $\overline{\text{RESET}}$	Yes, unless pullups enabled
VDD	N/A	N/A	N/A	N/A			N/A	N/A
VSS	N/A	N/A	N/A	N/A			N/A	N/A

Note: *PB6 and PB7 are available only in those devices without ADC.*

Table 4. Pin Characteristics (8-Pin Devices)

Symbol Mnemonic	Direction	Reset Direction	Active Low or Active High	Tristate Output	Internal Pull-up or Pull-down	Schmitt-Trigger Input	Open Drain Output	5 V Tolerance
PA0/DBG	I/O	I (but can change during reset if key sequence detected)	N/A	Yes	Programmable Pull-up	Yes	Yes, Programmable	Yes, unless pull-ups enabled
PA1	I/O	I	N/A	Yes	Programmable Pull-up	Yes	Yes, Programmable	Yes, unless pull-ups enabled
$\overline{\text{RESET}}$/PA2	I/O	I/O (defaults to $\overline{\text{RESET}}$)	Low (in Reset mode)	Yes	Programmable for PA2; always on for $\overline{\text{RESET}}$	Yes	Programmable for PA2; always on for $\overline{\text{RESET}}$	Yes, unless pull-ups enabled
PA[5:3]	I/O	I	N/A	Yes	Programmable Pull-up	Yes	Yes, Programmable	Yes, unless pull-ups enabled
V_{DD}	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
V_{SS}	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Table 14. Port Alternate Function Mapping (Non 8-Pin Parts) (Continued)

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port C	PC0	Reserved		AFS1[0]: 0
		ANA4/CINP/LED Drive	ADC or Comparator Input, or LED drive	AFS1[0]: 1
	PC1	Reserved		AFS1[1]: 0
		ANA5/CINN/ LED Drive	ADC or Comparator Input, or LED drive	AFS1[1]: 1
	PC2	Reserved		AFS1[2]: 0
		ANA6/LED/ VREF*	ADC Analog Input or LED Drive or ADC Voltage Reference	AFS1[2]: 1
	PC3	COUT	Comparator Output	AFS1[3]: 0
		LED	LED drive	AFS1[3]: 1
	PC4	Reserved		AFS1[4]: 0
		LED	LED Drive	AFS1[4]: 1
	PC5	Reserved		AFS1[5]: 0
		LED	LED Drive	AFS1[5]: 1
	PC6	Reserved		AFS1[6]: 0
		LED	LED Drive	AFS1[6]: 1
	PC7	Reserved		AFS1[7]: 0
		LED	LED Drive	AFS1[7]: 1

Note: Because there are at most two choices of alternate function for any pin of Port C, the Alternate Function Set register AFS2 is not used to select the function. Also, alternate function selection as described in Port A–D Alternate Function Sub-Registers on page 47 must also be enabled.
*VREF is available on PC2 in 20-pin parts only.

PAFS1[7:0]—Port Alternate Function Set 1
0 = Port Alternate Function selected as defined in Table 14 and Table 15 on page 44.
1 = Port Alternate Function selected as defined in Table 14 and Table 15 on page 44.

Port A–D Alternate Function Set 2 Sub-Registers

The Port A–D Alternate Function Set 2 sub-register (Table 26) is accessed through the Port A–D Control register by writing 08H to the Port A–D Address register. The Alternate Function Set 2 sub-registers selects the alternate function available at a port pin. Alternate Functions selected by setting or clearing bits of this register is defined in Table 15.

Note: *Alternate function selection on port pins must also be enabled as described in* Port A–D Alternate Function Sub-Registers *on page 47.*

Table 26. Port A–D Alternate Function Set 2 Sub-Registers (PxAFS2)

BITS	7	6	5	4	3	2	1	0
FIELD	PAFS27	PAFS26	PAFS25	PAFS24	PAFS23	PAFS22	PAFS21	PAFS20
RESET	00H (all ports of 20/28 pin devices); 04H (Port A of 8-pin device)							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	If 08H in Port A–D Address Register, accessible through the Port A–D Control Register							

PAFS2[7:0]—Port Alternate Function Set 2
0 = Port Alternate Function selected as defined in Table 15.
1 = Port Alternate Function selected as defined in Table 15.

Port A–C Input Data Registers

Reading from the Port A–C Input Data registers (Table 27) returns the sampled values from the corresponding port pins. The Port A–C Input Data registers are read-only. The value returned for any unused ports is 0. Unused ports include those missing on the 8- and 28-pin packages, as well as those missing on the ADC-enabled 28-pin packages.

Table 27. Port A–C Input Data Registers (PxIN)

BITS	7	6	5	4	3	2	1	0
FIELD	PIN7	PIN6	PIN5	PIN4	PIN3	PIN2	PIN1	PIN0
RESET	X	X	X	X	X	X	X	X
R/W	R	R	R	R	R	R	R	R
ADDR	FD2H, FD6H, FDAH							
X = Undefined.								

Caution: *To avoid re-triggerings of the Watchdog Timer interrupt after exiting the associated interrupt service routine, it is recommended that the service routine continues to read from the RSTSTAT register until the WDT bit is cleared as given in the following coding sample:*

```
CLEARWDT:
 LDX r0, RSTSTAT  ; read reset status register to clear wdt bit
 BTJNZ 5, r0, CLEARWDT   ; loop until bit is cleared
```

Interrupt Control Register Definitions

For all interrupts other than the Watchdog Timer interrupt, the Primary Oscillator Fail Trap, and the Watchdog Oscillator Fail Trap, the interrupt control registers enable individual interrupts, set interrupt priorities, and indicate interrupt requests.

Interrupt Request 0 Register

The Interrupt Request 0 (IRQ0) register (Table 33) stores the interrupt requests for both vectored and polled interrupts. When a request is presented to the interrupt controller, the corresponding bit in the IRQ0 register becomes 1. If interrupts are globally enabled (vectored interrupts), the interrupt controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU can read the Interrupt Request 0 register to determine if any interrupt requests are pending.

Table 33. Interrupt Request 0 Register (IRQ0)

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved	T1I	T0I	U0RXI	U0TXI	Reserved	Reserved	ADCI
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FC0H							

Reserved—Must be 0.

T1I—Timer 1 Interrupt Request
0 = No interrupt request is pending for Timer 1.
1 = An interrupt request from Timer 1 is awaiting service.

T0I—Timer 0 Interrupt Request
0 = No interrupt request is pending for Timer 0.
1 = An interrupt request from Timer 0 is awaiting service.

110 = 64 cycles delay
111 = 128 cycles delay

INPCAP—Input Capture Event
This bit indicates if the most recent timer interrupt is caused by a Timer Input Capture Event.

0 = Previous timer interrupt is not a result of Timer Input Capture Event
1 = Previous timer interrupt is a result of Timer Input Capture Event

Timer 0–1 Control Register 1

The Timer 0–1 Control (TxCTL1) registers enable/disable the timers, set the prescaler value, and determine the timer operating mode (Table 49).

Table 49. Timer 0–1 Control Register 1 (TxCTL1)

BITS	7	6	5	4	3	2	1	0
FIELD	TEN	TPOL	PRES			TMODE		
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F07H, F0FH							

TEN—Timer Enable
0 = Timer is disabled.
1 = Timer enabled to count.

TPOL—Timer Input/Output Polarity
Operation of this bit is a function of the current operating mode of the timer.

ONE-SHOT mode
When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

CONTINUOUS mode
When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

COUNTER mode
If the timer is enabled the Timer Output signal is complemented after timer reload.

0 = Count occurs on the rising edge of the Timer Input signal.

1 = Count occurs on the falling edge of the Timer Input signal.

CAPTURE RESTART mode
0 = Count is captured on the rising edge of the Timer Input signal.
1 = Count is captured on the falling edge of the Timer Input signal.

COMPARATOR COUNTER mode
When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload. Also:

0 = Count is captured on the rising edge of the comparator output.
1 = Count is captured on the falling edge of the comparator output.

Caution: *When the Timer Output alternate function TxOUT on a GPIO port pin is enabled, TxOUT changes to whatever state the TPOL bit is in.The timer does not need to be enabled for that to happen. Also, the Port data direction sub register is not needed to be set to output on TxOUT. Changing the TPOL bit with the timer enabled and running does not immediately change the TxOUT.*

PRES—Prescale value
The timer input clock is divided by 2^{PRES}, where PRES can be set from 0 to 7. The prescaler is reset each time the Timer is disabled. This reset ensures proper clock division each time the Timer is restarted.

000 = Divide by 1
001 = Divide by 2
010 = Divide by 4
011 = Divide by 8
100 = Divide by 16
101 = Divide by 32
110 = Divide by 64
111 = Divide by 128

TMODE—Timer mode
This field along with the TMODEHI bit in TxCTL0 register determines the operating mode of the timer. TMODEHI is the most significant bit of the Timer mode selection value. The entire operating mode bits are expressed as {TMODEHI, TMODE[2:0]}. The TMODEHI is bit 7 of the TxCTL0 register while TMODE[2:0] is the lower 3 bits of the TxCTL1 register.

0000 = ONE-SHOT mode
0001 = CONTINUOUS mode
0010 = COUNTER mode
0011 = PWM SINGLE OUTPUT mode
0100 = CAPTURE mode
0101 = COMPARE mode
0110 = GATED mode
0111 = CAPTURE/COMPARE mode

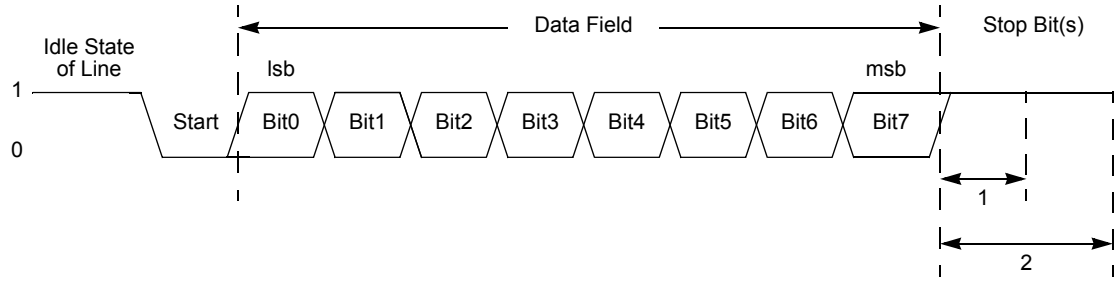


Figure 11. UART Asynchronous Data Format without Parity

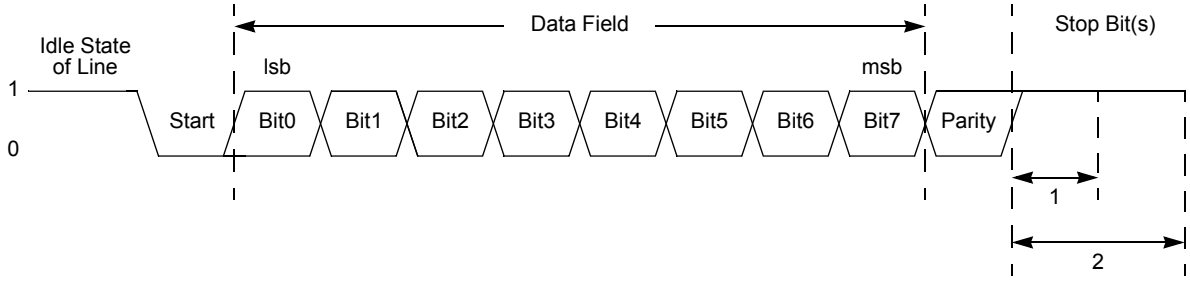


Figure 12. UART Asynchronous Data Format with Parity

Transmitting Data using the Polled Method

Follow the steps below to transmit data using the polled method of operation:

1. Write to the UART Baud Rate High and Low Byte registers to set the required baud rate.
2. Enable the UART pin functions by configuring the associated GPIO Port pins for alternate function operation.
3. Write to the UART Control 1 register, if MULTIPROCESSOR mode is appropriate, to enable MULTIPROCESSOR (9-bit) mode functions.
4. Set the Multiprocessor Mode Select (MPEN) bit to enable MULTIPROCESSOR mode.
5. Write to the UART Control 0 register to:
   - Set the transmit enable bit (TEN) to enable the UART for data transmission.
   - Set the parity enable bit (PEN), if parity is appropriate and MULTIPROCESSOR mode is not enabled, and select either even or odd parity (PSEL).
   - Set or clear the CTSE bit to enable or disable control from the remote receiver using the $\overline{\text{CTS}}$ pin.

MPRX—Multiprocessor Receive
Returns the value of the most recent multiprocessor bit received. Reading from the UART Receive Data register resets this bit to 0.

UART Transmit Data Register

Data bytes written to the UART Transmit Data (UxTXD) register (Table 65) are shifted out on the TXDx pin. The Write-only UART Transmit Data register shares a Register File address with the read-only UART Receive Data register.

Table 65. UART Transmit Data Register (U0TXD)

BITS	7	6	5	4	3	2	1	0
FIELD	TXD							
RESET	X	X	X	X	X	X	X	X
R/W	W	W	W	W	W	W	W	W
ADDR	F40H							

TXD—Transmit Data
UART transmitter data byte to be shifted out through the TXD*x* pin.

UART Receive Data Register

Data bytes received through the RXD*x* pin are stored in the UART Receive Data (UxRXD) register (Table 66). The read-only UART Receive Data register shares a Register File address with the Write-only UART Transmit Data register.

Table 66. UART Receive Data Register (U0RXD)

BITS	7	6	5	4	3	2	1	0
FIELD	RXD							
RESET	X	X	X	X	X	X	X	X
R/W	R	R	R	R	R	R	R	R
ADDR	F40H							
X = Undefined.								

RXD—Receive Data
UART receiver data byte from the RXD*x* pin

```
nop      ; wait for output to settle
clr irq0 ; clear any spurious interrupts pending
ei
```

Comparator Control Register Definitions

Comparator Control Register

The Comparator Control Register (CMP0) configures the comparator inputs and sets the value of the internal voltage reference.

Table 75. Comparator Control Register (CMP0)

BITS	7	6	5	4	3	2	1	0
FIELD	INPSEL	INNSEL	REFLVL				Reserved (20-/28-pin) REFLVL (8-pin)	
RESET	0	0	0	1	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F90H							

INPSEL—Signal Select for Positive Input
0 = GPIO pin used as positive comparator input
1 = temperature sensor used as positive comparator input

INNSEL—Signal Select for Negative Input
0 = internal reference disabled, GPIO pin used as negative comparator input
1 = internal reference enabled as negative comparator input

REFLVL—Internal Reference Voltage Level (this reference is independent of the ADC voltage reference). Note that the 8-pin devices contain two additional LSBs for increased resolution.

For 20-/28-pin devices:

0000 = 0.0 V
0001 = 0.2 V
0010 = 0.4 V
0011 = 0.6 V
0100 = 0.8 V
0101 = 1.0 V (Default)
0110 = 1.2 V
0111 = 1.4 V
1000 = 1.6 V

Flash Status Register

The Flash Status (FSTAT) register indicates the current state of the Flash Controller. This register can be read at any time. The read-only Flash Status register shares its Register File address with the Write-only Flash Control register.

Table 79. Flash Status Register (FSTAT)

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved		FSTAT					
RESET	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R
ADDR	FF8H							

Reserved—Must be 0.

FSTAT—Flash Controller Status
000000 = Flash Controller locked
000001 = First unlock command received (73H written)
000010 = Second unlock command received (8CH written)
000011 = Flash Controller unlocked

000100 = Sector protect register selected

001xxx = Program operation in progress
010xxx = Page erase operation in progress
100xxx = Mass erase operation in progress

Flash Page Select Register

The Flash Page Select (FPS) register shares address space with the Flash Sector Protect Register. Unless the Flash controller is unlocked and written with 5EH, writes to this address target the Flash Page Select Register.

The register is used to select one of the available Flash memory pages to be programmed or erased. Each Flash Page contains 512 bytes of Flash memory. During a Page Erase operation, all Flash memory having addresses with the most significant 7 bits given by FPS[6:0] are chosen for program/erase operation.

Table 117. Bit Manipulation Instructions

Mnemonic	Operands	Instruction
BCLR	bit, dst	Bit Clear
BIT	p, bit, dst	Bit Set or Clear
BSET	bit, dst	Bit Set
BSWAP	dst	Bit Swap
CCF	—	Complement Carry Flag
RCF	—	Reset Carry Flag
SCF	—	Set Carry Flag
TCM	dst, src	Test Complement Under Mask
TCMX	dst, src	Test Complement Under Mask using Extended Addressing
TM	dst, src	Test Under Mask
TMX	dst, src	Test Under Mask using Extended Addressing

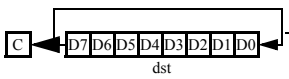
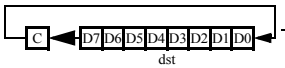
Table 118. Block Transfer Instructions

Mnemonic	Operands	Instruction
LDCI	dst, src	Load Constant to/from Program Memory and Auto-Increment Addresses
LDEI	dst, src	Load External Data to/from Data Memory and Auto-Increment Addresses

Table 119. CPU Control Instructions

Mnemonic	Operands	Instruction
ATM	—	Atomic Execution
CCF	—	Complement Carry Flag
DI	—	Disable Interrupts
EI	—	Enable Interrupts
HALT	—	Halt Mode
NOP	—	No Operation
RCF	—	Reset Carry Flag

Table 124. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Opcode(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
OR dst, src	dst ← dst OR src	r	r	42	–	*	*	0	–	–	2	3
		r	Ir	43							2	4
		R	R	44							3	3
		R	IR	45							3	4
		R	IM	46							3	3
		IR	IM	47							3	4
ORX dst, src	dst ← dst OR src	ER	ER	48	–	*	*	0	–	–	4	3
		ER	IM	49							4	3
POP dst	dst ← @SP SP ← SP + 1	R		50	–	–	–	–	–	–	2	2
		IR		51							2	3
POPX dst	dst ← @SP SP ← SP + 1	ER		D8	–	–	–	–	–	–	3	2
PUSH src	SP ← SP – 1 @SP ← src	R		70	–	–	–	–	–	–	2	2
		IR		71							2	3
		IM		IF70							3	2
PUSHX src	SP ← SP – 1 @SP ← src	ER		C8	–	–	–	–	–	–	3	2
RCF	C ← 0			CF	0	–	–	–	–	–	1	2
RET	PC ← @SP SP ← SP + 2			AF	–	–	–	–	–	–	1	4
RL dst		R		90	*	*	*	*	–	–	2	2
		IR		91							2	3
RLC dst		R		10	*	*	*	*	–	–	2	2
		IR		11							2	3

Flags Notation:	* = Value is a function of the result of the operation. – = Unaffected X = Undefined	0 = Reset to 0 1 = Set to 1

Electrical Characteristics

The data in this chapter is pre-qualification and pre-characterization and is subject to change. Additional electrical characteristics may be found in the individual chapters.

Absolute Maximum Ratings

Stresses greater than those listed in Table 126 may cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, tie unused inputs to one of the supply voltages (V_{DD} or V_{SS}).

Table 126. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	-40	+105	°C	
Storage temperature	-65	+150	°C	
Voltage on any pin with respect to V_{SS}	-0.3	+5.5	V	1
	-0.3	+3.9	V	2
Voltage on V_{DD} pin with respect to V_{SS}	-0.3	+3.6	V	
Maximum current on input and/or inactive output pin	-5	+5	µA	
Maximum output current from active output pin	-25	+25	mA	
8-pin Packages Maximum Ratings at 0 °C to 70 °C				
Total power dissipation		220	mW	
Maximum current into V_{DD} or out of V_{SS}		60	mA	
20-pin Packages Maximum Ratings at 0 °C to 70 °C				
Total power dissipation		430	mW	
Maximum current into V_{DD} or out of V_{SS}		120	mA	

Table 130. Internal Precision Oscillator Electrical Characteristics

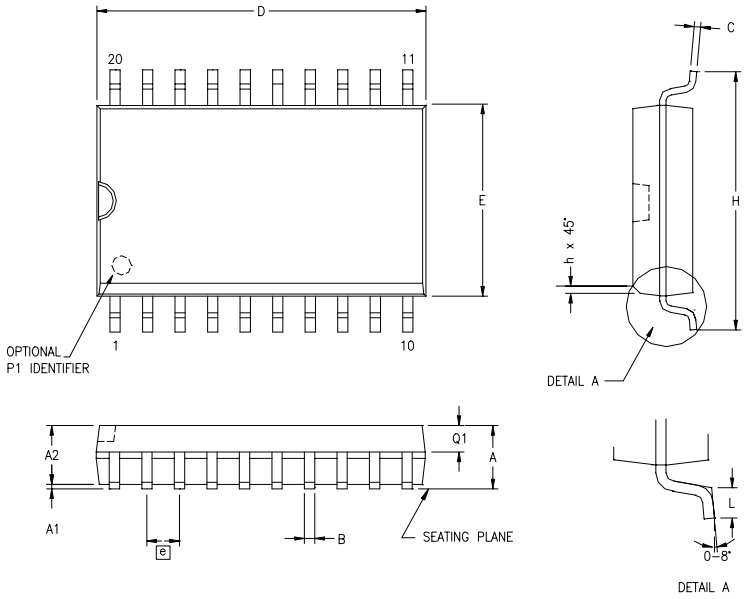
		V_{DD} = 2.7 V to 3.6 V T_A = -40 °C to +105 °C (unless otherwise stated)				
Symbol	**Parameter**	**Minimum**	**Typical**	**Maximum**	**Units**	**Conditions**
F_{IPO}	Internal Precision Oscillator Frequency (High Speed)		5.53		MHz	V_{DD} = 3.3 V T_A = 30 °C
F_{IPO}	Internal Precision Oscillator Frequency (Low Speed)		32.7		kHz	V_{DD} = 3.3 V T_A = 30 °C
F_{IPO}	Internal Precision Oscillator Error		±1	±4	%	
T_{IPOST}	Internal Precision Oscillator Startup Time		3		µs	

Table 135. Analog-to-Digital Converter Electrical Characteristics and Timing (Continued)

		V_{DD} = 3.0 V to 3.6 V T_A = 0 °C to +70 °C (unless otherwise stated)				
Symbol	**Parameter**	**Minimum**	**Typical**	**Maximum**	**Units**	**Conditions**
	Single-Shot Conversion Time	–	5129	–	System clock cycles	All measurements but temperature sensor
			10258			Temperature sensor measurement
	Continuous Conversion Time	–	256	–	System clock cycles	All measurements but temperature sensor
			512			Temperature sensor measurement
	Signal Input Bandwidth	–	10		kHz	As defined by -3 dB point
R_S	Analog Source Impedance[4]	–	–	10	kΩ	In unbuffered mode
				500	kΩ	In buffered modes
Zin	Input Impedance	–	150		kΩ	In unbuffered mode at 20 MHz[5]
		10	–		MΩ	In buffered modes
Vin	Input Voltage Range	0		V_{DD}	V	Unbuffered Mode
		0.3		V_{DD}-1.1	V	Buffered Modes
					Note:	*These values define the range over which the ADC performs within spec; exceeding these values does not cause damage or instability;* see DC Characteristics on page 222 *for absolute pin voltage limits*

Notes
1. Analog source impedance affects the ADC offset voltage (because of pin leakage) and input settling time.
2. Devices are factory calibrated at V_{DD} = 3.3 V and T_A = +30 °C, so the ADC is maximally accurate under these conditions.
3. LSBs are defined assuming 10-bit resolution.
4. This is the maximum recommended resistance seen by the ADC input pin.
5. The input impedance is inversely proportional to the system clock frequency.

Figure 43 displays the 20-pin Small Outline Integrated Circuit Package (SOIC) available for the Z8 Encore! XP F082A Series devices.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	12.60	12.95	**.496**	.510
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 43. 20-Pin Small Outline Integrated Circuit Package (SOIC)

Part Number	Flash	RAM	NVDS	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Description
Z8 Encore! XP® F082A Series with 1 KB Flash											
Standard Temperature: 0 °C to 70 °C											
Z8F011APB020SC	1 KB	256 B	16 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F011AQB020SC	1 KB	256 B	16 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F011ASB020SC	1 KB	256 B	16 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F011ASH020SC	1 KB	256 B	16 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F011AHH020SC	1 KB	256 B	16 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F011APH020SC	1 KB	256 B	16 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F011ASJ020SC	1 KB	256 B	16 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F011AHJ020SC	1 KB	256 B	16 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F011APJ020SC	1 KB	256 B	16 B	25	19	2	0	1	1	0	PDIP 28-pin package
Extended Temperature: -40 °C to 105 °C											
Z8F011APB020EC	1 KB	256 B	16 B	6	13	2	0	1	1	0	PDIP 8-pin package
Z8F011AQB020EC	1 KB	256 B	16 B	6	13	2	0	1	1	0	QFN 8-pin package
Z8F011ASB020EC	1 KB	256 B	16 B	6	13	2	0	1	1	0	SOIC 8-pin package
Z8F011ASH020EC	1 KB	256 B	16 B	17	19	2	0	1	1	0	SOIC 20-pin package
Z8F011AHH020EC	1 KB	256 B	16 B	17	19	2	0	1	1	0	SSOP 20-pin package
Z8F011APH020EC	1 KB	256 B	16 B	17	19	2	0	1	1	0	PDIP 20-pin package
Z8F011ASJ020EC	1 KB	256 B	16 B	25	19	2	0	1	1	0	SOIC 28-pin package
Z8F011AHJ020EC	1 KB	256 B	16 B	25	19	2	0	1	1	0	SSOP 28-pin package
Z8F011APJ020EC	1 KB	256 B	16 B	25	19	2	0	1	1	0	PDIP 28-pin package
Replace C with G for Lead-Free Packaging											

S