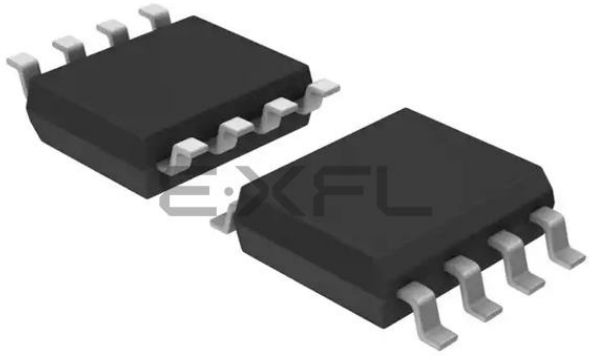

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	6
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f082asb020ec

Block Diagram

Figure 1displays the block diagram of the architecture of the Z8 Encore!® XP F082A Series devices.

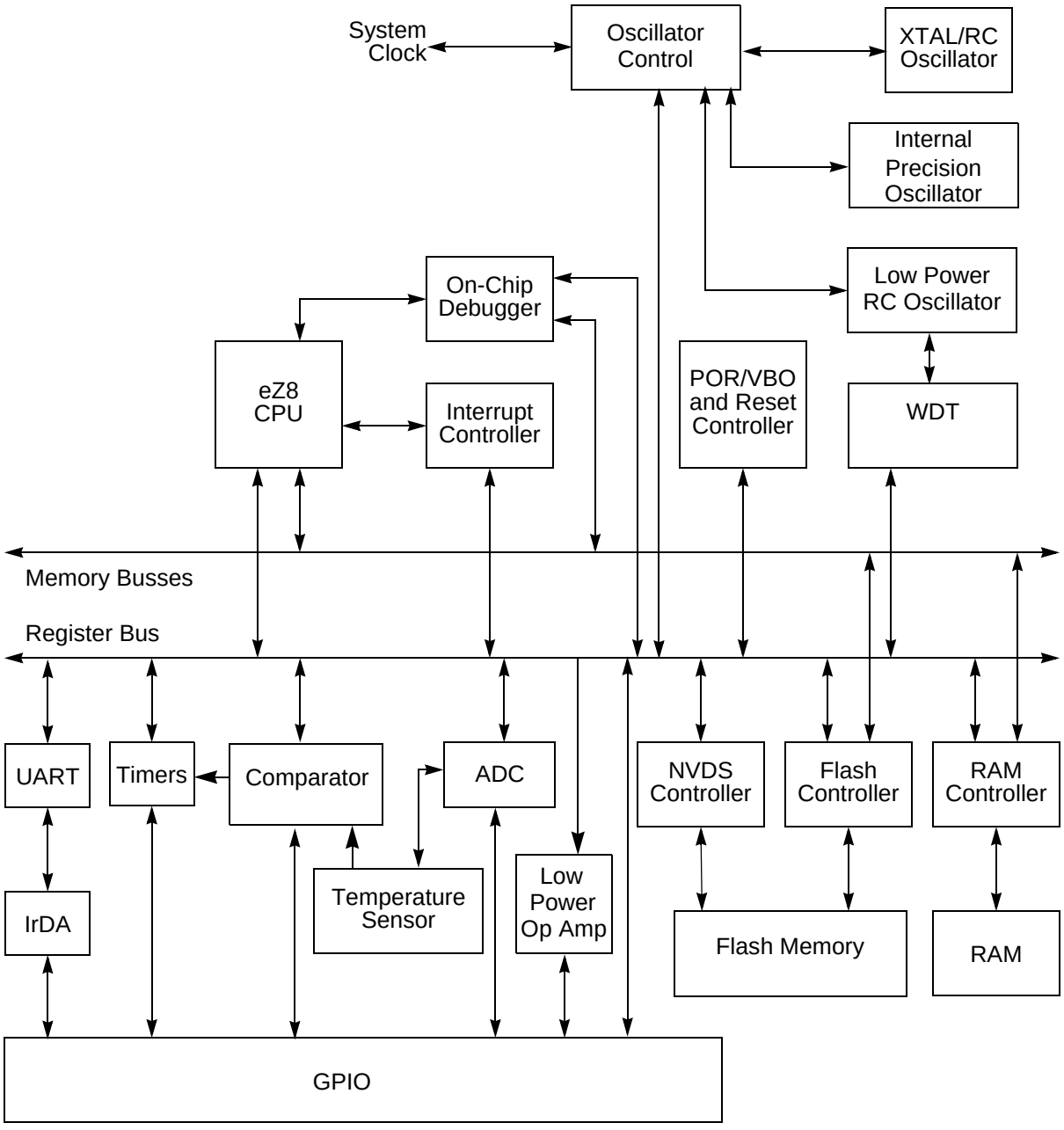

Figure 1. Z8 Encore! XP F082A Series Block Diagram

during STOP mode do not initiate Stop Mode Recovery.
1 = The Port pin is configured as a Stop Mode Recovery source. Any logic transition on this pin during STOP mode initiates Stop Mode Recovery.

Port A–D Pull-up Enable Sub-Registers

The Port A–D Pull-up Enable sub-register (Table 24) is accessed through the Port A–D Control register by writing 06H to the Port A–D Address register. Setting the bits in the Port A–D Pull-up Enable sub-registers enable weak internal resistive pull-up on the specified Port pins.

Table 24. Port A–D Pull-Up Enable Sub-Registers (PxPUE)

BITS	7	6	5	4	3	2	1	0
FIELD	PPUE7	PPUE6	PPUE5	PPUE4	PPUE3	PPUE2	PPUE1	PPUE0
RESET	00H (Ports A-C); 01H (Port D); 04H (Port A of 8-pin device)							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	If 06H in Port A–D Address Register, accessible through the Port A–D Control Register							

PPUE[7:0]—Port Pull-up Enabled
0 = The weak pull-up on the Port pin is disabled.
1 = The weak pull-up on the Port pin is enabled.

Port A–D Alternate Function Set 1 Sub-Registers

The Port A–D Alternate Function Set1 sub-register (Table 25) is accessed through the Port A–D Control register by writing 07H to the Port A–D Address register. The Alternate Function Set 1 sub-registers selects the alternate function available at a port pin. Alternate Functions selected by setting or clearing bits of this register are defined in GPIO Alternate Functions on page 38.

Note: *Alternate function selection on port pins must also be enabled as described in* Port A–D Alternate Function Sub-Registers *on page 47.*

Table 25. Port A–D Alternate Function Set 1 Sub-Registers (PxAFS1)

BITS	7	6	5	4	3	2	1	0
FIELD	PAFS17	PAFS16	PAFS15	PAFS14	PAFS13	PAFS12	PAFS11	PAFS10
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	If 07H in Port A–D Address Register, accessible through the Port A–D Control Register							

PAFS1[7:0]—Port Alternate Function Set 1
0 = Port Alternate Function selected as defined in Table 14 and Table 15 on page 44.
1 = Port Alternate Function selected as defined in Table 14 and Table 15 on page 44.

Port A–D Alternate Function Set 2 Sub-Registers

The Port A–D Alternate Function Set 2 sub-registers (Table 26) is accessed through the Port A–D Control register by writing 08H to the Port A–D Address register. The Alternate Function Set 2 sub-registers selects the alternate function available at a port pin. Alternate Functions selected by setting or clearing bits of this register is defined in Table 15.

Note: *Alternate function selection on port pins must also be enabled as described in* Port A–D Alternate Function Sub-Registers on page 47.

Table 26. Port A–D Alternate Function Set 2 Sub-Registers (PxAFS2)

BITS	7	6	5	4	3	2	1	0
FIELD	PAFS27	PAFS26	PAFS25	PAFS24	PAFS23	PAFS22	PAFS21	PAFS20
RESET	00H (all ports of 20/28 pin devices); 04H (Port A of 8-pin device)							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	If 08H in Port A–D Address Register, accessible through the Port A–D Control Register							

PAFS2[7:0]—Port Alternate Function Set 2
0 = Port Alternate Function selected as defined in Table 15.
1 = Port Alternate Function selected as defined in Table 15.

Port A–C Input Data Registers

Reading from the Port A–C Input Data registers (Table 27) returns the sampled values from the corresponding ports pins. The Port A–C Input Data registers are read-only. The value returned for any unused ports is 0. Unused ports include those missing on the 8- and 28-pin packages, as well as those missing on the ADC-enabled 28-pin packages.

Table 27. Port A–C Input Data Registers (PxIN)

BITS	7	6	5	4	3	2	1	0
FIELD	PIN7	PIN6	PIN5	PIN4	PIN3	PIN2	PIN1	PIN0
RESET	X	X	X	X	X	X	X	X
R/W	R	R	R	R	R	R	R	R
ADDR	FD2H, FD6H, FDAH							
X = Undefined.								

2. Write to the Timer High and Low Byte registers to set the starting count value. Writing these registers only affects the first pass in GATED mode. After the first timer reset in GATED mode, counting always begins at the reset value of 0001H.
3. Write to the Timer Reload High and Low Byte registers to set the Reload value.
4. Enable the timer interrupt, if appropriate, and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input deassertion and reload events. If appropriate, configure the timer interrupt to be generated only at the input deassertion event or the reload event by setting TICONFIG field of the TxCTL0 register.
5. Configure the associated GPIO port pin for the Timer Input alternate function.
6. Write to the Timer Control register to enable the timer.
7. Assert the Timer Input signal to initiate the counting.

CAPTURE/COMPARE Mode

In CAPTURE/COMPARE mode, the timer begins counting on the first external Timer Input transition. The acceptable transition is either (rising edge or falling edge) is set by the CAPCTL bit in the Timer Control Register. The timer input is the system clock.

Every subsequent acceptable transition (after the first) of the Timer Input signal captures the current count value. The Capture value is written to the Timer PWM High and Low Byte Registers. When the Capture event occurs, an interrupt is generated, the count value in the Timer High and Low Byte registers is reset to 0001H, and counting resumes. The INPCAP bit in TxCTL0 register is set to indicate the timer interrupt is caused by an input capture event.

If no Capture event occurs, the timer counts up to the 16-bit Compare value stored in the Timer Reload High and Low Byte registers. Upon reaching the Compare value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. The INPCAP bit in TxCTL0 register is cleared to indicate the timer interrupt is not because of an input capture event.

Follow the steps below for configuring the timer for CAPTURE/COMPARE mode and initiating the count:

1. Write to the Timer Control register to:
   - Disable the timer.
   - Configure the timer for CAPTURE/COMPARE mode.
   - Set the prescale value.
   - Set the Capture edge (rising edge or falling edge) for the Timer Input.
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
3. Write to the Timer Reload High and Low Byte registers to set the Compare value.

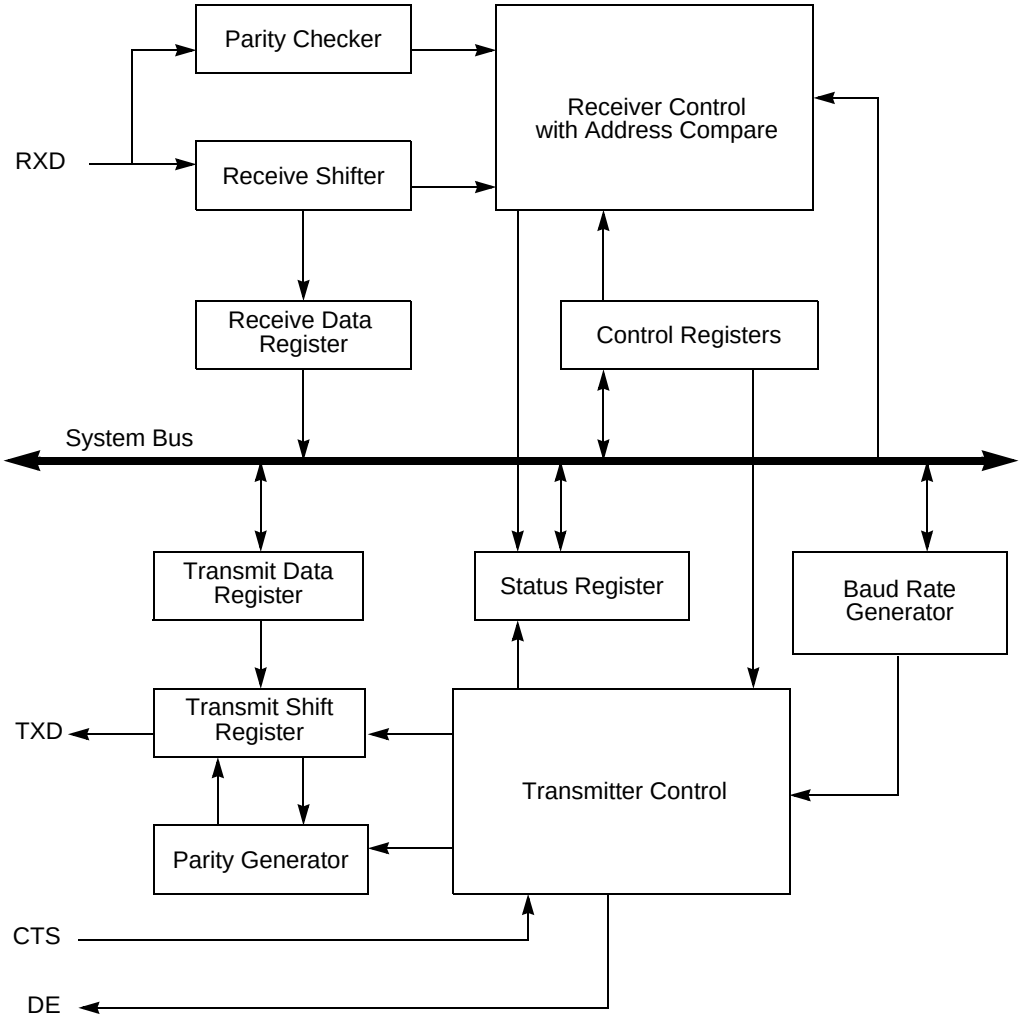

Figure 10. UART Block Diagram

Operation

Data Format

The UART always transmits and receives data in 8-bit data format, least-significant bit first. An even or odd parity bit can be added to the data stream. Each character begins with an active Low START bit and ends with either 1 or 2 active High STOP bits. Figure 11 and Figure 12 display the asynchronous data format employed by the UART without parity and with parity, respectively.

UART Address Compare Register

The UART Address Compare (UADDR) register stores the multi-node network address of the UART (see Table 67). When the MPMD[1] bit of UART Control Register 0 is set, all incoming address bytes are compared to the value stored in the Address Compare register. Receive interrupts and RDA assertion only occur in the event of a match.

Table 67. UART Address Compare Register (U0ADDR)

BITS	7	6	5	4	3	2	1	0
FIELD	COMP_ADDR							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F45H							

COMP_ADDR—Compare Address
This 8-bit value is compared to incoming address bytes.

UART Baud Rate High and Low Byte Registers

The UART Baud Rate High (UxBRH) and Low Byte (UxBRL) registers (Table 68 and Table 69) combine to create a 16-bit baud rate divisor value (BRG[15:0]) that sets the data transmission rate (baud rate) of the UART.

Table 68. UART Baud Rate High Byte Register (U0BRH)

BITS	7	6	5	4	3	2	1	0
FIELD	BRH							
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F46H							

Table 69. UART Baud Rate Low Byte Register (U0BRL)

BITS	7	6	5	4	3	2	1	0
FIELD	BRL							
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F47H							

Table 70. UART Baud Rates (Continued)

3.579545 MHz System Clock				1.8432 MHz System Clock			
Acceptable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)	Acceptable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)
1250.0	N/A	N/A	N/A	1250.0	N/A	N/A	N/A
625.0	N/A	N/A	N/A	625.0	N/A	N/A	N/A
250.0	1	223.72	-10.51	250.0	N/A	N/A	N/A
115.2	2	111.9	-2.90	115.2	1	115.2	0.00
57.6	4	55.9	-2.90	57.6	2	57.6	0.00
38.4	6	37.3	-2.90	38.4	3	38.4	0.00
19.2	12	18.6	-2.90	19.2	6	19.2	0.00
9.60	23	9.73	1.32	9.60	12	9.60	0.00
4.80	47	4.76	-0.83	4.80	24	4.80	0.00
2.40	93	2.41	0.23	2.40	48	2.40	0.00
1.20	186	1.20	0.23	1.20	96	1.20	0.00
0.60	373	0.60	-0.04	0.60	192	0.60	0.00
0.30	746	0.30	-0.04	0.30	384	0.30	0.00

Operation

The Flash Controller programs and erases the Flash memory. The Flash Controller provides the proper Flash controls and timing for Byte Programming, Page Erase, and Mass Erase of Flash memory.

The Flash Controller contains several protection mechanisms to prevent accidental programming or erasure. These mechanism operate at the page, sector, and full-memory levels.

The Flow Chart in Figure 22 displays basic Flash Controller operation. The following subsections provide details about the various operations (Lock, Unlock, Byte Programming, Page Protect, Page Unprotect, Page Select, Page Erase, and Mass Erase) displayed in Figure 22

Flash Control Regi ster Definitions

Flash Control Register

The Flash Controller must be unlocked using the Flash Control (FCTL) register before programming or erasing the Flash memory. Writing the sequence 73H 8CH, sequentially, to the Flash Control register unlocks the Flash Controller. When the Flash Controller is unlocked, the Flash memory can be enabled for Mass Erase or Page Erase by writing the appropriate enable command to the FCTL register. Page Erase applies only to the active page selected in Flash Page Select register. Mass Erase is enabled only through the On-Chip Debugger. Writing an invalid value or an invalid sequence returns the Flash Controller to its locked state. The Write-only Flash Control Register shares its Register File address with the read-only Flash Status Register.

Table 78. Flash Control Register (FCTL)

BITS	7	6	5	4	3	2	1	0
FIELD	FCMD							
RESET	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W
ADDR	FF8H							

FCMD—Flash Command
73H = First unlock command.
8CH = Second unlock command.

95H = Page Erase command (must be third command in sequence to initiate Page Erase).
63H = Mass Erase command (must be third command in sequence to initiate Mass Erase).

5EH = Enable Flash Sector Protect Register Access

Table 94. ADC Calibration Data Location (Continued)

Info Page Address	Memory Address	Compensation Usage	ADC Mode	Reference Type
34	FE34	Negative Gain High Byte	Differential Unbuffered	External 2.0 V
35	FE35	Negative Gain Low Byte	Differential Unbuffered	External 2.0 V
78	FE78	Offset	Differential 1x Buffered	Internal 2.0 V
18	FE18	Positive Gain High Byte	Differential 1x Buffered	Internal 2.0 V
19	FE19	Positive Gain Low Byte	Differential 1x Buffered	Internal 2.0 V
36	FE36	Negative Gain High Byte	Differential 1x Buffered	Internal 2.0 V
37	FE37	Negative Gain Low Byte	Differential 1x Buffered	Internal 2.0 V
7B	FE7B	Offset	Differential 1x Buffered	External 2.0 V
1A	FE1A	Positive Gain High Byte	Differential 1x Buffered	External 2.0 V
1B	FE1B	Positive Gain Low Byte	Differential 1x Buffered	External 2.0 V
38	FE38	Negative Gain High Byte	Differential 1x Buffered	External 2.0 V
39	FE39	Negative Gain Low Byte	Differential 1x Buffered	External 2.0 V

DBGACK—Debug Acknowledge
This bit enables the debug acknowledge feature. If this bit is set to 1, the OCD sends a Debug Acknowledge character (FFH) to the host when a Breakpoint occurs.
0 = Debug Acknowledge is disabled.
1 = Debug Acknowledge is enabled.

Reserved—Must be 0.

RST—Reset
Setting this bit to 1 resets the Z8F04xA family device. The device goes through a normal Power-On Reset sequence with the exception that the On-Chip Debugger is not reset. This bit is automatically cleared to 0 at the end of reset.
0 = No effect.
1 = Reset the Flash Read Protect Option Bit device.

OCD Status Register

The OCD Status register reports status information about the current state of the debugger and the system.

Table 107. OCD Status Register (OCDSTAT)

BITS	7	6	5	4	3	2	1	0
FIELD	DBG	HALT	FRPENB	Reserved				
RESET	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

DBG—Debug Status
0 = NORMAL mode
1 = DEBUG mode

HALT—HALT Mode
0 = Not in HALT mode
1 = In HALT mode

FRPENB—Flash Read Protect Option Bit Enable
0 = FRP bit enabled, that allows disabling of many OCD commands
1 = FRP bit has no effect

Reserved—Must be 0

Table 108. Oscillator Configuration and Selection

Clock Source	Characteristics	Required Setup
Internal Precision RC Oscillator	• 32.8 kHz or 5.53 MHz • High accuracy • No external components required	• Unlock and write Oscillator Control Register (OSCCTL) to enable and select oscillator at either 5.53 MHz or 32.8 kHz
External Crystal/ Resonator	• 32 kHz to 20 MHz • Very high accuracy (dependent on crystal or resonator used) • Requires external components	• Configure Flash option bits for correct external oscillator mode • Unlock and write OSCCTL to enable crystal oscillator, wait for it to stabilize and select as system clock (if the XTLDIS option bit has been de-asserted, no waiting is required)
External RC Oscillator	• 32 kHz to 4 MHz • Accuracy dependent on external components	• Configure Flash option bits for correct external oscillator mode • Unlock and write OSCCTL to enable crystal oscillator and select as system clock
External Clock Drive	• 0 to 20 MHz • Accuracy dependent on external clock source	• Write GPIO registers to configure PB3 pin for external clock function • Unlock and write OSCCTL to select external system clock • Apply external clock signal to GPIO
Internal Watchdog Timer Oscillator	• 10 kHz nominal • Low accuracy; no external components required • Very low power consumption	• Enable WDT if not enabled and wait until WDT Oscillator is operating. • Unlock and write Oscillator Control Register (OSCCTL) to enable and select oscillator

Caution: *Unintentional accesses to the oscillator control register can actually stop the chip by switching to a non-functioning oscillator. To prevent this condition, the oscillator control block employs a register unlocking/locking scheme.*

OSC Control Register Unlocking/Locking

To write the oscillator control register, unlock it by making two writes to the OSCCTL register with the values E7H followed by 18H. A third write to the OSCCTL register changes the value of the actual register and locks the register to a locked state. Any other sequence of oscillator control register writes has no effect. The values written to unlock the register must be ordered correctly, but not necessarily consecutive. It is possible to write to or read from other registers within the unlocking/locking operation.

WDFEN—Watchdog Timer Oscillator Failure Detection Enable
1 = Failure detection of Watchdog Timer oscillator is enabled
0 = Failure detection of Watchdog Timer oscillator is disabled

SCKSEL—System Clock Oscillator Select
000 = Internal precision oscillator functions as system clock at 5.53 MHz
001 = Internal precision oscillator functions as system clock at 32 kHz
010 = Crystal oscillator or external RC oscillator functions as system clock
011 = Watchdog Timer oscillator functions as system
100 = External clock signal on PB3 functions as system clock
101 = Reserved
110 = Reserved
111 = Reserved

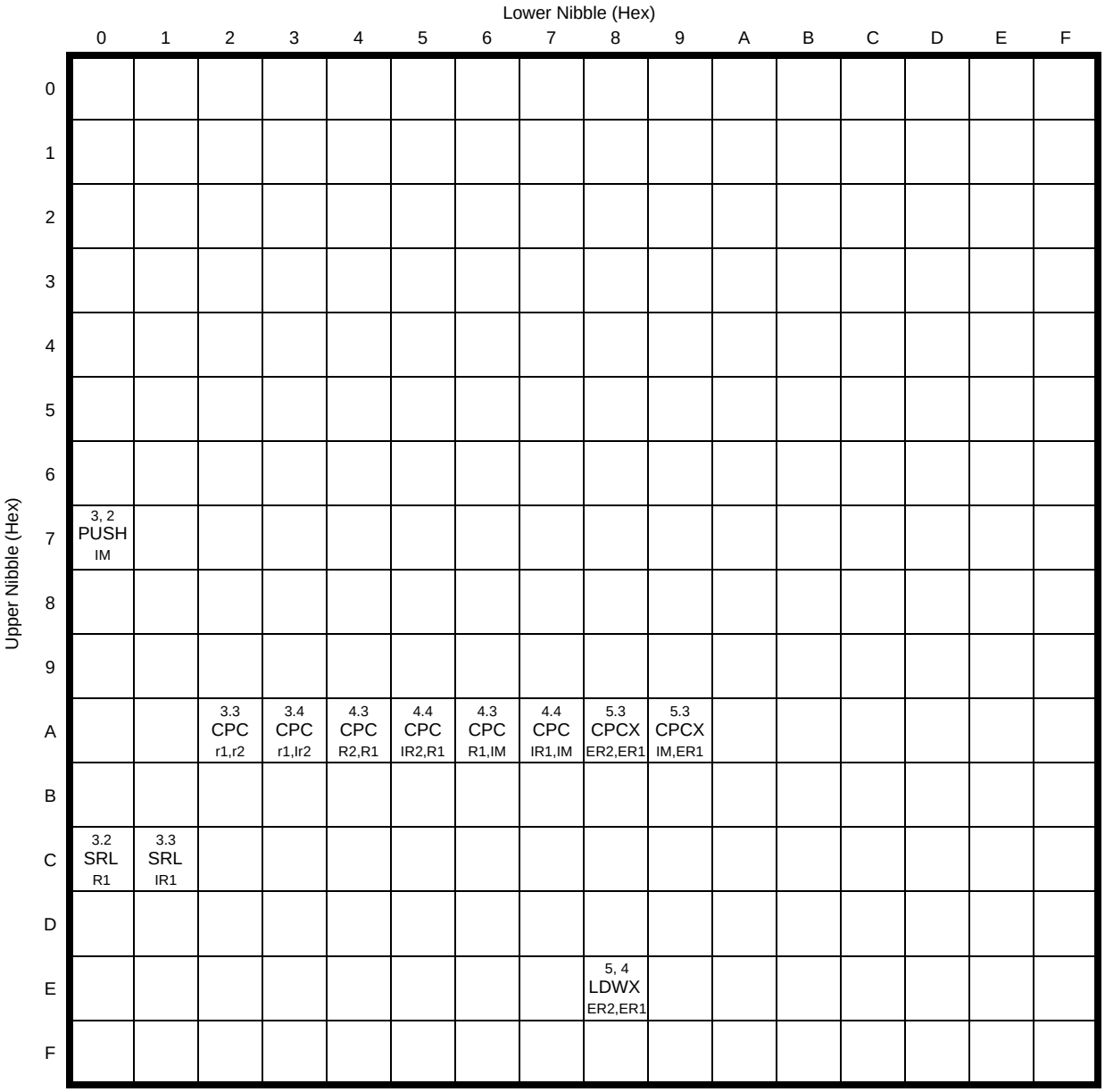

Figure 32. Second Opcode Map after 1FH

On-Chip Peripheral AC and DC Electrical Characteristics

Table 131. Power-On Reset and Voltage Brownout Electrical Characteristics and Timing

		T_A = -40 °C to +105 °C				
Symbol	Parameter	Minimum	Typical [1]	Maximum	Units	Conditions
V_{POR}	Power-On Reset Voltage Threshold	2.20	2.45	2.70	V	$V_{DD} = V_{POR}$
V_{VBO}	Voltage Brownout Reset Voltage Threshold	2.15	2.40	2.65	V	$V_{DD} = V_{VBO}$
	V_{POR} to V_{VBO} hysteresis		50	75	mV	
	Starting V_{DD} voltage to ensure valid Power-On Reset.	–	V_{SS}	–	V	
T_{ANA}	Power-On Reset Analog Delay	–	70	–	µs	$V_{DD} > V_{POR}$; T_{POR} Digital Reset delay follows T_{ANA}
T_{POR}	Power-On Reset Digital Delay		16		µs	66 Internal Precision Oscillator cycles + IPO startup time (T_{IPOST})
T_{POR}	Power-On Reset Digital Delay		1		ms	5000 Internal Precision Oscillator cycles
T_{SMR}	Stop Mode Recovery with crystal oscillator disabled		16		µs	66 Internal Precision Oscillator cycles
T_{SMR}	Stop Mode Recovery with crystal oscillator enabled		1		ms	5000 Internal Precision Oscillator cycles
T_{VBO}	Voltage Brownout Pulse Rejection Period	–	10	–	µs	Period of time in which $V_{DD} < V_{VBO}$ without generating a Reset.
T_{RAMP}	Time for V_{DD} to transition from V_{SS} to V_{POR} to ensure valid Reset	0.10	–	100	ms	
T_{SMP}	Stop Mode Recovery pin pulse rejection period		20		ns	For any SMR pin or for the Reset pin when it is asserted in STOP mode.

[1]Data in the typical column is from characterization at 3.3 V and 30 °C. These values are provided for design guidance only and are not tested in production.

Table 134. Non-Volatile Data Storage

	V_{DD} = 2.7 V to 3.6 V T_A = -40 °C to +105 °C				
Parameter	Minimum	Typical	Maximum	Units	Notes
NVDS Byte Read Time	34	–	519	µs	With system clock at 20 MHz
NVDS Byte Program Time	0.171	–	39.7	ms	With system clock at 20 MHz
Data Retention	100	–	–	years	25 °C
Endurance	160,000	–	–	cycles	Cumulative write cycles for entire memory

Table 135. Analog-to-Digital Converter Electrical Characteristics and Timing

		V_{DD} = 3.0 V to 3.6 V T_A = 0 °C to +70 °C (unless otherwise stated)				
Symbol	Parameter	Minimum	Typical	Maximum	Units	Conditions
	Resolution	10		–	bits	
	Differential Nonlinearity (DNL)	-1.0	–	1.0	LSB[3]	External V_{REF} = 2.0 V; $R_S \leftarrow$ 3.0 kΩ
	Integral Nonlinearity (INL)	-3.0	–	3.0	LSB[3]	External V_{REF} = 2.0 V; $R_S \leftarrow$ 3.0 kΩ
	Offset Error with Calibration		±1		LSB[3]	
	Absolute Accuracy with Calibration		±3		LSB[3]	
V_{REF}	Internal Reference Voltage	1.0 2.0	1.1 2.2	1.2 2.4	V	REFSEL=01 REFSEL=10
V_{REF}	Internal Reference Variation with Temperature		±1.0		%	Temperature variation with V_{DD} = 3.0
V_{REF}	Internal Reference Voltage Variation with V_{DD}		±0.5		%	Supply voltage variation with T_A = 30 °C
R_{REFOUT}	Reference Buffer Output Impedance		850		Ω	When the internal reference is buffered and driven out to the VREF pin (REFOUT = 1)

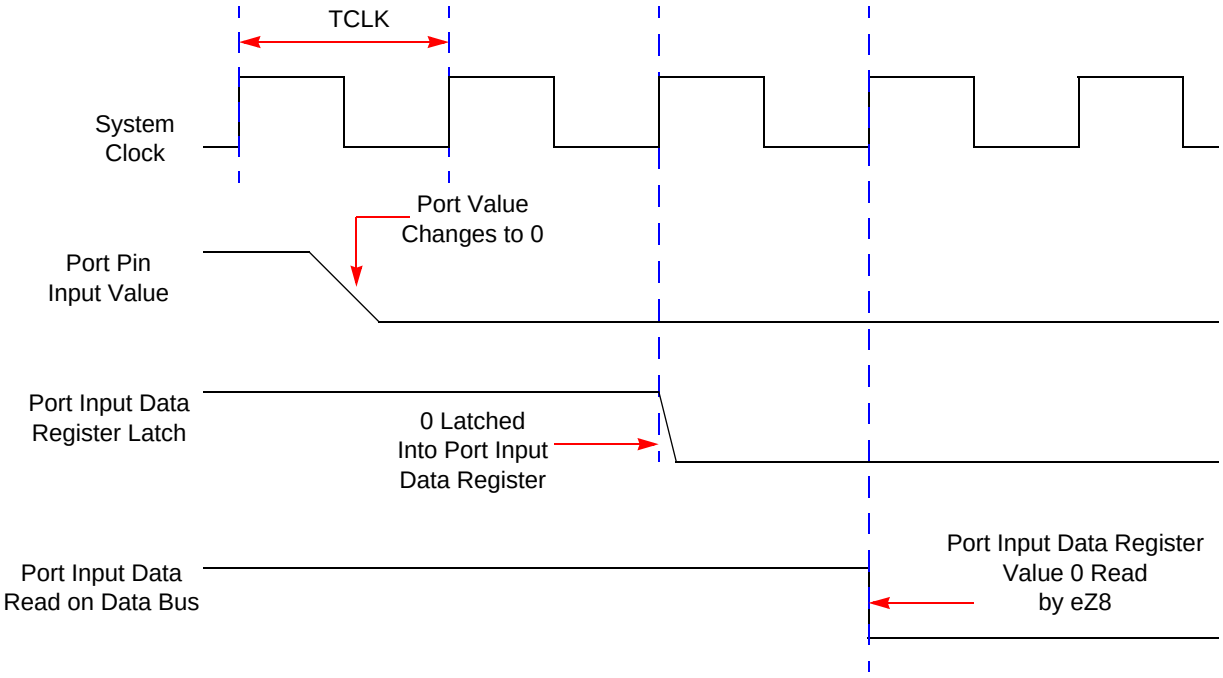

Figure 34. Port Input Sample Timing

Table 139. GPIO Port Input Timing

		Delay (ns)	
Parameter	Abbreviation	Minimum	Maximum
T_{S_PORT}	Port Input Transition to XIN Rise Setup Time (Not pictured)	5	–
T_{H_PORT}	XIN Rise to Port Input Transition Hold Time (Not pictured)	0	–
T_{SMR}	GPIO Port Pin Pulse Width to ensure Stop Mode Recovery (for GPIO Port Pins enabled as SMR sources)	1 µs	

S