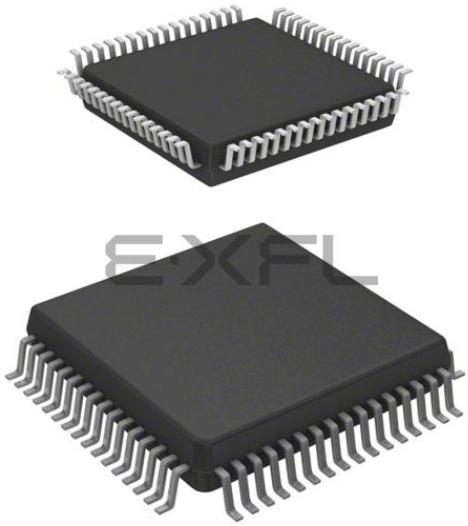

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, PWM, WDT
Number of I/O	58
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x6b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mke04z64vqh4

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to **nxp.com** and perform a part number search for the following device numbers: KE06Z.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q KE## A FFF R T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KE##	Kinetis family	• KE04
A	Key attribute	• Z = M0+ core
FFF	Program flash memory size	• 128 = 128 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LD = 44 LQFP (10 mm x 10 mm)

Table continues on the next page...

Field	Description	Values
		• QH = 64 QFP (14 mm x 14 mm) • LH = 64 LQFP (10 mm x 10 mm) • LK = 80 LQFP (14 mm x 14 mm)
CC	Maximum CPU frequency (MHz)	• 4 = 48 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

MKE06Z128VLK4

3 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 1. Parameter classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–6000	+6000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 125°C	–100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78D, *IC Latch-up Test*.
   - Test was performed at 125 °C case temperature (Class II).
   - I/O pins pass ±100 mA I-test with I_{DD} current limit at 400 mA.
   - I/O pins pass +50/-100 mA I-test with I_{DD} current limit at 1000 mA.
   - Supply groups pass 1.5 V_{ccmax}.
   - $\overline{\text{RESET}}$ pin was only tested with negative I-test due to product conditioning requirement.

2. Only PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0 (64-pin and 80-pin packages only), and PTH1 (64-pin and 80-pin packages only) support high current output.
3. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
4. All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD}. PTA2 and PTA3 are true open drain I/O pins that are internally clamped to V_{SS}.
5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger value.
6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is higher than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as when no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 4. LVD and POR specification

Symbol	C	Description		Min	Typ	Max	Unit
V_{POR}	D	POR re-arm voltage[1]		1.5	1.75	2.0	V
V_{LVDH}	C	Falling low-voltage detect threshold—high range (LVDV = 1)[2]		4.2	4.3	4.4	V
V_{LVW1H}	C	Falling low-voltage warning threshold—high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V_{LVW2H}	C		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V_{LVW3H}	C		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V_{LVW4H}	C		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V_{HYSH}	C	High range low-voltage detect/warning hysteresis		—	100	—	mV
V_{LVDL}	C	Falling low-voltage detect threshold—low range (LVDV = 0)		2.56	2.61	2.66	V
V_{LVW1L}	C	Falling low-voltage warning threshold—low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V_{LVW2L}	C		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V_{LVW3L}	C		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V_{LVW4L}	C		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V_{HYSDL}	C	Low range low-voltage detect hysteresis		—	40	—	mV
V_{HYSWL}	C	Low range low-voltage warning hysteresis		—	80	—	mV
V_{BG}	P	Buffered bandgap output [3]		1.14	1.16	1.18	V

1. Maximum is highest voltage that POR is guaranteed.
2. Rising thresholds are falling threshold + hysteresis.
3. voltage Factory trimmed at V_{DD} = 5.0 V, Temp = 25 °C

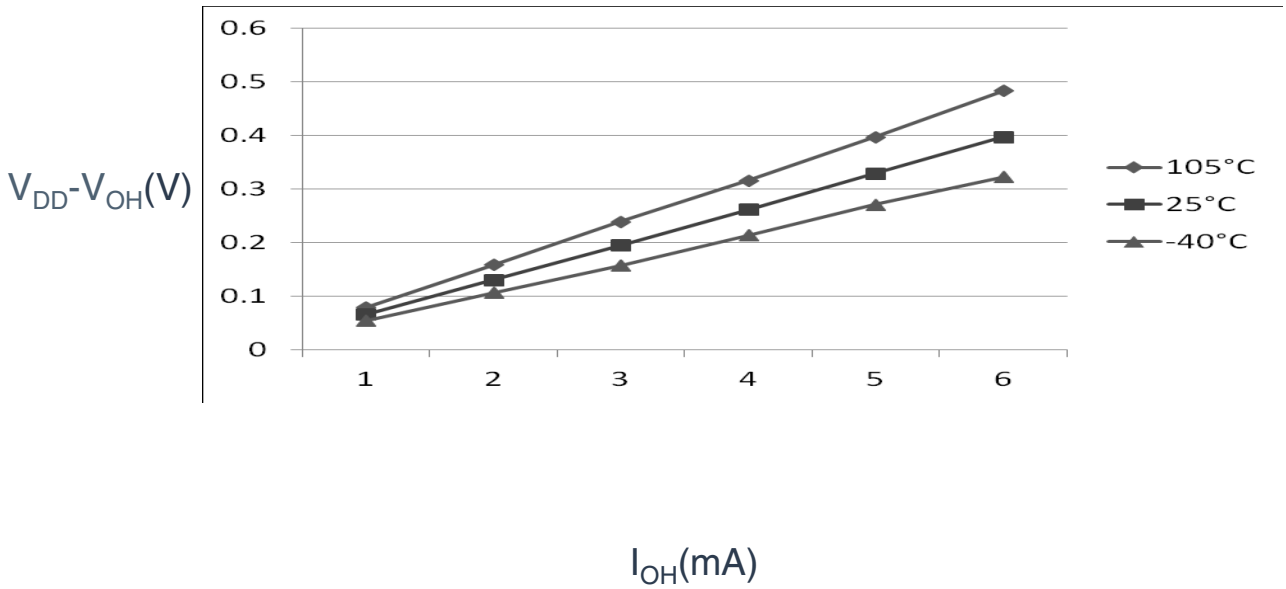


Figure 1. Typical V_{DD}-V_{OH} Vs. I_{OH} (standard drive strength) (V_{DD} = 5 V)

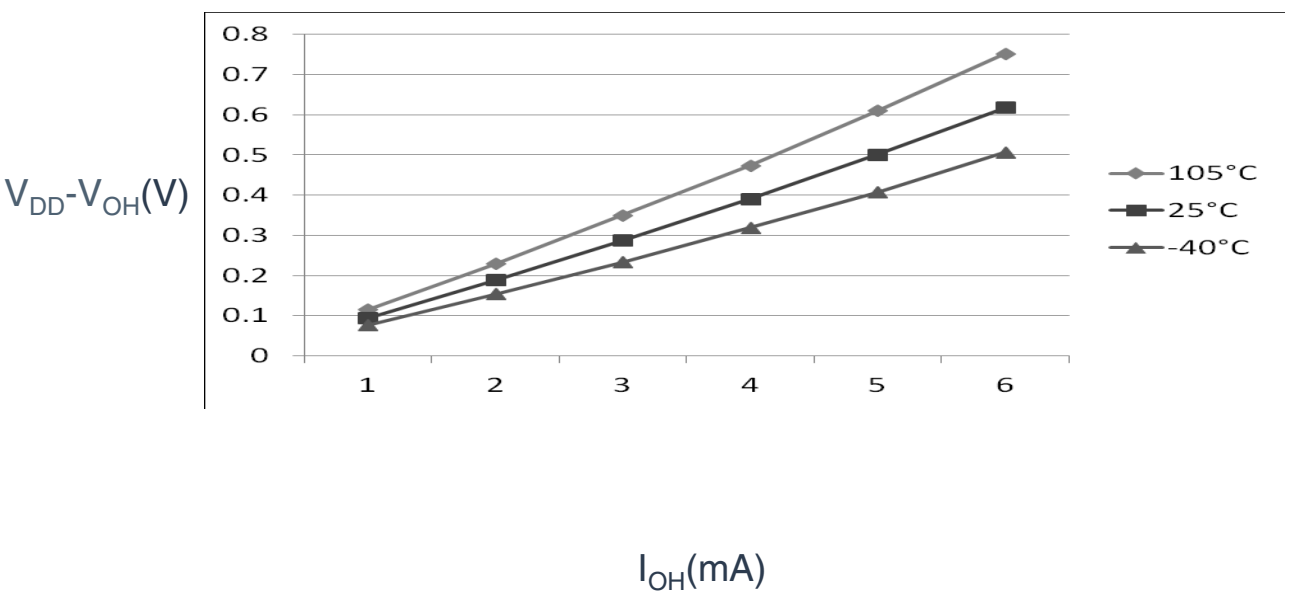


Figure 2. Typical V_{DD}-V_{OH} Vs. I_{OH} (standard drive strength) (V_{DD} = 3 V)

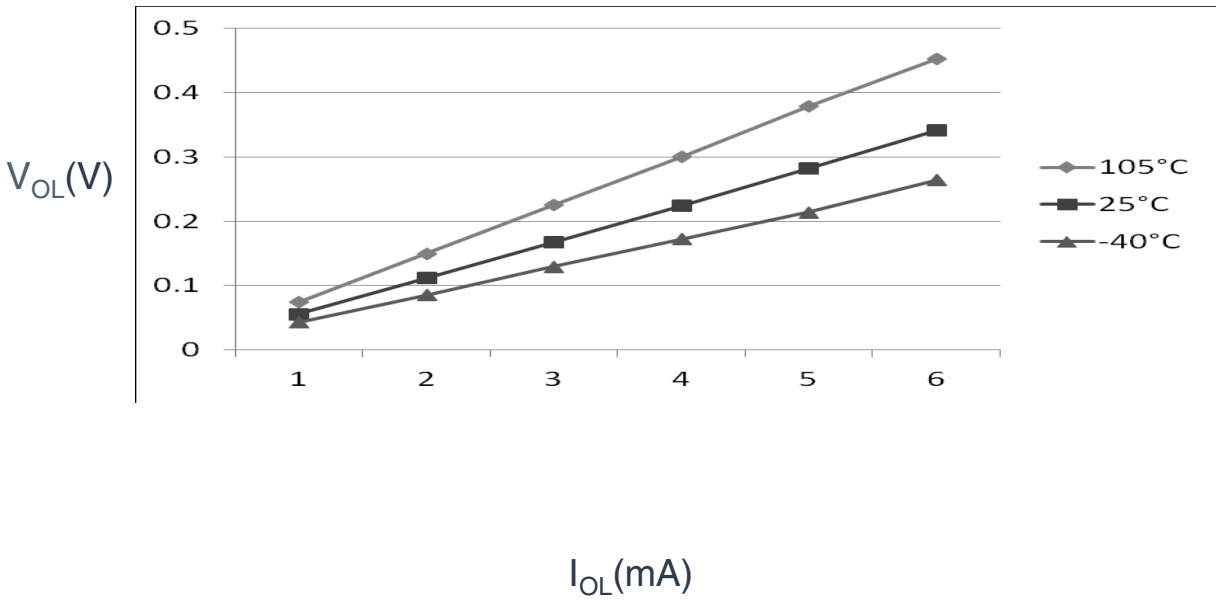


Figure 5. Typical V_{OL} Vs. I_{OL} (standard drive strength) (V_{DD} = 5 V)

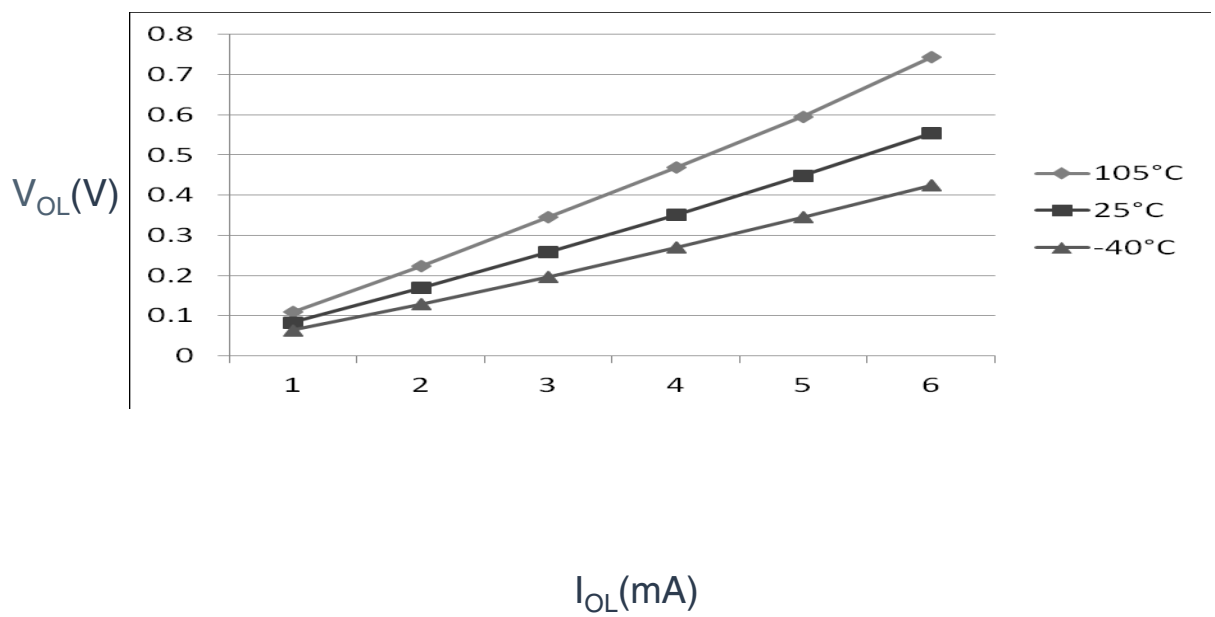


Figure 6. Typical V_{OL} Vs. I_{OL} (standard drive strength) (V_{DD} = 3 V)

5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 5. Supply current characteristics

C	Parameter	Symbol	Core/Bus Freq	V_{DD} (V)	Typical[1]	Max[2]	Unit	Temp
C	Run supply current FEI mode, all modules clocks enabled; run from flash	RI_{DD}	48/24 MHz	5	11.1	—	mA	-40 to 105 °C
C			24/24 MHz		8	—		
C			12/12 MHz		5	—		
C			1/1 MHz		2.4	—		
C			48/24 MHz	3	11	—		
C			24/24 MHz		7.9	—		
C			12/12 MHz		4.9	—		
			1/1 MHz		2.3	—		
C	Run supply current FEI mode, all modules clocks disabled and gated; run from flash	RI_{DD}	48/24 MHz	5	7.8	—	mA	-40 to 105 °C
C			24/24 MHz		5.5	—		
C			12/12 MHz		3.8	—		
C			1/1 MHz		2.3	—		
C			48/24 MHz	3	7.7	—		
C			24/24 MHz		5.4	—		
C			12/12 MHz		3.7	—		
C			1/1 MHz		2.2	—		
C	Run supply current FBE mode, all modules clocks enabled; run from RAM	RI_{DD}	48/24 MHz	5	14.7	—	mA	-40 to 105 °C
P			24/24 MHz		9.8	14.9		
C			12/12 MHz		6	—		
C			1/1 MHz		2.4	—		
C			48/24 MHz	3	14.6	—		
P			24/24 MHz		9.6	12.8		
C			12/12 MHz		5.9	—		
C			1/1 MHz		2.3	—		
C	Run supply current FBE mode, all modules clocks disabled and gated; run from RAM	RI_{DD}	48/24 MHz	5	11.4	—	mA	-40 to 105 °C
P			24/24 MHz		7.7	12.5		
C			12/12 MHz		4.7	—		
C			1/1 MHz		2.3	—		
C			48/24 MHz	3	11.3	—		
P			24/24 MHz		7.6	9.5		
C			12/12 MHz		4.6	—		
			1/1 MHz		2.2	—		

Table continues on the next page...

- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

5.1.3.1 EMC radiated emissions operating behaviors

Table 6. EMC radiated emissions operating behaviors for 80-pin LQFP package

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	6	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	6	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	11	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	5	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	N[3]	—	2, 4

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 5.0 V, T_A = 25 °C, f_{OSC} = 8 MHz (crystal), f_{SYS} = 40 MHz, f_{BUS} = 20 MHz
3. IEC/SAE Level Maximums: N≤12 dBµV, M≤18 dBµV, K≤30 dBµV, I ≤36 dBµV, H≤42 dBµV.
4. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

5.2 Switching specifications

5.2.1 Control timing

Table 7. Control timing

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	D	System and core clock		f_{Sys}	DC	—	48	MHz
2	P	Bus frequency (t_{cyc} = 1/f_{Bus})		f_{Bus}	DC	—	24	MHz
3	P	Internal low power oscillator frequency		f_{LPO}	0.67	1.0	1.25	KHz
4	D	External reset pulse width[2]		t_{extrst}	1.5 × t_{cyc}	—	—	ns
5	D	Reset low drive		t_{rstdrv}	34 × t_{cyc}	—	—	ns
6	D	IRQ pulse width	Asynchronous path[2]	t_{ILIH}	100	—	—	ns
	D		Synchronous path[3]	t_{IHIL}	1.5 × t_{cyc}	—	—	ns

Table continues on the next page...

Where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts - chip internal power

$P_{I/O}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$P_D = K \div (T_J + 273\ °C)$

Solving the equations above for K gives:

$K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (P_D)^2$

where K is a constant pertaining to the particular part. K can be determined by measuring P_D (at equilibrium) for an known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 SWD electricals

Table 11. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	5.5	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	24	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	3	—	ns

Table continues on the next page...

Table 11. SWD full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J11	SWD_CLK high to SWD_DIO data valid	—	35	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

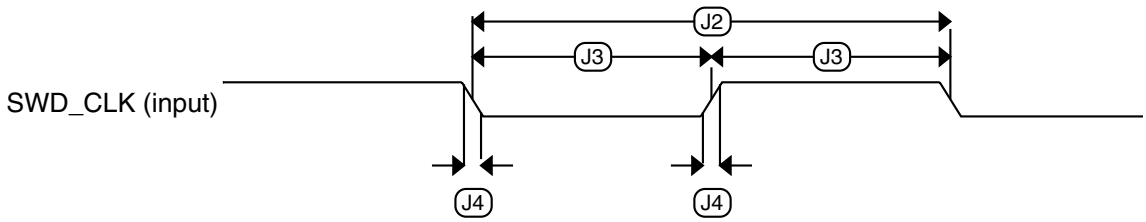


Figure 13. Serial wire clock input timing

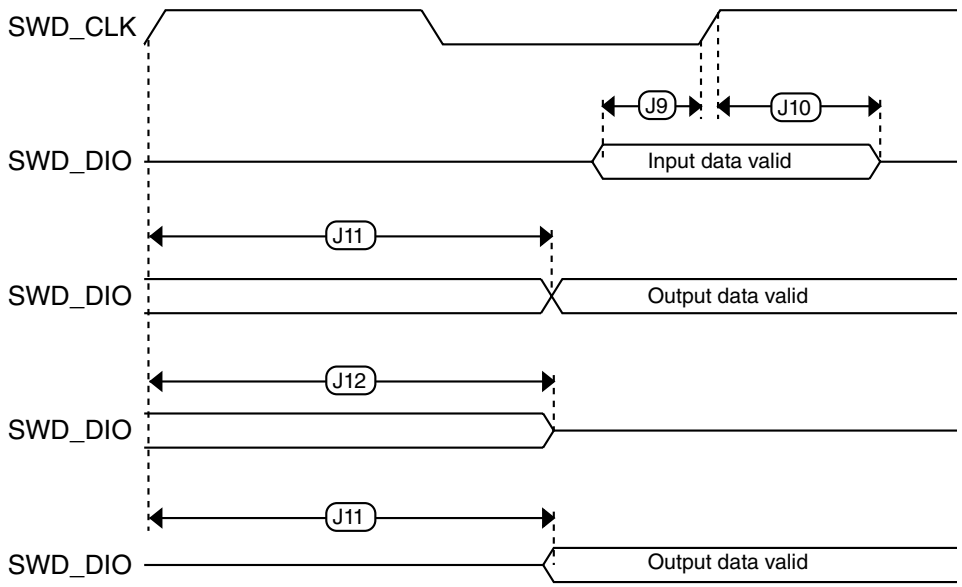


Figure 14. Serial wire data timing

6.2 External oscillator (OSC) and ICS characteristics

Table 12. OSC and ICS specifications (temperature range = -40 to 105 °C ambient)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
1	C	Crystal or resonator frequency	Low range (RANGE = 0)	f_{lo}	31.25	32.768	39.0625	kHz
	C		High range (RANGE = 1)	f_{hi}	4	—	24	MHz

Table continues on the next page...

Table 12. OSC and ICS specifications (temperature range = -40 to 105 °C ambient) (continued)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
2	D	Load capacitors		C1, C2	See Note[2]			
3	D	Feedback resistor	Low Frequency, Low-Power Mode[3]	R_F	—	—	—	MΩ
			Low Frequency, High-Gain Mode		—	10	—	MΩ
			High Frequency, Low-Power Mode		—	1	—	MΩ
			High Frequency, High-Gain Mode		—	1	—	MΩ
4	D	Series resistor - Low Frequency	Low-Power Mode [3]	R_S	—	0	—	kΩ
			High-Gain Mode		—	200	—	kΩ
5	D	Series resistor - High Frequency	Low-Power Mode[3]	R_S	—	0	—	kΩ
	D	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	D		8 MHz		—	0	—	kΩ
	D		16 MHz		—	0	—	kΩ
6	C	Crystal start-up time low range = 32.768 kHz crystal; High range = 20 MHz crystal[4,5]	Low range, low power	t_{CSTL}	—	1000	—	ms
	C		Low range, high gain		—	800	—	ms
	C		High range, low power	t_{CSTH}	—	3	—	ms
	C		High range, high gain		—	1.5	—	ms
7	T	Internal reference start-up time		t_{IRST}	—	20	50	µs
8	P	Internal reference clock (IRC) frequency trim range		f_{int_t}	31.25	—	39.0625	kHz
9	P	Internal reference clock frequency, factory trimmed	T = 25 °C, V_{DD} = 5 V	f_{int_ft}	—	37.5	—	kHz
10	P	DCO output frequency range	FLL reference = fint_t, flo, or fhi/RDIV	f_{dco}	40	—	50	MHz
11	P	Factory trimmed internal oscillator accuracy	T = 25 °C, V_{DD} = 5 V	Δf_{int_ft}	-0.5	—	0.5	%
12	C	Deviation of IRC over temperature when trimmed at T = 25 °C, V_{DD} = 5 V	Over temperature range from -40 °C to 105°C	Δf_{int_t}	-1	—	0.5	%
			Over temperature range from 0 °C to 105°C	Δf_{int_t}	-0.5	—	0.5	
13	C	Frequency accuracy of DCO output using factory trim value	Over temperature range from -40 °C to 105°C	Δf_{dco_ft}	-1.5	—	1	%
			Over temperature range from 0 °C to 105°C	Δf_{dco_ft}	-1	—	1	

Table continues on the next page...

Table 13. Flash characteristics (continued)

C	Characteristic	Symbol	Min[1]	Typical[2]	Max[3]	Unit[4]
D	NVM Bus frequency	f_{NVMBUS}	1	—	24	MHz
D	NVM Operating frequency	f_{NVMOP}	0.8	1	1.05	MHz
D	Erase Verify All Blocks	t_{VFYALL}	—	—	2605	t_{cyc}
D	Erase Verify Flash Block	t_{RD1BLK}	—	—	2579	t_{cyc}
D	Erase Verify Flash Section	t_{RD1SEC}	—	—	485	t_{cyc}
D	Read Once	t_{RDONCE}	—	—	464	t_{cyc}
D	Program Flash (2 word)	t_{PGM2}	0.12	0.13	0.31	ms
D	Program Flash (4 word)	t_{PGM4}	0.21	0.21	0.49	ms
D	Program Once	$t_{PGMONCE}$	0.20	0.21	0.21	ms
D	Erase All Blocks	t_{ERSALL}	95.42	100.18	100.30	ms
D	Erase Flash Block	t_{ERSBLK}	95.42	100.18	100.30	ms
D	Erase Flash Sector	t_{ERSPG}	19.10	20.05	20.09	ms
D	Unsecure Flash	t_{UNSECU}	95.42	100.19	100.31	ms
D	Verify Backdoor Access Key	t_{VFYKEY}	—	—	482	t_{cyc}
D	Set User Margin Level	t_{MLOADU}	—	—	415	t_{cyc}
C	FLASH Program/erase endurance T_L to T_H = -40 °C to 105 °C	n_{FLPE}	10 k	100 k	—	Cycles
C	Data retention at an average junction temperature of T_{Javg} = 85°C after up to 10,000 program/erase cycles	t_{D_ret}	15	100	—	years

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}
2. Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging
4. $t_{cyc} = 1 / f_{NVMBUS}$

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Flash Memory Module section in the reference manual.

6.4 Analog

6.4.1 ADC characteristics

Table 14. 5 V 12-bit ADC operating conditions

Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit	Comment
Reference potential	• Low • High	V_{REFL} V_{REFH}	V_{SSA} $V_{DDA}/2$	— —	$V_{DDA}/2$ V_{DDA}	V	—

Table continues on the next page...

Table 14. 5 V 12-bit ADC operating conditions (continued)

Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
	Delta to V_{DD} (V_{DD}-V_{DDA})	ΔV_{DDA}	-100	0	+100	mV	—
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	—
Input resistance		R_{ADIN}	—	3	5	kΩ	—
Analog source resistance	12-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz	R_{AS}	— —	— —	2 5	kΩ	External to MCU
	10-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz		— —	— —	5 10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

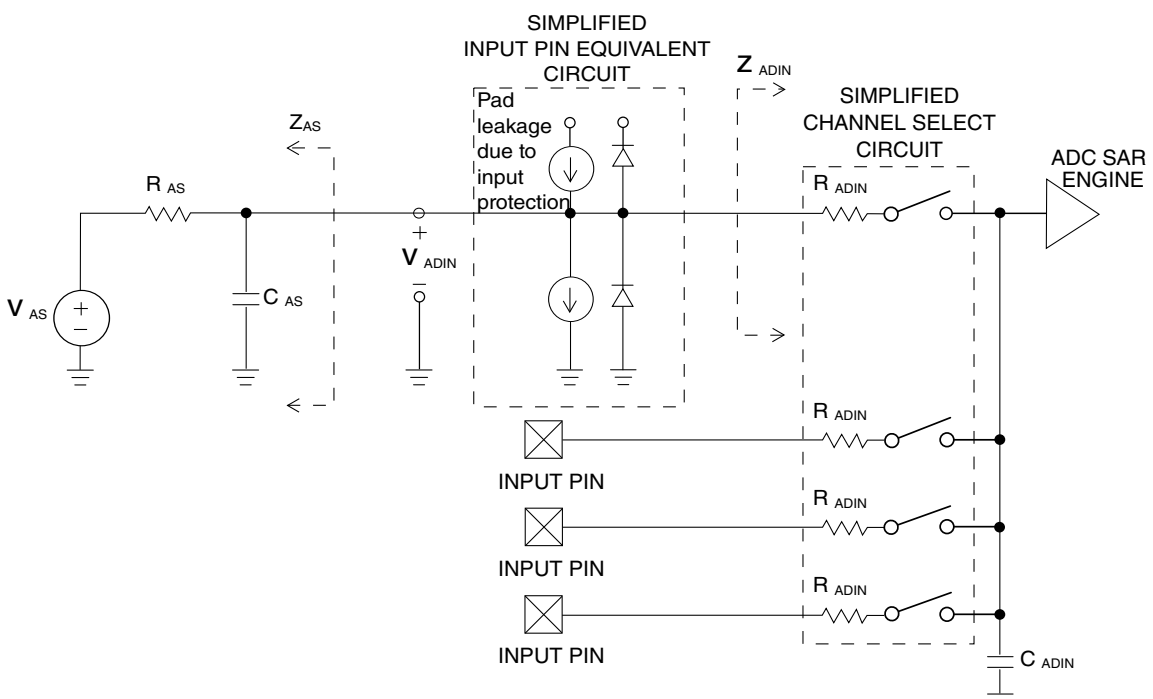


Figure 16. ADC input impedance equivalency diagram

Table 15. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	C	Symbol	Min	Typ[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	133	—	μA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	μA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	μA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	582	990	μA
Supply current	Stop, reset, module off	T	I_{DDA}	—	0.011	1	μA
ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error[2]	12-bit mode	C	E_{TUE}	—	±5.0	—	LSB[3]
	10-bit mode	C		—	±1.5	—	
	8-bit mode	C		—	±0.8	—	
Differential Non-Liniarity	12-bit mode	C	DNL	—	±1.5	—	LSB[3]
	10-bit mode	C		—	±0.4	—	
	8-bit mode	C		—	±0.15	—	
Integral Non-Linearity	12-bit mode	C	INL	—	±1.5	—	LSB[3]
	10-bit mode	C		—	±0.4	—	
	8-bit mode	C		—	±0.15	—	
Zero-scale error[4]	12-bit mode	C	E_{ZS}	—	±1.0	—	LSB[3]
	10-bit mode	C		—	±0.2	—	

Table continues on the next page...

Table 15. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Characteristic	Conditions	C	Symbol	Min	Typ[1]	Max	Unit
	8-bit mode	C		—	±0.35	—	
Full-scale error[5]	12-bit mode	C	E_{FS}	—	±2.5	—	LSB[3]
	10-bit mode	C		—	±0.3	—	
	8-bit mode	C		—	±0.25	—	
Quantization error	≤12 bit modes	D	E_Q	—	—	±0.5	LSB[3]
Input leakage error[6]	all modes	D	E_{IL}	I_{In} * R_{AS}			mV
Temp sensor slope	-40 °C–25 °C	D	m	—	3.266	—	mV/°C
	25 °C–125 °C			—	3.638	—	
Temp sensor voltage	25 °C	D	V_{TEMP25}	—	1.396	—	V

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization
3. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
4. $V_{ADIN} = V_{SSA}$
5. $V_{ADIN} = V_{DDA}$
6. I_{In} = leakage current (refer to DC characteristics)

6.4.2 Analog comparator (ACMP) electricals

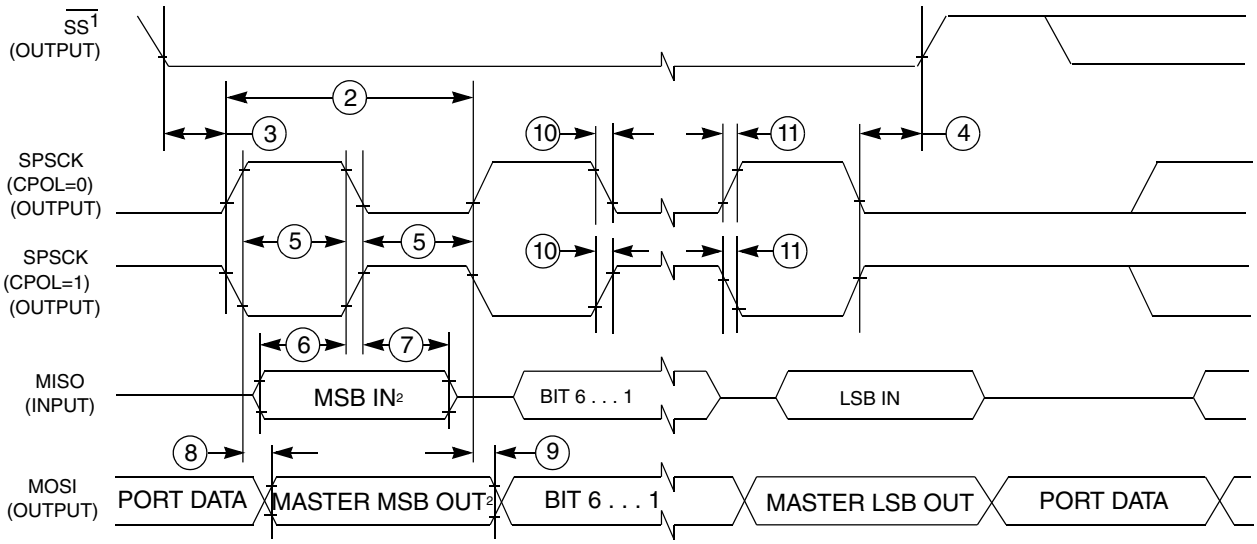
Table 16. Comparator electrical specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DDA}	2.7	—	5.5	V
T	Supply current (Operation mode)	I_{DDA}	—	10	20	µA
D	Analog input voltage	V_{AIN}	V_{SS} - 0.3	—	V_{DDA}	V
P	Analog input offset voltage	V_{AIO}	—	—	40	mV
C	Analog comparator hysteresis (HYST=0)	V_H	—	15	20	mV
C	Analog comparator hysteresis (HYST=1)	V_H	—	20	30	mV
T	Supply current (Off mode)	I_{DDAOFF}	—	60	—	nA
C	Propagation Delay	t_D	—	0.4	1	µs

6.5 Communication interfaces

6.5.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI master mode timing (CPHA=1)

Table 18. SPI slave mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{Bus}/4$	Hz	f_{Bus} is the bus clock as defined in Control timing.
2	t_{SPSCK}	SPSCK period	4 x t_{Bus}	—	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1	—	t_{Bus}	—
4	t_{Lag}	Enable lag time	1	—	t_{Bus}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{Bus} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	25	—	ns	—
8	t_a	Slave access time	—	t_{Bus}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{Bus}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCK edge)	—	25	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{Bus} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

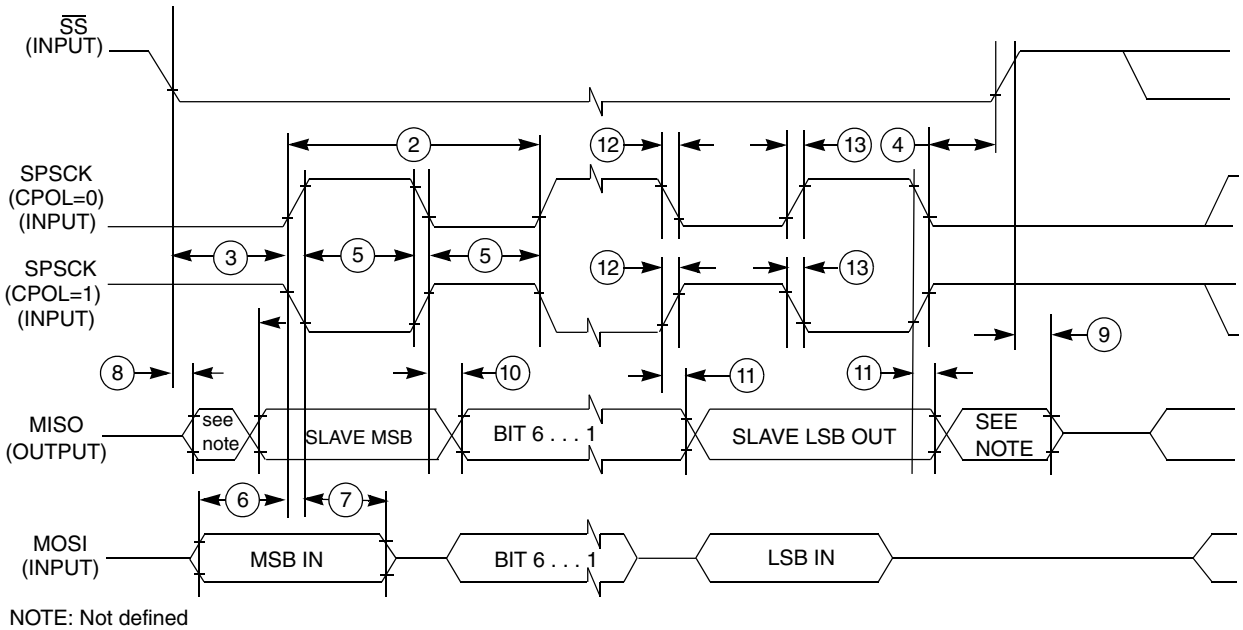


Figure 19. SPI slave mode timing (CPHA = 0)

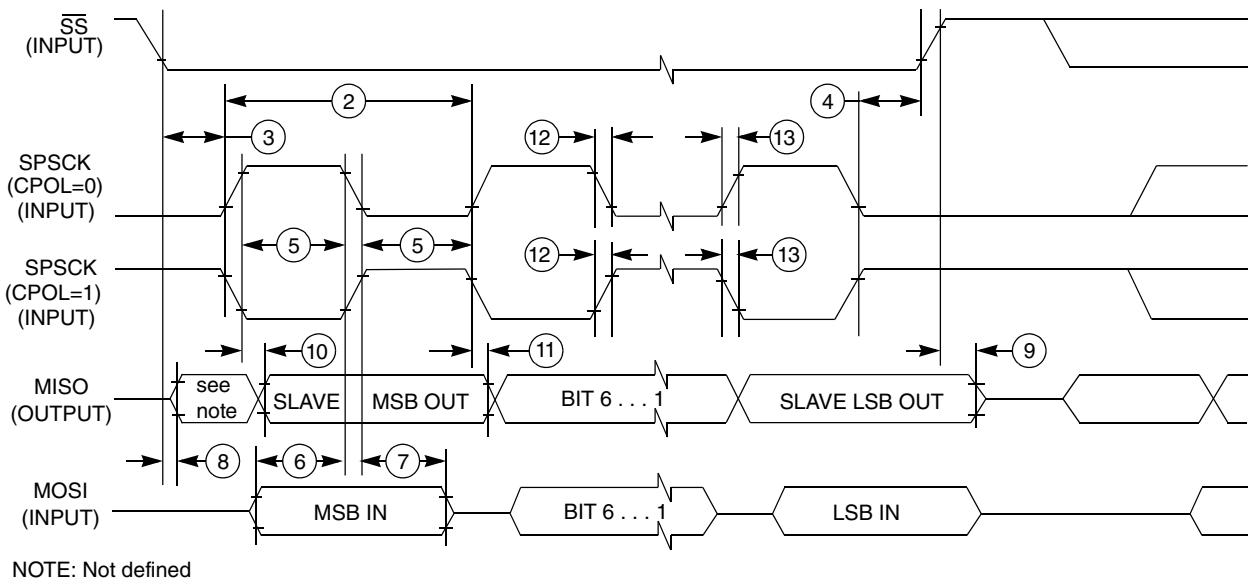


Figure 20. SPI slave mode timing (CPHA=1)

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

80 LQFP	64 LQFP /QFP	44 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
9	8	6	VDDA	VDDA						VREFH	VDDA	
10	—	—	VREFH	VREFH							VREFH	
11	9	7	VREFL	VREFL							VREFL	
12	10	8	VSS/ VSSA	VSS/ VSSA						VSSA	VSS	
13	11	9	PTB7	EXTAL	PTB7	KBI0_P15	I2C0_SCL				EXTAL	
14	12	10	PTB6	XTAL	PTB6	KBI0_P14	I2C0_SDA				XTAL	
15	13	11	PTI4	DISABLED	PTI4		IRQ					
16	—	—	PTI1	DISABLED	PTI1		IRQ	UART2_TX				
17	—	—	PTI0	DISABLED	PTI0		IRQ	UART2_RX				
18	14	—	PTH1	DISABLED	PTH1	KBI1_P25	FTM2_CH1					
19	15	—	PTH0	DISABLED	PTH0	KBI1_P24	FTM2_CH0					
20	16	—	PTE6	DISABLED	PTE6	KBI1_P6						
21	17	—	PTE5	DISABLED	PTE5	KBI1_P5						
22	18	12	PTB5	DISABLED	PTB5	KBI0_P13	FTM2_CH5	SPI0_PCS	ACMP1_OUT			
23	19	13	PTB4	NMI_b	PTB4	KBI0_P12	FTM2_CH4	SPI0_MISO	ACMP1_IN2	NMI_b		
24	20	14	PTC3	ADC0_SE11	PTC3	KBI0_P19	FTM2_CH3		ADC0_SE11			
25	21	15	PTC2	ADC0_SE10	PTC2	KBI0_P18	FTM2_CH2		ADC0_SE10			
26	22	16	PTD7	DISABLED	PTD7	KBI0_P31	UART2_TX					
27	23	17	PTD6	DISABLED	PTD6	KBI0_P30	UART2_RX					
28	24	18	PTD5	DISABLED	PTD5	KBI0_P29	PWT_IN0					
29	—	—	PTI6	DISABLED	PTI6	IRQ						
30	—	—	PTI5	DISABLED	PTI5	IRQ						
31	25	19	PTC1	ADC0_SE9	PTC1	KBI0_P17	FTM2_CH1		ADC0_SE9			
32	26	20	PTC0	ADC0_SE8	PTC0	KBI0_P16	FTM2_CH0		ADC0_SE8			
33	—	—	PTH4	DISABLED	PTH4	KBI1_P28	I2C1_SCL					
34	—	—	PTH3	DISABLED	PTH3	KBI1_P27	I2C1_SDA					
35	27	—	PTF7	ADC0_SE15	PTF7	KBI1_P15			ADC0_SE15			
36	28	—	PTF6	ADC0_SE14	PTF6	KBI1_P14			ADC0_SE14			
37	29	—	PTF5	ADC0_SE13	PTF5	KBI1_P13			ADC0_SE13			
38	30	—	PTF4	ADC0_SE12	PTF4	KBI1_P12			ADC0_SE12			
39	31	21	PTB3	ADC0_SE7	PTB3	KBI0_P11	SPI0_MOSI	FTM0_CH1	ADC0_SE7			
40	32	22	PTB2	ADC0_SE6	PTB2	KBI0_P10	SPI0_SCK	FTM0_CH0	ADC0_SE6			
41	33	23	PTB1	ADC0_SE5	PTB1	KBI0_P9	UART0_TX		ADC0_SE5			
42	34	24	PTB0	ADC0_SE4	PTB0	KBI0_P8	UART0_RX	PWT_IN1	ADC0_SE4			
43	35	—	PTF3	DISABLED	PTF3	KBI1_P11	UART1_TX					
44	36	—	PTF2	DISABLED	PTF2	KBI1_P10	UART1_RX					
45	37	25	PTA7	ADC0_SE3	PTA7	KBI0_P7	FTM2_FLT2	ACMP1_IN1	ADC0_SE3			
46	38	26	PTA6	ADC0_SE2	PTA6	KBI0_P6	FTM2_FLT1	ACMP1_IN0	ADC0_SE2			
47	39	—	PTE4	DISABLED	PTE4	KBI1_P4						
48	40	27	VSS	VSS							VSS	

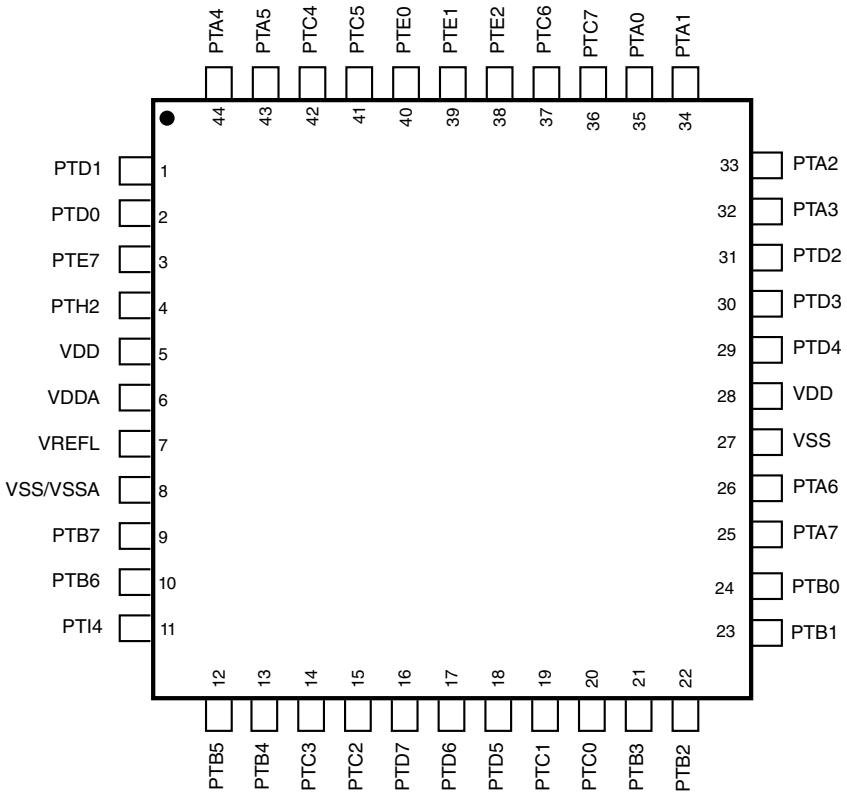


Figure 23. 44-pin LQFP package

9 Revision history

The following table provides a revision history for this document.

Table 19. Revision history

Rev. No.	Date	Substantial Changes
1	12/2013	Initial NDA release.
2	3/2014	Initial public release.
3	5/2014	• Updated the Max. of SI_{DD}. • Updated footnote to the V_{OH}. • Corrected Unit in the FTM input timing table.
4	07/2016	• Added a new section of Thermal operating requirements. • Corrected pinout diagram for 44-pin LQFP in the Device pin assignment.