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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 17x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f524t8adff-30

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products

Group	Part No.	Part No. (for Orders)	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (max.)	Chip Version
RX24T	R5F524TEADFP	R5F524TEADFP#31	PLQP0100KB-B	512 Kbytes	32 Kbytes	8 Kbytes	80 MHz	B
	R5F524TCADFP	R5F524TCADFP#31	PLQP0100KB-B	384 Kbytes				
	R5F524TBADFP	R5F524TBADFP#31	PLQP0100KB-B	256 Kbytes				
	R5F524TAADFP	R5F524TAADFP#31	PLQP0100KB-B	256 Kbytes	16 Kbytes	8 Kbytes	80 MHz	A
	R5F524TAADFF	R5F524TAADFF#31	PLQP0080JA-A					
	R5F524TAADFN	R5F524TAADFN#31	PLQP0080KB-B					
	R5F524TAADFM	R5F524TAADFM#31	PLQP0064KB-C					
	R5F524T8ADFP	R5F524T8ADFP#31	PLQP0100KB-B	128 Kbytes				
	R5F524T8ADFF	R5F524T8ADFF#31	PLQP0080JA-A					
	R5F524T8ADFN	R5F524T8ADFN#31	PLQP0080KB-B					
	R5F524T8ADFM	R5F524T8ADFM#31	PLQP0064KB-C					

Note: The part numbers for orders above are used for products in mass production or under development when this manual is issued. Refer to the Renesas Electronics Corporation website for the latest part numbers.

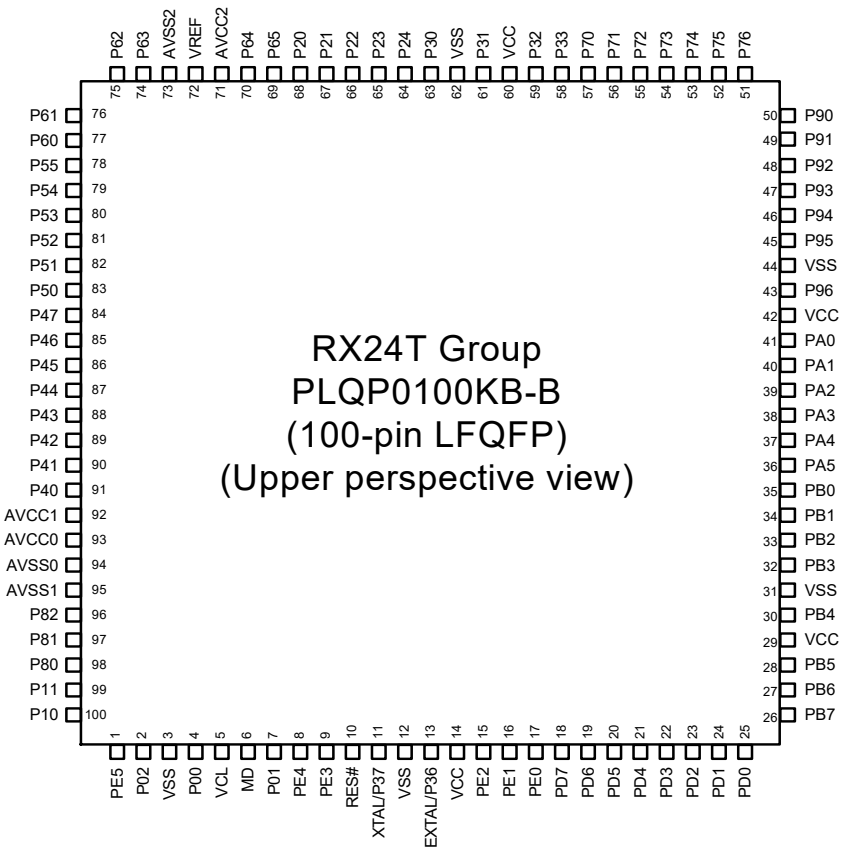
Table 1.4 Pin Functions (4/4)

Classifications	Pin Name	I/O	Description
I/O ports	P00 to P02	I/O	3-bit input/output pins.
	P10, P11	I/O	2-bit input/output pins.
	P20 to P24	I/O	5-bit input/output pins.
	P30 to P33, P36, P37	I/O	6-bit input/output pins.
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P55	I/O	6-bit input/output pins.
	P60 to P65	I/O	6-bit input/output pins.
	P70 to P76	I/O	7-bit input/output pins.
	P80 to P82	I/O	3-bit input/output pins.
	P90 to P96	I/O	7-bit input/output pins.
	PA0 to PA5	I/O	6-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE5	I/O	6-bit input/output pins (PE2: input).

Note: When the A/D converter, D/A converter, and comparator C are not used, connect the AVCC0, AVCC1, AVCC2, and VREF pins to VCC, and connect the AVSS0, AVSS1 and AVSS2 pins to VSS, respectively.

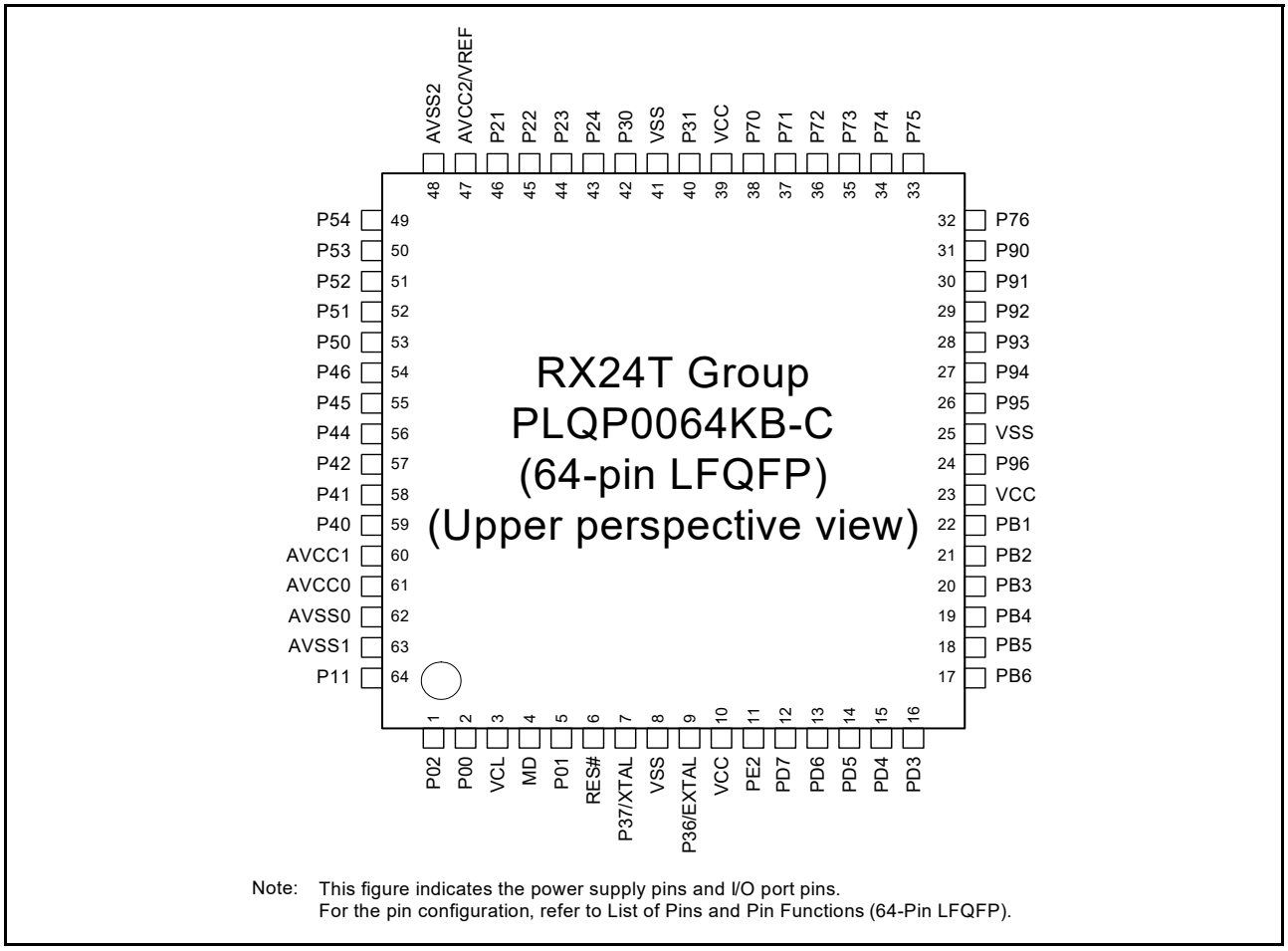
1.5 Pin Assignments

Figure 1.3 to Figure 1.6 shows the pin assignments. Table 1.5 to Table 1.8 shows the lists of pins and pin functions.



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, refer to List of Pins and Pin Functions (100-Pin LFQFP, Chip Version A) or (100-Pin LFQFP, Chip Version B).

Figure 1.3 Pin Assignments of the 100-Pin LFQFP (Chip Version A and B)

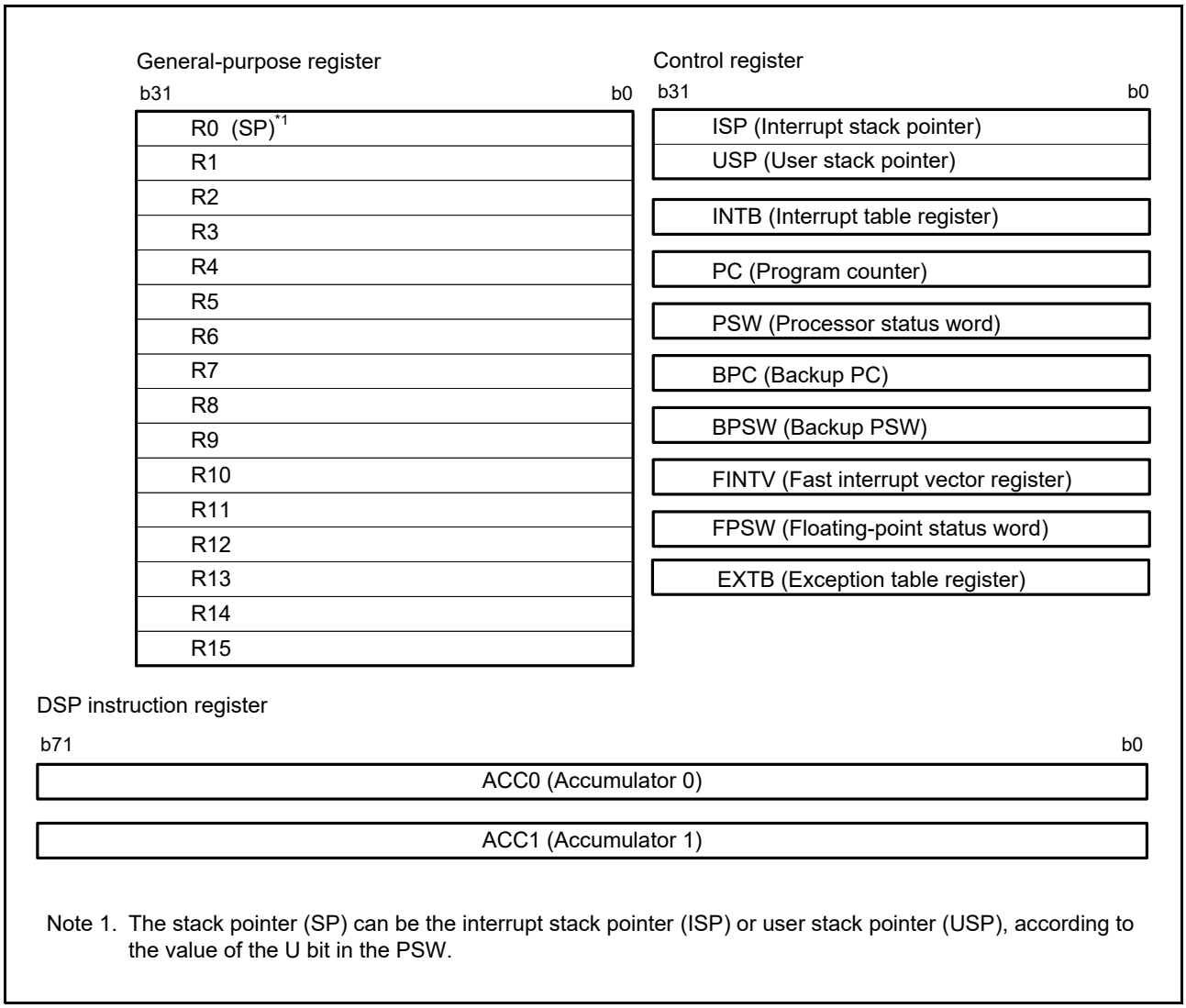


Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, refer to List of Pins and Pin Functions (64-Pin LFQFP).

Figure 1.6 Pin Assignments of the 64-Pin LFQFP

2. CPU

Figure 2.1 shows register set of the CPU.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW.

Figure 2.1 Register Set of the CPU

(9) Floating-point status word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

2.3 Accumulator

The accumulator (ACC0 or ACC1) is a 72-bit register used for DSP instructions. The accumulator is handled as a 96-bit register for reading and writing. At this time, when bits 95 to 72 of the accumulator are read, the value where the value of bit 71 is sign extended is read. Writing to bits 95 to 72 of the accumulator is ignored. ACC0 is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in ACC0 is modified by execution of the instruction.
Use the MVTACGU, MVTACHI, and MVTACLO instructions for writing to the accumulator. The MVTACGU, MVTACHI, and MVTACLO instructions write data to bits 95 to 64, the higher-order 32 bits (bits 63 to 32), and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions for reading data from the accumulator. The MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions read data from the guard bits (bits 95 to 64), higher-order 32 bits (bits 63 to 32), the middle 32 bits (bits 47 to 16), and the lower-order 32 bits (bits 31 to 0), respectively.

Table 4.1 List of I/O Registers (Address Order) (3/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 7043h	ICU	Interrupt Request Register 067	IR067	8	8	2 ICLK
0008 7044h	ICU	Interrupt Request Register 068	IR068	8	8	2 ICLK
0008 7045h	ICU	Interrupt Request Register 069	IR069	8	8	2 ICLK
0008 7046h	ICU	Interrupt Request Register 070	IR070	8	8	2 ICLK
0008 7047h	ICU	Interrupt Request Register 071	IR071	8	8	2 ICLK
0008 7058h	ICU	Interrupt Request Register 088	IR088	8	8	2 ICLK
0008 7059h	ICU	Interrupt Request Register 089	IR089	8	8	2 ICLK
0008 7062h	ICU	Interrupt Request Register 098*2	IR098	8	8	2 ICLK
0008 7063h	ICU	Interrupt Request Register 099*2	IR099	8	8	2 ICLK
0008 7064h	ICU	Interrupt Request Register 100*2	IR100	8	8	2 ICLK
0008 7065h	ICU	Interrupt Request Register 101*2	IR101	8	8	2 ICLK
0008 7066h	ICU	Interrupt Request Register 102	IR102	8	8	2 ICLK
0008 7067h	ICU	Interrupt Request Register 103	IR103	8	8	2 ICLK
0008 7068h	ICU	Interrupt Request Register 104	IR104	8	8	2 ICLK
0008 7069h	ICU	Interrupt Request Register 105	IR105	8	8	2 ICLK
0008 706Ah	ICU	Interrupt Request Register 106	IR106	8	8	2 ICLK
0008 706Bh	ICU	Interrupt Request Register 107	IR107	8	8	2 ICLK
0008 706Ch	ICU	Interrupt Request Register 108	IR108	8	8	2 ICLK
0008 706Dh	ICU	Interrupt Request Register 109	IR109	8	8	2 ICLK
0008 706Eh	ICU	Interrupt Request Register 110	IR110	8	8	2 ICLK
0008 706Fh	ICU	Interrupt Request Register 111	IR111	8	8	2 ICLK
0008 7070h	ICU	Interrupt Request Register 112	IR112	8	8	2 ICLK
0008 7071h	ICU	Interrupt Request Register 113	IR113	8	8	2 ICLK
0008 7072h	ICU	Interrupt Request Register 114	IR114	8	8	2 ICLK
0008 7073h	ICU	Interrupt Request Register 115	IR115	8	8	2 ICLK
0008 7074h	ICU	Interrupt Request Register 116	IR116	8	8	2 ICLK
0008 7075h	ICU	Interrupt Request Register 117	IR117	8	8	2 ICLK
0008 7076h	ICU	Interrupt Request Register 118	IR118	8	8	2 ICLK
0008 7077h	ICU	Interrupt Request Register 119	IR119	8	8	2 ICLK
0008 7078h	ICU	Interrupt Request Register 120	IR120	8	8	2 ICLK
0008 7079h	ICU	Interrupt Request Register 121	IR121	8	8	2 ICLK
0008 707Ah	ICU	Interrupt Request Register 122	IR122	8	8	2 ICLK
0008 707Bh	ICU	Interrupt Request Register 123	IR123	8	8	2 ICLK
0008 707Ch	ICU	Interrupt Request Register 124	IR124	8	8	2 ICLK
0008 707Dh	ICU	Interrupt Request Register 125	IR125	8	8	2 ICLK
0008 707Eh	ICU	Interrupt Request Register 126	IR126	8	8	2 ICLK
0008 707Fh	ICU	Interrupt Request Register 127	IR127	8	8	2 ICLK
0008 7080h	ICU	Interrupt Request Register 128	IR128	8	8	2 ICLK
0008 7081h	ICU	Interrupt Request Register 129	IR129	8	8	2 ICLK
0008 7082h	ICU	Interrupt Request Register 130	IR130	8	8	2 ICLK
0008 7083h	ICU	Interrupt Request Register 131	IR131	8	8	2 ICLK
0008 7084h	ICU	Interrupt Request Register 132	IR132	8	8	2 ICLK
0008 7085h	ICU	Interrupt Request Register 133	IR133	8	8	2 ICLK
0008 7086h	ICU	Interrupt Request Register 134	IR134	8	8	2 ICLK
0008 7087h	ICU	Interrupt Request Register 135	IR135	8	8	2 ICLK
0008 7088h	ICU	Interrupt Request Register 136	IR136	8	8	2 ICLK
0008 7089h	ICU	Interrupt Request Register 137	IR137	8	8	2 ICLK
0008 708Ah	ICU	Interrupt Request Register 138	IR138	8	8	2 ICLK
0008 708Bh	ICU	Interrupt Request Register 139	IR139	8	8	2 ICLK
0008 708Ch	ICU	Interrupt Request Register 140	IR140	8	8	2 ICLK
0008 708Dh	ICU	Interrupt Request Register 141	IR141	8	8	2 ICLK
0008 708Eh	ICU	Interrupt Request Register 142	IR142	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (9/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 733Fh	ICU	Interrupt Source Priority Register 063*2	IPR063	8	8	2 ICLK
0008 7340h	ICU	Interrupt Source Priority Register 064	IPR064	8	8	2 ICLK
0008 7341h	ICU	Interrupt Source Priority Register 065	IPR065	8	8	2 ICLK
0008 7342h	ICU	Interrupt Source Priority Register 066	IPR066	8	8	2 ICLK
0008 7343h	ICU	Interrupt Source Priority Register 067	IPR067	8	8	2 ICLK
0008 7344h	ICU	Interrupt Source Priority Register 068	IPR068	8	8	2 ICLK
0008 7345h	ICU	Interrupt Source Priority Register 069	IPR069	8	8	2 ICLK
0008 7346h	ICU	Interrupt Source Priority Register 070	IPR070	8	8	2 ICLK
0008 7347h	ICU	Interrupt Source Priority Register 071	IPR071	8	8	2 ICLK
0008 7358h	ICU	Interrupt Source Priority Register 088	IPR088	8	8	2 ICLK
0008 7359h	ICU	Interrupt Source Priority Register 089	IPR089	8	8	2 ICLK
0008 7362h	ICU	Interrupt Source Priority Register 098*2	IPR098	8	8	2 ICLK
0008 7363h	ICU	Interrupt Source Priority Register 099*2	IPR099	8	8	2 ICLK
0008 7364h	ICU	Interrupt Source Priority Register 100*2	IPR100	8	8	2 ICLK
0008 7365h	ICU	Interrupt Source Priority Register 101*2	IPR101	8	8	2 ICLK
0008 7366h	ICU	Interrupt Source Priority Register 102	IPR102	8	8	2 ICLK
0008 7367h	ICU	Interrupt Source Priority Register 103	IPR103	8	8	2 ICLK
0008 7368h	ICU	Interrupt Source Priority Register 104	IPR104	8	8	2 ICLK
0008 7369h	ICU	Interrupt Source Priority Register 105	IPR105	8	8	2 ICLK
0008 736Ah	ICU	Interrupt Source Priority Register 106	IPR106	8	8	2 ICLK
0008 736Bh	ICU	Interrupt Source Priority Register 107	IPR107	8	8	2 ICLK
0008 736Ch	ICU	Interrupt Source Priority Register 108	IPR108	8	8	2 ICLK
0008 736Dh	ICU	Interrupt Source Priority Register 109	IPR109	8	8	2 ICLK
0008 736Eh	ICU	Interrupt Source Priority Register 110	IPR110	8	8	2 ICLK
0008 736Fh	ICU	Interrupt Source Priority Register 111	IPR111	8	8	2 ICLK
0008 7370h	ICU	Interrupt Source Priority Register 112	IPR112	8	8	2 ICLK
0008 7371h	ICU	Interrupt Source Priority Register 113	IPR113	8	8	2 ICLK
0008 7372h	ICU	Interrupt Source Priority Register 114	IPR114	8	8	2 ICLK
0008 7376h	ICU	Interrupt Source Priority Register 118	IPR118	8	8	2 ICLK
0008 7379h	ICU	Interrupt Source Priority Register 121	IPR121	8	8	2 ICLK
0008 737Bh	ICU	Interrupt Source Priority Register 123	IPR123	8	8	2 ICLK
0008 737Dh	ICU	Interrupt Source Priority Register 125	IPR125	8	8	2 ICLK
0008 737Fh	ICU	Interrupt Source Priority Register 127	IPR127	8	8	2 ICLK
0008 7381h	ICU	Interrupt Source Priority Register 129	IPR129	8	8	2 ICLK
0008 7385h	ICU	Interrupt Source Priority Register 133	IPR133	8	8	2 ICLK
0008 7386h	ICU	Interrupt Source Priority Register 134	IPR134	8	8	2 ICLK
0008 738Ah	ICU	Interrupt Source Priority Register 138	IPR138	8	8	2 ICLK
0008 738Bh	ICU	Interrupt Source Priority Register 139	IPR139	8	8	2 ICLK
0008 738Eh	ICU	Interrupt Source Priority Register 142	IPR142	8	8	2 ICLK
0008 7392h	ICU	Interrupt Source Priority Register 146	IPR146	8	8	2 ICLK
0008 7395h	ICU	Interrupt Source Priority Register 149	IPR149	8	8	2 ICLK
0008 7397h	ICU	Interrupt Source Priority Register 151	IPR151	8	8	2 ICLK
0008 7399h	ICU	Interrupt Source Priority Register 153	IPR153	8	8	2 ICLK
0008 739Fh	ICU	Interrupt Source Priority Register 159	IPR159	8	8	2 ICLK
0008 73A3h	ICU	Interrupt Source Priority Register 163	IPR163	8	8	2 ICLK
0008 73A8h	ICU	Interrupt Source Priority Register 168	IPR168	8	8	2 ICLK
0008 73ADh	ICU	Interrupt Source Priority Register 173	IPR173	8	8	2 ICLK
0008 73AEh	ICU	Interrupt Source Priority Register 174	IPR174	8	8	2 ICLK
0008 73B1h	ICU	Interrupt Source Priority Register 177	IPR177	8	8	2 ICLK
0008 73B4h	ICU	Interrupt Source Priority Register 180	IPR180	8	8	2 ICLK
0008 73B7h	ICU	Interrupt Source Priority Register 183	IPR183	8	8	2 ICLK
0008 73BAh	ICU	Interrupt Source Priority Register 186	IPR186	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (12/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 8227h	TMR5	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB
0008 8228h	TMR4	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8229h	TMR5	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB
0008 822Ah	TMR4	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 822Bh	TMR5	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB
0008 8230h	TMR6	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8231h	TMR7	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8232h	TMR6	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8233h	TMR7	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8234h	TMR6	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8235h	TMR7	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB
0008 8236h	TMR6	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8237h	TMR7	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB
0008 8238h	TMR6	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8239h	TMR7	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB
0008 823Ah	TMR6	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 823Bh	TMR7	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2 or 3 PCLKB
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2 or 3 PCLKB
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2 or 3 PCLKB
0008 8300h	RIIC0	I^2C-bus Control Register 1	ICCR1	8	8	2 or 3 PCLKB
0008 8301h	RIIC0	I^2C-bus Control Register 2	ICCR2	8	8	2 or 3 PCLKB
0008 8302h	RIIC0	I^2C-bus Mode Register 1	ICMR1	8	8	2 or 3 PCLKB
0008 8303h	RIIC0	I^2C-bus Mode Register 2	ICMR2	8	8	2 or 3 PCLKB
0008 8304h	RIIC0	I^2C-bus Mode Register 3	ICMR3	8	8	2 or 3 PCLKB
0008 8305h	RIIC0	I^2C-bus Function Enable Register	ICFER	8	8	2 or 3 PCLKB
0008 8306h	RIIC0	I^2C-bus Status Enable Register	ICSER	8	8	2 or 3 PCLKB
0008 8307h	RIIC0	I^2C-bus Interrupt Enable Register	ICIER	8	8	2 or 3 PCLKB
0008 8308h	RIIC0	I^2C-bus Status Register 1	ICSR1	8	8	2 or 3 PCLKB
0008 8309h	RIIC0	I^2C-bus Status Register 2	ICSR2	8	8	2 or 3 PCLKB
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 or 3 PCLKB
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2 or 3 PCLKB
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2 or 3 PCLKB
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2 or 3 PCLKB
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2 or 3 PCLKB
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2 or 3 PCLKB
0008 8310h	RIIC0	I^2C-bus Bit Rate Low-Level Register	ICBRL	8	8	2 or 3 PCLKB
0008 8311h	RIIC0	I^2C-bus Bit Rate High-Level Register	ICBRH	8	8	2 or 3 PCLKB
0008 8312h	RIIC0	I^2C-bus Transmit Data Register	ICDRT	8	8	2 or 3 PCLKB
0008 8313h	RIIC0	I^2C-bus Receive Data Register	ICDRR	8	8	2 or 3 PCLKB
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2 or 3 PCLKB
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2 or 3 PCLKB
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2 or 3 PCLKB
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2 or 3 PCLKB
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2 or 3 PCLKB
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2 or 3 PCLKB
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2 or 3 PCLKB
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2 or 3 PCLKB
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2 or 3 PCLKB
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2 or 3 PCLKB
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2 or 3 PCLKB
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (16/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 A0AFh	SCI5	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 A0B0h	SCI5	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB
0008 A0B0h	SCI5	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 A0B1h	SCI5	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 A0B2h	SCI5	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 A0C0h	SCI6	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A0C1h	SCI6	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A0C2h	SCI6	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A0C3h	SCI6	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A0C4h	SCI6	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A0C5h	SCI6	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A0C6h	SMCI6	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A0C7h	SCI6	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A0C8h	SCI6	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A0C9h	SCI6	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A0CAh	SCI6	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A0CBh	SCI6	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A0CCh	SCI6	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A0CDh	SCI6	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A0CEh	SCI6	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB
0008 A0CEh	SCI6	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB
0008 A0CFh	SCI6	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 A0D0h	SCI6	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB
0008 A0D0h	SCI6	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 A0D1h	SCI6	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 A0D2h	SCI6	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 B000h	CAC	CAC Control Register 0	CACR0	8	8	2 or 3 PCLKB
0008 B001h	CAC	CAC Control Register 1	CACR1	8	8	2 or 3 PCLKB
0008 B002h	CAC	CAC Control Register 2	CACR2	8	8	2 or 3 PCLKB
0008 B003h	CAC	CAC Interrupt Request Enable Register	CAICR	8	8	2 or 3 PCLKB
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2 or 3 PCLKB
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2 or 3 PCLKB
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2 or 3 PCLKB
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2 or 3 PCLKB
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2 or 3 PCLKB
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2 or 3 PCLKB
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2 or 3 PCLKB
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C004h	PORT4	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C005h	PORT5	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C006h	PORT6	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C007h	PORT7	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C008h	PORT8	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C009h	PORT9	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Ah	PORTA	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Bh	PORTB	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Dh	PORTD	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Eh	PORTE	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C020h	PORT0	Port Output Data Register	PODR	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (29/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
000C 1208h	MTU3	Timer Interrupt Enable Register	TIER	8	8, 16	4 or 5 PCLKA
000C 1209h	MTU4	Timer Interrupt Enable Register	TIER	8	8	4 or 5 PCLKA
000C 120Ah	MTU	Timer Output Master Enable Register A	TOERA	8	8	4 or 5 PCLKA
000C 120Dh	MTU	Timer Gate Control Register	TGCRA	8	8	4 or 5 PCLKA
000C 120Eh	MTU	Timer Output Control Register 1A	TOCR1A	8	8, 16	4 or 5 PCLKA
000C 120Fh	MTU	Timer Output Control Register 2A	TOCR2A	8	8	4 or 5 PCLKA
000C 1210h	MTU3	Timer Counter	TCNT	16	16, 32	4 or 5 PCLKA
000C 1212h	MTU4	Timer Counter	TCNT	16	16	4 or 5 PCLKA
000C 1214h	MTU	Timer Period Data Register A	TCDRA	16	16, 32	4 or 5 PCLKA
000C 1216h	MTU	Timer Dead Time Data Register A	TDDRA	16	16	4 or 5 PCLKA
000C 1218h	MTU3	Timer General Register A	TGRA	16	16, 32	4 or 5 PCLKA
000C 121Ah	MTU3	Timer General Register B	TGRB	16	16	4 or 5 PCLKA
000C 121Ch	MTU4	Timer General Register A	TGRA	16	16, 32	4 or 5 PCLKA
000C 121Eh	MTU4	Timer General Register B	TGRB	16	16	4 or 5 PCLKA
000C 1220h	MTU	Timer Subcounters A	TCNTSA	16	16, 32	4 or 5 PCLKA
000C 1222h	MTU	Timer Period Buffer Register A	TCBRA	16	16	4 or 5 PCLKA
000C 1224h	MTU3	Timer General Register C	TGRC	16	16, 32	4 or 5 PCLKA
000C 1226h	MTU3	Timer General Register D	TGRD	16	16	4 or 5 PCLKA
000C 1228h	MTU4	Timer General Register C	TGRC	16	16, 32	4 or 5 PCLKA
000C 122Ah	MTU4	Timer General Register D	TGRD	16	16	4 or 5 PCLKA
000C 122Ch	MTU3	Timer Status Register	TSR	8	8, 16	4 or 5 PCLKA
000C 122Dh	MTU4	Timer Status Register	TSR	8	8	4 or 5 PCLKA
000C 1230h	MTU	Timer Interrupt Skipping Set Register 1A	TITCR1A	8	8, 16	4 or 5 PCLKA
000C 1231h	MTU	Timer Interrupt Skipping Counters 1A	TITCNT1A	8	8	4 or 5 PCLKA
000C 1232h	MTU	Timer Buffer Transfer Set Register A	TBTERA	8	8	4 or 5 PCLKA
000C 1234h	MTU	Timer Dead Time Enable Register A	TDERA	8	8	4 or 5 PCLKA
000C 1236h	MTU	Timer Output Level Buffer Register A	TOLBRA	8	8	4 or 5 PCLKA
000C 1238h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8, 16	4 or 5 PCLKA
000C 1239h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4 or 5 PCLKA
000C 123Ah	MTU	Timer Interrupt Skipping Mode Register A	TITMRA	8	8	4 or 5 PCLKA
000C 123Bh	MTU	Timer Interrupt Skipping Set Register 2A	TITCR2A	8	8	4 or 5 PCLKA
000C 123Ch	MTU	Timer Interrupt Skipping Counters 2A	TITCNT2A	8	8	4 or 5 PCLKA
000C 1240h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	4 or 5 PCLKA
000C 1244h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16, 32	4 or 5 PCLKA
000C 1246h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	4 or 5 PCLKA
000C 1248h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16, 32	4 or 5 PCLKA
000C 124Ah	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	4 or 5 PCLKA
000C 124Ch	MTU3	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA
000C 124Dh	MTU4	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA
000C 1260h	MTU	Timer Waveform Control Register A	TWCRA	8	8	4 or 5 PCLKA
000C 1270h	MTU	Timer Mode Register 2A	TMDR2A	8	8	4 or 5 PCLKA
000C 1272h	MTU3	Timer General Register E	TGRE	16	16	4 or 5 PCLKA
000C 1274h	MTU4	Timer General Register E	TGRE	16	16	4 or 5 PCLKA
000C 1276h	MTU4	Timer General Register F	TGRF	16	16	4 or 5 PCLKA
000C 1280h	MTU	Timer Start Register A	TSTRA	8	8, 16	4 or 5 PCLKA
000C 1281h	MTU	Timer Synchronous Register A	TSYRA	8	8	4 or 5 PCLKA
000C 1282h	MTU	Timer Counter Synchronous Start Register	TCSYSTR	8	8	4 or 5 PCLKA
000C 1284h	MTU	Timer Read/Write Enable Register A	TRWERA	8	8	4 or 5 PCLKA
000C 1290h	MTU0	Noise Filter Control Register 0	NFCR0	8	8	4 or 5 PCLKA
000C 1291h	MTU1	Noise Filter Control Register 1	NFCR1	8	8	4 or 5 PCLKA
000C 1292h	MTU2	Noise Filter Control Register 2	NFCR2	8	8	4 or 5 PCLKA

Table 4.1 List of I/O Registers (Address Order) (30/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000C 1293h	MTU3	Noise Filter Control Register 3	NFCR3	8	8	4 or 5 PCLKA
000C 1294h	MTU4	Noise Filter Control Register 4	NFCR4	8	8	4 or 5 PCLKA
000C 1296h	MTU9	Noise Filter Control Register 9	NFCR9	8	8	4 or 5 PCLKA
000C 1299h	MTU0	Noise Filter Control Register C	NFCRC	8	8	4 or 5 PCLKA
000C 1300h	MTU0	Timer Control Register	TCR	8	8, 16, 32	4 or 5 PCLKA
000C 1301h	MTU0	Timer Mode Register 1	TMDR1	8	8	4 or 5 PCLKA
000C 1302h	MTU0	Timer I/O Control Register H	TIORH	8	8, 16	4 or 5 PCLKA
000C 1303h	MTU0	Timer I/O Control Register L	TIORL	8	8	4 or 5 PCLKA
000C 1304h	MTU0	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4 or 5 PCLKA
000C 1306h	MTU0	Timer Counter	TCNT	16	16	4 or 5 PCLKA
000C 1308h	MTU0	Timer General Register A	TGRA	16	16, 32	4 or 5 PCLKA
000C 130Ah	MTU0	Timer General Register B	TGRB	16	16	4 or 5 PCLKA
000C 130Ch	MTU0	Timer General Register C	TGRC	16	16, 32	4 or 5 PCLKA
000C 130Eh	MTU0	Timer General Register D	TGRD	16	16	4 or 5 PCLKA
000C 1320h	MTU0	Timer General Register E	TGRE	16	16, 32	4 or 5 PCLKA
000C 1322h	MTU0	Timer General Register F	TGRF	16	16	4 or 5 PCLKA
000C 1324h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8, 16	4 or 5 PCLKA
000C 1326h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4 or 5 PCLKA
000C 1328h	MTU0	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA
000C 1380h	MTU1	Timer Control Register	TCR	8	8, 16	4 or 5 PCLKA
000C 1381h	MTU1	Timer Mode Register 1	TMDR1	8	8	4 or 5 PCLKA
000C 1382h	MTU1	Timer I/O Control Register	TIOR	8	8	4 or 5 PCLKA
000C 1384h	MTU1	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4 or 5 PCLKA
000C 1385h	MTU1	Timer Status Register	TSR	8	8	4 or 5 PCLKA
000C 1386h	MTU1	Timer Counter	TCNT	16	16	4 or 5 PCLKA
000C 1388h	MTU1	Timer General Register A	TGRA	16	16, 32	4 or 5 PCLKA
000C 138Ah	MTU1	Timer General Register B	TGRB	16	16	4 or 5 PCLKA
000C 1390h	MTU1	Timer Input Capture Control Register	TICCR	8	8	4 or 5 PCLKA
000C 1391h	MTU1	Timer Mode Register 3	TMDR3	8	8	4 or 5 PCLKA
000C 1394h	MTU1	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA
000C 13A0h	MTU1	Timer Longword Counter	TCNTLW	32	32	4 or 5 PCLKA
000C 13A4h	MTU1	Timer Longword General Register	TGRALW	32	32	4 or 5 PCLKA
000C 13A8h	MTU1	Timer Longword General Register	TGRBLW	32	32	4 or 5 PCLKA
000C 1400h	MTU2	Timer Control Register	TCR	8	8, 16	4 or 5 PCLKA
000C 1401h	MTU2	Timer Mode Register 1	TMDR1	8	8	4 or 5 PCLKA
000C 1402h	MTU2	Timer I/O Control Register	TIOR	8	8	4 or 5 PCLKA
000C 1404h	MTU2	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4 or 5 PCLKA
000C 1405h	MTU2	Timer Status Register	TSR	8	8	4 or 5 PCLKA
000C 1406h	MTU2	Timer Counter	TCNT	16	16	4 or 5 PCLKA
000C 1408h	MTU2	Timer General Register A	TGRA	16	16, 32	4 or 5 PCLKA
000C 140Ah	MTU2	Timer General Register B	TGRB	16	16	4 or 5 PCLKA
000C 140Ch	MTU2	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA
000C 1580h	MTU9	Timer Control Register	TCR	8	8, 16, 32	4 or 5 PCLKA
000C 1581h	MTU9	Timer Mode Register 1	TMDR1	8	8	4 or 5 PCLKA
000C 1582h	MTU9	Timer I/O Control Register H	TIORH	8	8, 16	4 or 5 PCLKA
000C 1583h	MTU9	Timer I/O Control Register L	TIORL	8	8	4 or 5 PCLKA
000C 1584h	MTU9	Timer Interrupt Enable Register	TIER	8	8, 16, 32	4 or 5 PCLKA
000C 1586h	MTU9	Timer Counter	TCNT	16	16	4 or 5 PCLKA
000C 1588h	MTU9	Timer General Register A	TGRA	16	16, 32	4 or 5 PCLKA
000C 158Ah	MTU9	Timer General Register B	TGRB	16	16	4 or 5 PCLKA
000C 158Ch	MTU9	Timer General Register C	TGRC	16	16, 32	4 or 5 PCLKA
000C 158Eh	MTU9	Timer General Register D	TGRD	16	16	4 or 5 PCLKA

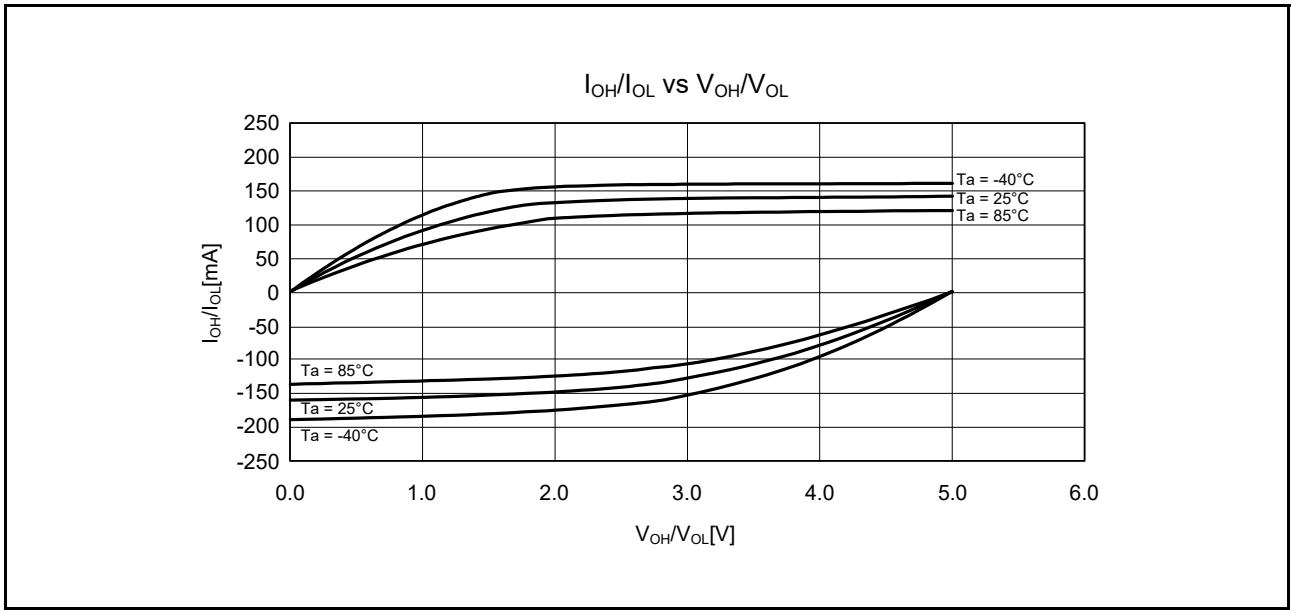


Figure 5.16 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Large Current Ports at VCC = 5.0 V (Reference Data)

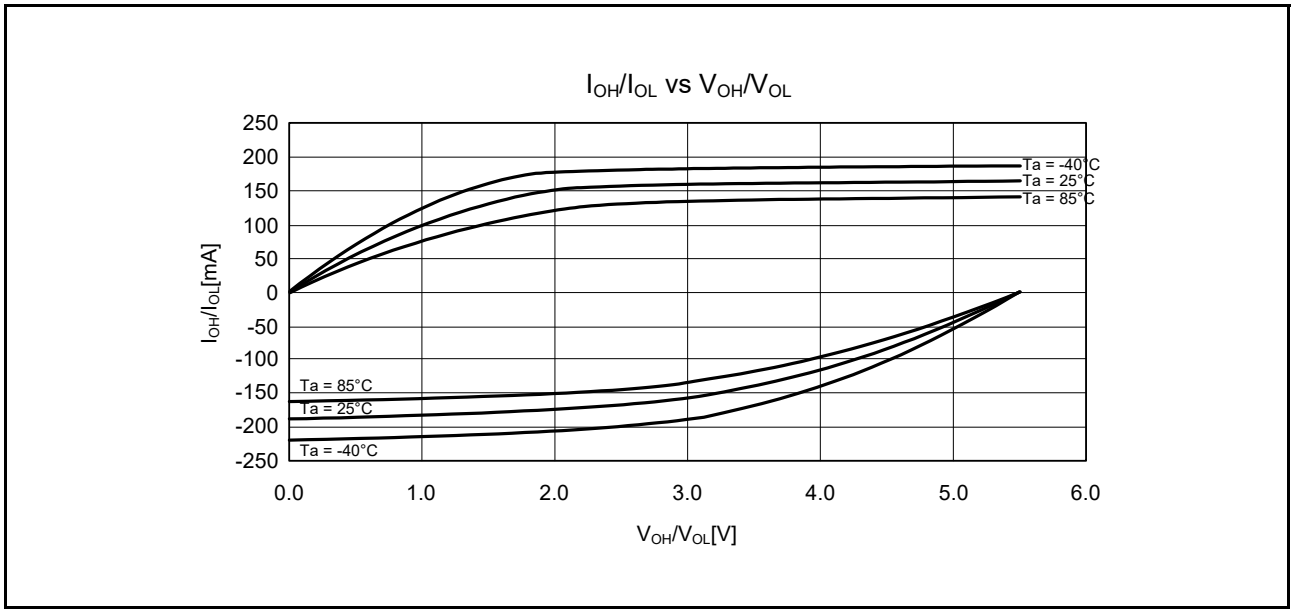


Figure 5.17 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Large Current Ports at VCC = 5.5 V (Reference Data)

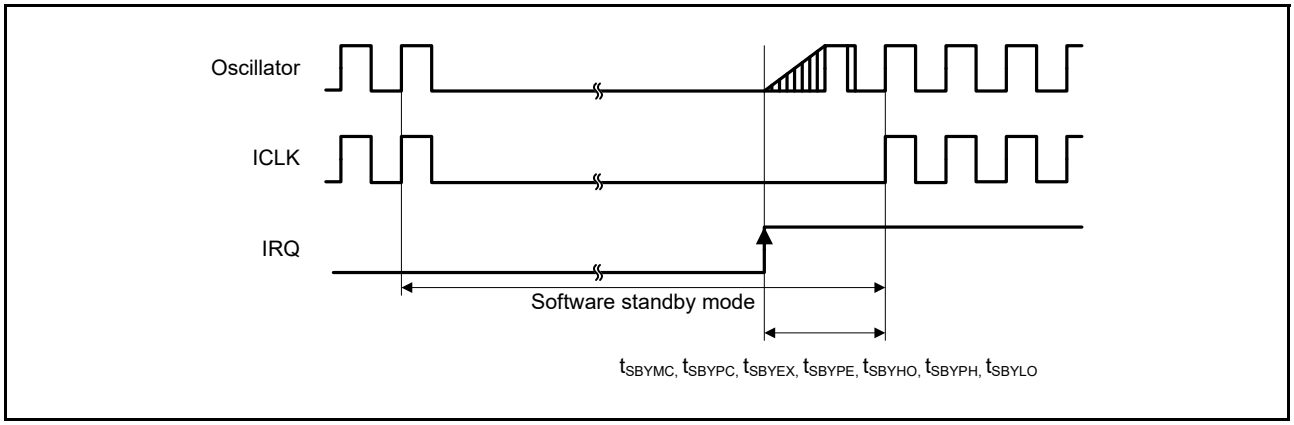


Figure 5.32 Software Standby Mode Recovery Timing

Table 5.20 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	t_{DSLP}	—	2	3.5	µs	Figure 5.33
	Middle-speed mode*3	t_{DSLP}	—	3	4	µs	

Note 1. Oscillators continue oscillating in deep sleep mode.
Note 2. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are 32 MHz.
Note 3. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are 12 MHz.

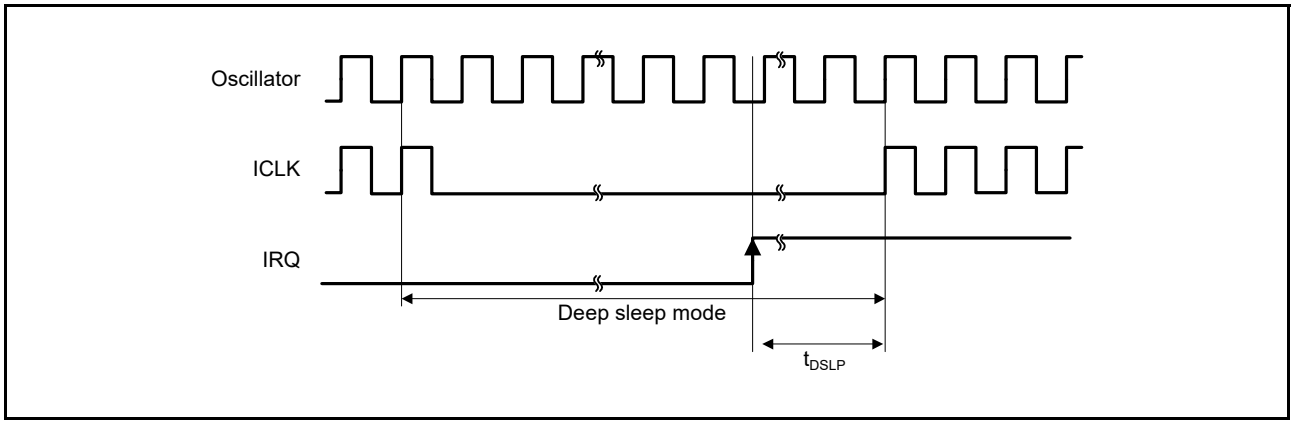


Figure 5.33 Deep Sleep Mode Recovery Timing

Table 5.21 Operating Mode Transition Time

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Mode before Transition	Mode after Transition	ICLK Frequency	Transition Time			Unit
			Min.	Typ.	Max.	
High-speed operating mode	Middle-speed operating modes	8 MHz	—	10	—	µs
Middle-speed operating modes	High-speed operating mode	8 MHz	—	37.5	—	µs

Note: Values when the frequencies of PCLKA, PCLKB, PCLKD, and FCLK are not divided.

Table 5.24 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 =AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C, C = 30pF

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	Figure 5.47
		Slave			6	—		
	RSPCK clock high pulse width	Master	VCC = 4.0 V or above	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 5$	—	ns	
			VCC = 2.7 V or above		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 8$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master	VCC = 4.0 V or above	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 5$	—	ns	
			VCC = 2.7 V or above		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 8$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	VCC = 4.0 V or above	t_{SPCKr}, t_{SPCKf}	—	6	ns	
			VCC = 2.7 V or above		—	10		
		Input			—	0.1	μs/V	
	Data input setup time	Master	VCC = 4.0 V or above	t_{SU}	10	—	ns	Figure 5.48 to Figure 5.51
			VCC = 2.7 V or above		26	—		
		Slave			20	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	0	—		
	SSL setup time	Master		t_{LEAD}	–30 + N*2 × t_{SPcyc}	—	ns	
		Slave			6	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	–30 + N*3 × t_{SPcyc}	—	ns	
		Slave			6	—	t_{Pcyc}	
	Data output delay time	Master	VCC = 4.0 V or above	t_{OD}	—	10	ns	
			VCC = 2.7 V or above		—	14		
		Slave			—	65		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$6 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output		t_{Dr}, t_{Df}	—	10	ns	
		Input			—	1	μs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	10	ns	
		Input			—	1	μs	
	Slave access time			t_{SA}	—	6	t_{Pcyc}	Figure 5.50, Figure 5.51
	Slave output release time			t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

Table 5.26 Timing of On-Chip Peripheral Modules (4)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Standard mode, SMBus)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 5.52
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t_{STAS}	1000	—	ns	
	STOP condition setup time	t_{STOS}	1000	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast mode)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 5.52
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	300	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t_{STAS}	300	—	ns	
	STOP condition setup time	t_{STOS}	300	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. t_{IICcyc}: RIIC internal reference count clock (IICφ) cycle

Note 2. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

5.10 ROM (Flash Memory for Code Storage) Characteristics

Table 5.39 ROM (Flash Memory for Code Storage) Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	—	—	Times	
Data hold time	After 1000 times of N_{PEC}	t_{DRP}	20*2, *3	—	—	Year	T_a = +85°C

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 5.40 ROM (Flash Memory for Code Storage) Characteristics (2): High-Speed Operating Mode

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8-byte	t_{P8}	—	112.0	967.0	—	52.3	490.5	µs
Erasure time	2-Kbyte	t_{E2K}	—	8.7	278.1	—	5.5	214.6	ms
	256-Kbyte (when block erase command used)	t_{E256K}	—	469.1	9813.6	—	41.2	1049.2	ms
	256-Kbyte (when all-block erase command used)	t_{EA256K}	—	463.9	9609.0	—	36.0	839.5	ms
	512-Kbyte (when block erase command used)	t_{E512K}	—	927.8	19218.0	—	72.0	1678.9	ms
	512-Kbyte (when all-block erase command used)	t_{EA512K}	—	922.7	19013.4	—	66.7	1469.2	ms
Blank check time	8-byte	t_{BC8}	—	—	55.0	—	—	16.1	µs
	2-Kbyte	t_{BC2K}	—	—	1840.0	—	—	135.7	µs
Erase operation forcible stop time		t_{SED}	—	—	18.0	—	—	10.7	µs
Start-up area switching setting time		t_{SAS}	—	12.3	566.5	—	6.2	433.5	ms
Access window time		t_{AWS}	—	12.3	566.5	—	6.2	433.5	ms
ROM mode transition wait time 1		t_{DIS}	2.0	—	—	2.0	—	—	µs
ROM mode transition wait time 2		t_{MS}	5.0	—	—	5.0	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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