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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

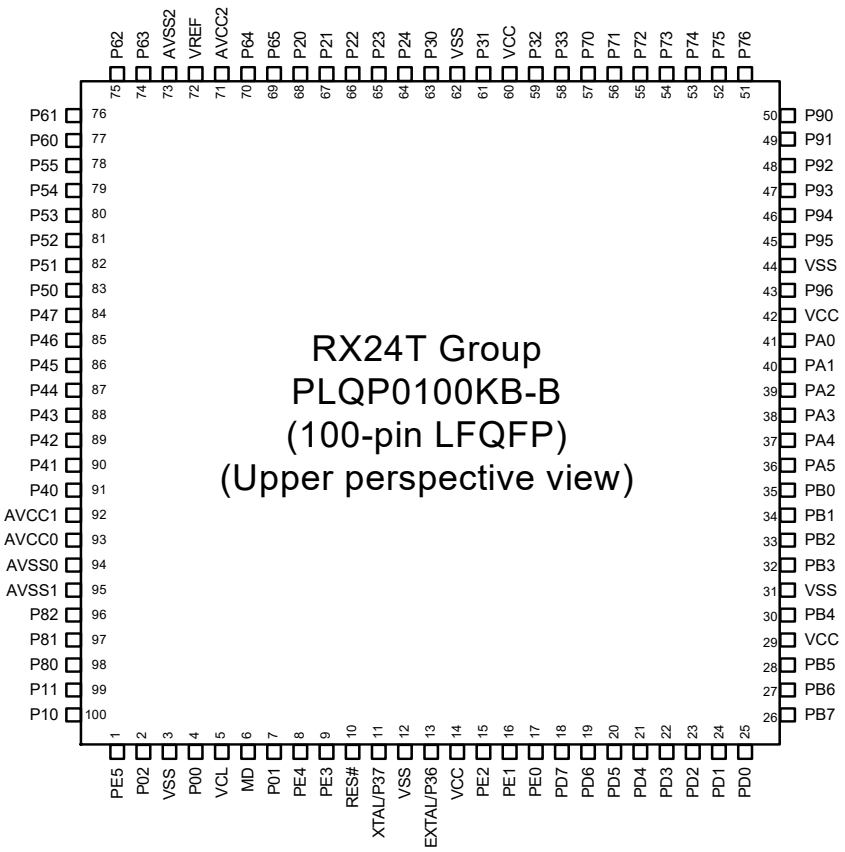
Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 17x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f524t8adff-31

Table 1.4 Pin Functions (3/4)

Classifications	Pin Name	I/O	Description
I²C bus interface (RIICa)	SCL0	I/O	Input/output pin for I²C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA0	I/O	Input/output pin for I²C bus interface data. Bus can be directly driven by the N-channel open drain output.
Serial peripheral interface (RSPIb)	RSPCKA	I/O	Input/output pin for the RSPI clock.
	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master.
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave.
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI.
CAN module (RSCAN)	CRXD0	Input	Input pin
	CTXD0	Output	Output pin
12-bit A/D converter (S12ADF)	AN000 to AN003, AN016, AN100 to AN103, AN116, AN200 to AN211	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADST0, ADST1, ADST2	Output	Output pins for A/D conversion status.
	ADTRG0#, ADTRG1#, ADTRG2#	Input	Input pins for the external trigger signals that start the A/D conversion.
8-bit D/A converter (DAa)	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter
Comparator C (CMPC)	COMP0 to COMP3	Output	Comparator detection result output pins.
	CVREFC0, CVREFC1	Input	Analog reference voltage supply pins for comparator C.
	CMPC00 to CMPC03	Input	Analog input pin for CMPC0
	CMPC10 to CMPC13	Input	Analog input pin for CMPC1
	CMPC20 to CMPC23	Input	Analog input pin for CMPC2
	CMPC30 to CMPC33	Input	Analog input pin for CMPC3
Analog power supply	AVCC0	—	Analog power supply and reference power supply pin for 12-bit A/D converter unit 0. Connect the AVCC0 pin to AVCC1, AVCC2, or VREF when 12-bit A/D converter unit 0 is not used.
	AVSS0	—	Analog ground and reference ground pin for 12-bit A/D converter unit 0. Connect the AVSS0 pin to AVSS1 or AVSS2 when 12-bit A/D converter unit 0 is not used.
	AVCC1	—	Analog power supply and reference power supply pin for 12-bit A/D converter unit 1. Connect the AVCC1 pin to AVCC0, AVCC2, or VREF when 12-bit A/D converter unit 1 is not used.
	AVSS1	—	Analog ground and reference ground pin for 12-bit A/D converter unit 1. Connect the AVSS1 pin to AVSS0 or AVSS2 when 12-bit A/D converter unit 1 is not used.
	AVCC2	—	Analog power supply and reference power supply pin for 12-bit A/D converter unit 2. Connect the AVCC2 pin to AVCC0, AVCC1, or VREF when 12-bit A/D converter unit 2 is not used.
	AVSS2	—	Analog ground and reference ground pin for 12-bit A/D converter unit 2. Analog ground pin for comparator C and 8-bit D/A converter. Connect the AVSS2 pin to AVSS0 or AVSS1 when 12-bit A/D converter unit 2, comparator C and 8-bit D/A converter are not used.
	VREF	—	Analog power supply pin for comparator C and 8-bit D/A converter. For the 64-pin LFQFP package, the VREF pin is internally connected to AVCC2 and is shared. Connect the VREF pin to AVCC0, AVCC1, or AVCC2 when comparator C and 8-bit D/A converter are not used.

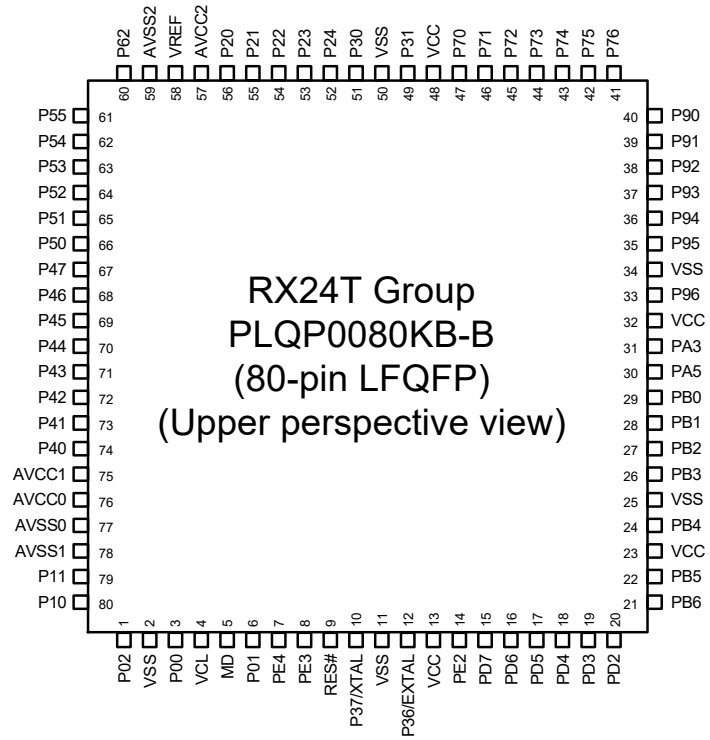
1.5 Pin Assignments

Figure 1.3 to Figure 1.6 shows the pin assignments. Table 1.5 to Table 1.8 shows the lists of pins and pin functions.



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, refer to List of Pins and Pin Functions (100-Pin LFQFP, Chip Version A) or (100-Pin LFQFP, Chip Version B).

Figure 1.3 Pin Assignments of the 100-Pin LFQFP (Chip Version A and B)



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, refer to List of Pins and Pin Functions (80-Pin LQFP/LFQFP).

Figure 1.5 Pin Assignments of the 80-Pin LFQFP

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version B) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
94	AVSS0				
95	AVSS1				
96		P82	MTIC5U, MTIC5U#, TMO4	SCK6	
97		P81	MTIC5V, MTIC5V#, TMCI4	TXD6, SMOSI6, SSDA6	
98		P80	MTIC5W, MTIC5W#, TMRI4	RXD6, SMISO6, SSCL6	
99		P11	MTIOC3A, MTIOC3A#, MTCLKC, MTCLKC#, TMO3		IRQ1
100		P10	MTIOC9B, MTIOC9B#, MTCLKD, MTCLKD#, TMRI3, POE12#	CTS6#, RTS6#, SS6#	IRQ0

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps.

4. I/O Registers

This section provides information on the on-chip I/O register addresses and bit configuration. The information is given as shown below. Notes on writing to registers are also given below.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- Numbers of cycles for access indicate numbers of cycles of the given base clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERn of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

(a) Write to an I/O register.
(b) Read the value from the I/O register to a general register.
(c) Execute the operation using the value read.
(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

Table 4.1 List of I/O Registers (Address Order) (9/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 733Fh	ICU	Interrupt Source Priority Register 063*2	IPR063	8	8	2 ICLK
0008 7340h	ICU	Interrupt Source Priority Register 064	IPR064	8	8	2 ICLK
0008 7341h	ICU	Interrupt Source Priority Register 065	IPR065	8	8	2 ICLK
0008 7342h	ICU	Interrupt Source Priority Register 066	IPR066	8	8	2 ICLK
0008 7343h	ICU	Interrupt Source Priority Register 067	IPR067	8	8	2 ICLK
0008 7344h	ICU	Interrupt Source Priority Register 068	IPR068	8	8	2 ICLK
0008 7345h	ICU	Interrupt Source Priority Register 069	IPR069	8	8	2 ICLK
0008 7346h	ICU	Interrupt Source Priority Register 070	IPR070	8	8	2 ICLK
0008 7347h	ICU	Interrupt Source Priority Register 071	IPR071	8	8	2 ICLK
0008 7358h	ICU	Interrupt Source Priority Register 088	IPR088	8	8	2 ICLK
0008 7359h	ICU	Interrupt Source Priority Register 089	IPR089	8	8	2 ICLK
0008 7362h	ICU	Interrupt Source Priority Register 098*2	IPR098	8	8	2 ICLK
0008 7363h	ICU	Interrupt Source Priority Register 099*2	IPR099	8	8	2 ICLK
0008 7364h	ICU	Interrupt Source Priority Register 100*2	IPR100	8	8	2 ICLK
0008 7365h	ICU	Interrupt Source Priority Register 101*2	IPR101	8	8	2 ICLK
0008 7366h	ICU	Interrupt Source Priority Register 102	IPR102	8	8	2 ICLK
0008 7367h	ICU	Interrupt Source Priority Register 103	IPR103	8	8	2 ICLK
0008 7368h	ICU	Interrupt Source Priority Register 104	IPR104	8	8	2 ICLK
0008 7369h	ICU	Interrupt Source Priority Register 105	IPR105	8	8	2 ICLK
0008 736Ah	ICU	Interrupt Source Priority Register 106	IPR106	8	8	2 ICLK
0008 736Bh	ICU	Interrupt Source Priority Register 107	IPR107	8	8	2 ICLK
0008 736Ch	ICU	Interrupt Source Priority Register 108	IPR108	8	8	2 ICLK
0008 736Dh	ICU	Interrupt Source Priority Register 109	IPR109	8	8	2 ICLK
0008 736Eh	ICU	Interrupt Source Priority Register 110	IPR110	8	8	2 ICLK
0008 736Fh	ICU	Interrupt Source Priority Register 111	IPR111	8	8	2 ICLK
0008 7370h	ICU	Interrupt Source Priority Register 112	IPR112	8	8	2 ICLK
0008 7371h	ICU	Interrupt Source Priority Register 113	IPR113	8	8	2 ICLK
0008 7372h	ICU	Interrupt Source Priority Register 114	IPR114	8	8	2 ICLK
0008 7376h	ICU	Interrupt Source Priority Register 118	IPR118	8	8	2 ICLK
0008 7379h	ICU	Interrupt Source Priority Register 121	IPR121	8	8	2 ICLK
0008 737Bh	ICU	Interrupt Source Priority Register 123	IPR123	8	8	2 ICLK
0008 737Dh	ICU	Interrupt Source Priority Register 125	IPR125	8	8	2 ICLK
0008 737Fh	ICU	Interrupt Source Priority Register 127	IPR127	8	8	2 ICLK
0008 7381h	ICU	Interrupt Source Priority Register 129	IPR129	8	8	2 ICLK
0008 7385h	ICU	Interrupt Source Priority Register 133	IPR133	8	8	2 ICLK
0008 7386h	ICU	Interrupt Source Priority Register 134	IPR134	8	8	2 ICLK
0008 738Ah	ICU	Interrupt Source Priority Register 138	IPR138	8	8	2 ICLK
0008 738Bh	ICU	Interrupt Source Priority Register 139	IPR139	8	8	2 ICLK
0008 738Eh	ICU	Interrupt Source Priority Register 142	IPR142	8	8	2 ICLK
0008 7392h	ICU	Interrupt Source Priority Register 146	IPR146	8	8	2 ICLK
0008 7395h	ICU	Interrupt Source Priority Register 149	IPR149	8	8	2 ICLK
0008 7397h	ICU	Interrupt Source Priority Register 151	IPR151	8	8	2 ICLK
0008 7399h	ICU	Interrupt Source Priority Register 153	IPR153	8	8	2 ICLK
0008 739Fh	ICU	Interrupt Source Priority Register 159	IPR159	8	8	2 ICLK
0008 73A3h	ICU	Interrupt Source Priority Register 163	IPR163	8	8	2 ICLK
0008 73A8h	ICU	Interrupt Source Priority Register 168	IPR168	8	8	2 ICLK
0008 73ADh	ICU	Interrupt Source Priority Register 173	IPR173	8	8	2 ICLK
0008 73AEh	ICU	Interrupt Source Priority Register 174	IPR174	8	8	2 ICLK
0008 73B1h	ICU	Interrupt Source Priority Register 177	IPR177	8	8	2 ICLK
0008 73B4h	ICU	Interrupt Source Priority Register 180	IPR180	8	8	2 ICLK
0008 73B7h	ICU	Interrupt Source Priority Register 183	IPR183	8	8	2 ICLK
0008 73BAh	ICU	Interrupt Source Priority Register 186	IPR186	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (15/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 94D4h	S12AD2	A/D Channel Select Register C0	ADANSC0	16	16	2 or 3 PCLKB
0008 94D9h	S12AD2	A/D Group C Trigger Select Register	ADGCTRGR	8	8	2 or 3 PCLKB
0008 94DFh	S12AD2	A/D Sampling State Register O	ADSSTRO	8	8	2 or 3 PCLKB
0008 94E0h	S12AD2	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB
0008 94E1h	S12AD2	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB
0008 94E2h	S12AD2	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB
0008 94E3h	S12AD2	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB
0008 94E4h	S12AD2	A/D Sampling State Register 4	ADSSTR4	8	8	2 or 3 PCLKB
0008 94E5h	S12AD2	A/D Sampling State Register 5	ADSSTR5	8	8	2 or 3 PCLKB
0008 94E6h	S12AD2	A/D Sampling State Register 6	ADSSTR6	8	8	2 or 3 PCLKB
0008 94E7h	S12AD2	A/D Sampling State Register 7	ADSSTR7	8	8	2 or 3 PCLKB
0008 94E8h	S12AD2	A/D Sampling State Register 8	ADSSTR8	8	8	2 or 3 PCLKB
0008 94E9h	S12AD2	A/D Sampling State Register 9	ADSSTR9	8	8	2 or 3 PCLKB
0008 94EAh	S12AD2	A/D Sampling State Register 10	ADSSTR10	8	8	2 or 3 PCLKB
0008 94EBh	S12AD2	A/D Sampling State Register 11	ADSSTR11	8	8	2 or 3 PCLKB
0008 A020h	SCI1	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A021h	SCI1	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A022h	SCI1	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A023h	SCI1	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A024h	SCI1	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A025h	SCI1	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A026h	SMCI1	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A027h	SCI1	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A028h	SCI1	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A029h	SCI1	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A02Ah	SCI1	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A02Bh	SCI1	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A02Ch	SCI1	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A02Dh	SCI1	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A02Eh	SCI1	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB
0008 A02Eh	SCI1	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB
0008 A02Fh	SCI1	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 A030h	SCI1	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB
0008 A030h	SCI1	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 A031h	SCI1	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 A032h	SCI1	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 A0A0h	SCI5	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A0A1h	SCI5	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A0A2h	SCI5	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A0A3h	SCI5	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A0A4h	SCI5	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A0A5h	SCI5	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A0A6h	SMCI5	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A0A7h	SCI5	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A0A8h	SCI5	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A0A9h	SCI5	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A0AAh	SCI5	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A0ABh	SCI5	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A0ACh	SCI5	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A0ADh	SCI5	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A0AEh	SCI5	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB
0008 A0AEh	SCI5	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (16/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 A0AFh	SCI5	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 A0B0h	SCI5	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB
0008 A0B0h	SCI5	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 A0B1h	SCI5	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 A0B2h	SCI5	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 A0C0h	SCI6	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A0C1h	SCI6	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A0C2h	SCI6	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A0C3h	SCI6	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A0C4h	SCI6	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A0C5h	SCI6	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A0C6h	SMCI6	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A0C7h	SCI6	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A0C8h	SCI6	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A0C9h	SCI6	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A0CAh	SCI6	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A0CBh	SCI6	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A0CCh	SCI6	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A0CDh	SCI6	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A0CEh	SCI6	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB
0008 A0CEh	SCI6	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB
0008 A0CFh	SCI6	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 A0D0h	SCI6	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB
0008 A0D0h	SCI6	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 A0D1h	SCI6	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 A0D2h	SCI6	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 B000h	CAC	CAC Control Register 0	CACR0	8	8	2 or 3 PCLKB
0008 B001h	CAC	CAC Control Register 1	CACR1	8	8	2 or 3 PCLKB
0008 B002h	CAC	CAC Control Register 2	CACR2	8	8	2 or 3 PCLKB
0008 B003h	CAC	CAC Interrupt Request Enable Register	CAICR	8	8	2 or 3 PCLKB
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2 or 3 PCLKB
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2 or 3 PCLKB
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2 or 3 PCLKB
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2 or 3 PCLKB
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2 or 3 PCLKB
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2 or 3 PCLKB
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2 or 3 PCLKB
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C004h	PORT4	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C005h	PORT5	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C006h	PORT6	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C007h	PORT7	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C008h	PORT8	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C009h	PORT9	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Ah	PORTA	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Bh	PORTB	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Dh	PORTD	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Eh	PORTE	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C020h	PORT0	Port Output Data Register	PODR	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (24/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
000A 83F8h	RSCAN	Receive Buffer Register 5CL*2	RMDF05	16	16	2 or 3 PCLKB
000A 83FAh	RSCAN	Receive Rule Entry Register 7BH*2	GAFLMH7	16	16	2 or 3 PCLKB
000A 83FAh	RSCAN	Receive Buffer Register 5CH*2	RMDF15	16	16	2 or 3 PCLKB
000A 83FCh	RSCAN	Receive Rule Entry Register 7CL*2	GAFLPL7	16	16	2 or 3 PCLKB
000A 83FCh	RSCAN	Receive Buffer Register 5DL*2	RMDF25	16	16	2 or 3 PCLKB
000A 83FEh	RSCAN	Receive Rule Entry Register 7CH*2	GAFLPH7	16	16	2 or 3 PCLKB
000A 83FEh	RSCAN	Receive Buffer Register 5DH*2	RMDF35	16	16	2 or 3 PCLKB
000A 8400h	RSCAN	Receive Rule Entry Register 8AL*2	GAFLIDL8	16	16	2 or 3 PCLKB
000A 8400h	RSCAN	Receive Buffer Register 6AL*2	RMIDL6	16	16	2 or 3 PCLKB
000A 8402h	RSCAN	Receive Rule Entry Register 8AH*2	GAFLIDH8	16	16	2 or 3 PCLKB
000A 8402h	RSCAN	Receive Buffer Register 6AH*2	RMIDH6	16	16	2 or 3 PCLKB
000A 8404h	RSCAN	Receive Rule Entry Register 8BL*2	GAFLML8	16	16	2 or 3 PCLKB
000A 8404h	RSCAN	Receive Buffer Register 6BL*2	RMTS6	16	16	2 or 3 PCLKB
000A 8406h	RSCAN	Receive Rule Entry Register 8BH*2	GAFLMH8	16	16	2 or 3 PCLKB
000A 8406h	RSCAN	Receive Buffer Register 6BH*2	RMPTR6	16	16	2 or 3 PCLKB
000A 8408h	RSCAN	Receive Rule Entry Register 8CL*2	GAFLPL8	16	16	2 or 3 PCLKB
000A 8408h	RSCAN	Receive Buffer Register 6CL*2	RMDF06	16	16	2 or 3 PCLKB
000A 840Ah	RSCAN	Receive Rule Entry Register 8CH*2	GAFLPH8	16	16	2 or 3 PCLKB
000A 840Ah	RSCAN	Receive Buffer Register 6CH*2	RMDF16	16	16	2 or 3 PCLKB
000A 840Ch	RSCAN	Receive Rule Entry Register 9AL*2	GAFLIDL9	16	16	2 or 3 PCLKB
000A 840Ch	RSCAN	Receive Buffer Register 6DL*2	RMDF26	16	16	2 or 3 PCLKB
000A 840Eh	RSCAN	Receive Rule Entry Register 9AH*2	GAFLIDH9	16	16	2 or 3 PCLKB
000A 840Eh	RSCAN	Receive Buffer Register 6DH*2	RMDF36	16	16	2 or 3 PCLKB
000A 8410h	RSCAN	Receive Rule Entry Register 9BL*2	GAFLML9	16	16	2 or 3 PCLKB
000A 8410h	RSCAN	Receive Buffer Register 7AL*2	RMIDL7	16	16	2 or 3 PCLKB
000A 8412h	RSCAN	Receive Rule Entry Register 9BH*2	GAFLMH9	16	16	2 or 3 PCLKB
000A 8412h	RSCAN	Receive Buffer Register 7AH*2	RMIDH7	16	16	2 or 3 PCLKB
000A 8414h	RSCAN	Receive Rule Entry Register 9CL*2	GAFLPL9	16	16	2 or 3 PCLKB
000A 8414h	RSCAN	Receive Buffer Register 7BL*2	RMTS7	16	16	2 or 3 PCLKB
000A 8416h	RSCAN	Receive Rule Entry Register 9CH*2	GAFLPH9	16	16	2 or 3 PCLKB
000A 8416h	RSCAN	Receive Buffer Register 7BH*2	RMPTR7	16	16	2 or 3 PCLKB
000A 8418h	RSCAN	Receive Rule Entry Register 10AL*2	GAFLIDL10	16	16	2 or 3 PCLKB
000A 8418h	RSCAN	Receive Buffer Register 7CL*2	RMDF07	16	16	2 or 3 PCLKB
000A 841Ah	RSCAN	Receive Rule Entry Register 10AH*2	GAFLIDH10	16	16	2 or 3 PCLKB
000A 841Ah	RSCAN	Receive Buffer Register 7CH*2	RMDF17	16	16	2 or 3 PCLKB
000A 841Ch	RSCAN	Receive Rule Entry Register 10BL*2	GAFLML10	16	16	2 or 3 PCLKB
000A 841Ch	RSCAN	Receive Buffer Register 7DL*2	RMDF27	16	16	2 or 3 PCLKB
000A 841Eh	RSCAN	Receive Rule Entry Register 10BH*2	GAFLMH10	16	16	2 or 3 PCLKB
000A 841Eh	RSCAN	Receive Buffer Register 7DH*2	RMDF37	16	16	2 or 3 PCLKB
000A 8420h	RSCAN	Receive Rule Entry Register 10CL*2	GAFLPL10	16	16	2 or 3 PCLKB
000A 8420h	RSCAN	Receive Buffer Register 8AL*2	RMIDL8	16	16	2 or 3 PCLKB
000A 8422h	RSCAN	Receive Rule Entry Register 10CH*2	GAFLPH10	16	16	2 or 3 PCLKB
000A 8422h	RSCAN	Receive Buffer Register 8AH*2	RMIDH8	16	16	2 or 3 PCLKB
000A 8424h	RSCAN	Receive Rule Entry Register 11AL*2	GAFLIDL11	16	16	2 or 3 PCLKB
000A 8424h	RSCAN	Receive Buffer Register 8BL*2	RMTS8	16	16	2 or 3 PCLKB
000A 8426h	RSCAN	Receive Rule Entry Register 11AH*2	GAFLIDH11	16	16	2 or 3 PCLKB
000A 8426h	RSCAN	Receive Buffer Register 8BH*2	RMPTR8	16	16	2 or 3 PCLKB
000A 8428h	RSCAN	Receive Rule Entry Register 11BL*2	GAFLML11	16	16	2 or 3 PCLKB
000A 8428h	RSCAN	Receive Buffer Register 8CL*2	RMDF08	16	16	2 or 3 PCLKB
000A 842Ah	RSCAN	Receive Rule Entry Register 11BH*2	GAFLMH11	16	16	2 or 3 PCLKB
000A 842Ah	RSCAN	Receive Buffer Register 8CH*2	RMDF18	16	16	2 or 3 PCLKB
000A 842Ch	RSCAN	Receive Rule Entry Register 11CL*2	GAFLPL11	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (35/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
000C 2280h	GPT3	General PWM Timer I/O Control Register*2	GTIOR	16	8, 16, 32	4 or 5 PCLKA
000C 2282h	GPT3	General PWM Timer Interrupt Output Setting Register*2	GTINTAD	16	8, 16, 32	4 or 5 PCLKA
000C 2284h	GPT3	General PWM Timer Control Register*2	GTCR	16	8, 16, 32	4 or 5 PCLKA
000C 2286h	GPT3	General PWM Timer Buffer Enable Register*2	GTBER	16	8, 16, 32	4 or 5 PCLKA
000C 2288h	GPT3	General PWM Timer Count Direction Register*2	GTUDC	16	8, 16, 32	4 or 5 PCLKA
000C 228Ah	GPT3	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register*2	GTITC	16	8, 16, 32	4 or 5 PCLKA
000C 228Ch	GPT3	General PWM Timer Status Register*2	GTST	16	8, 16, 32	4 or 5 PCLKA
000C 228Eh	GPT3	General PWM Timer Counter*2	GTCNT	16	16	4 or 5 PCLKA
000C 2290h	GPT3	General PWM Timer Compare Capture Register A*2	GTCCRA	16	16, 32	4 or 5 PCLKA
000C 2292h	GPT3	General PWM Timer Compare Capture Register B*2	GTCCRB	16	16, 32	4 or 5 PCLKA
000C 2294h	GPT3	General PWM Timer Compare Capture Register C*2	GTCCRC	16	16, 32	4 or 5 PCLKA
000C 2296h	GPT3	General PWM Timer Compare Capture Register D*2	GTCCRD	16	16, 32	4 or 5 PCLKA
000C 2298h	GPT3	General PWM Timer Compare Capture Register E*2	GTCCRE	16	16, 32	4 or 5 PCLKA
000C 229Ah	GPT3	General PWM Timer Compare Capture Register F*2	GTCCRF	16	16, 32	4 or 5 PCLKA
000C 229Ch	GPT3	General PWM Timer Period Setting Register*2	GTPR	16	16, 32	4 or 5 PCLKA
000C 229Eh	GPT3	General PWM Timer Period Setting Buffer Register*2	GTPBR	16	16, 32	4 or 5 PCLKA
000C 22A0h	GPT3	General PWM Timer Period Setting Double Buffer Register*2	GTPDBR	16	16, 32	4 or 5 PCLKA
000C 22A4h	GPT3	A/D Converter Start Request Timing Register A*2	GTADTRA	16	16, 32	4 or 5 PCLKA
000C 22A6h	GPT3	A/D Converter Start Request Timing Buffer Register A*2	GTADTBRA	16	16, 32	4 or 5 PCLKA
000C 22A8h	GPT3	A/D Converter Start Request Timing Double Buffer Register A*2	GTADTDBRA	16	16, 32	4 or 5 PCLKA
000C 22ACh	GPT3	A/D Converter Start Request Timing Register B*2	GTADTRB	16	16, 32	4 or 5 PCLKA
000C 22AEh	GPT3	A/D Converter Start Request Timing Buffer Register B*2	GTADTBRB	16	16, 32	4 or 5 PCLKA
000C 22B0h	GPT3	A/D Converter Start Request Timing Double Buffer Register B*2	GTADTDBRB	16	16, 32	4 or 5 PCLKA
000C 22B4h	GPT3	General PWM Timer Output Negate Control Register*2	GTONCR	16	16, 32	4 or 5 PCLKA
000C 22B6h	GPT3	General PWM Timer Dead Time Control Register*2	GTDTCR	16	16, 32	4 or 5 PCLKA
000C 22B8h	GPT3	General PWM Timer Dead Time Value Register U*2	GTDVU	16	16, 32	4 or 5 PCLKA
000C 22BAh	GPT3	General PWM Timer Dead Time Value Register D*2	GTDVD	16	16, 32	4 or 5 PCLKA
000C 22BCh	GPT3	General PWM Timer Dead Time Buffer Register U*2	GTDBU	16	16, 32	4 or 5 PCLKA
000C 22BEh	GPT3	General PWM Timer Dead Time Buffer Register D*2	GTDBD	16	16, 32	4 or 5 PCLKA
000C 22C0h	GPT3	General PWM Timer Output Protection Function Status Register*2	GTSOS	16	16, 32	4 or 5 PCLKA
000C 22C2h	GPT3	General PWM Timer Output Protection Function Temporary Release Register*2	GTSOTR	16	16, 32	4 or 5 PCLKA
000C 2300h	GPT01	General PWM Timer Longword Counter*2	GTCNTLW	32	32	4 or 5 PCLKA
000C 2304h	GPT01	General PWM Timer Longword Compare Capture Register A*2	GTCCRALW	32	32	4 or 5 PCLKA
000C 2308h	GPT01	General PWM Timer Longword Compare Capture Register B*2	GTCCRBLW	32	32	4 or 5 PCLKA
000C 230Ch	GPT01	General PWM Timer Longword Compare Capture Register C*2	GTCCRCLW	32	32	4 or 5 PCLKA
000C 2310h	GPT01	General PWM Timer Longword Compare Capture Register D*2	GTCCRDLW	32	32	4 or 5 PCLKA
000C 2314h	GPT01	General PWM Timer Longword Compare Capture Register E*2	GTCCRELW	32	32	4 or 5 PCLKA
000C 2318h	GPT01	General PWM Timer Longword Compare Capture Register F*2	GTCCRFLW	32	32	4 or 5 PCLKA
000C 231Ch	GPT01	General PWM Timer Longword Period Setting Register*2	GTPRLW	32	32	4 or 5 PCLKA
000C 2320h	GPT01	General PWM Timer Longword Period Setting Buffer Register*2	GTPBRLW	32	32	4 or 5 PCLKA
000C 2324h	GPT01	General PWM Timer Longword Period Setting Double Buffer Register*2	GTPDBRLW	32	32	4 or 5 PCLKA
000C 2328h	GPT01	Longword A/D Converter Start Request Timing Register A*2	GTADTRALW	32	32	4 or 5 PCLKA
000C 232Ch	GPT01	Longword A/D Converter Start Request Timing Buffer Register A*2	GTADTBRALW	32	32	4 or 5 PCLKA

5.2 DC Characteristics

Table 5.3 DC Characteristics (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)	V_{IH}	VCC × 0.7	—	5.8	V	
	Ports B1, B2 (5 V tolerant)		VCC × 0.8	—	5.8		
	Ports 00 to 02, ports 10, 11, ports 20 to 24, ports 30 to 33, 36, 37, ports 70 to 76, ports 80 to 82, ports 90 to 96, ports A0 to A5, port B0, ports B3 to B7, ports D0 to D7, ports E0 to E5, RES#		VCC × 0.8	—	VCC + 0.3		
	Ports 40 to 47, ports 50 to 55, ports 60 to 65		VREF × 0.8	—	VREF + 0.3		
	RIIC input pin (except for SMBus)	V_{IL}	–0.3	—	VCC × 0.3		
	Ports 40 to 47, ports 50 to 55, ports 60 to 65		–0.3	—	VREF × 0.2		
	Other than RIIC input pin, Other than ports 40 to 47, 50 to 55, or 60 to 65		–0.3	—	VCC × 0.2		
	RIIC input pin (except for SMBus)	ΔV_T	VCC × 0.05	—	—		
	Ports 40 to 47, ports 50 to 55, ports 60 to 65		VREF × 0.1	—	—		
	Other than RIIC input pin, Other than ports 40 to 47, 50 to 55, or 60 to 65		VCC × 0.1	—	—		
Input level voltage (except for Schmitt trigger input pins)	MD	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL (external clock input)		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (SMBus)		2.1	—	VCC + 0.3		VCC ≤ 5.2 V
	MD	V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL (external clock input)		–0.3	—	VCC × 0.2		
	RIIC input pin (SMBus)		–0.3	—	0.8		VCC ≤ 5.2 V

5.3 AC Characteristics

5.3.1 Clock Timing

Table 5.14 Operating Frequency Value (High-Speed Operating Mode)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	min.	typ.	max.	Unit
Operating frequency	System clock (ICLK)	f_{max}	—	—	80	MHz
	FlashIF clock (FCLK)*1, *2		—	—	32	
	Peripheral module clock (PCLKA)		—	—	80	
	Peripheral module clock (PCLKB)		—	—	40	
	Peripheral module clock (PCLKD)		—	—	40	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.

Table 5.15 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	min.	typ.	max.	Unit
Operating frequency	System clock (ICLK)	f_{max}	—	—	12	MHz
	FlashIF clock (FCLK)*1, *2		—	—	12	
	Peripheral module clock (PCLKA)		—	—	12	
	Peripheral module clock (PCLKB)		—	—	12	
	Peripheral module clock (PCLKD)		—	—	12	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.

5.3.2 Reset Timing

Table 5.17 Reset Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	At power-on	t_{RESWP}	3	—	—	ms	Figure 5.29
	Other than above	t_{RESW}	30	—	—	µs	Figure 5.30
Wait time after RES# cancellation (at power-on)		t_{RESWT}	—	27.5	—	ms	Figure 5.29
Wait time after RES# cancellation (during powered-on state)		t_{RESWT}	—	114	—	µs	Figure 5.30
Independent watchdog timer reset period		t_{RESWIW}	—	1	—	IWDT clock cycle	Figure 5.31
Software reset period		t_{RESWSW}	—	1	—	ICLK cycle	
Wait time after independent watchdog timer reset cancellation*1		t_{RESW2}	—	300	—	µs	
Wait time after software reset cancellation		t_{RESW2}	—	168	—	µs	

Note 1. When IWDTCR.CKS[3:0] = 0000b.

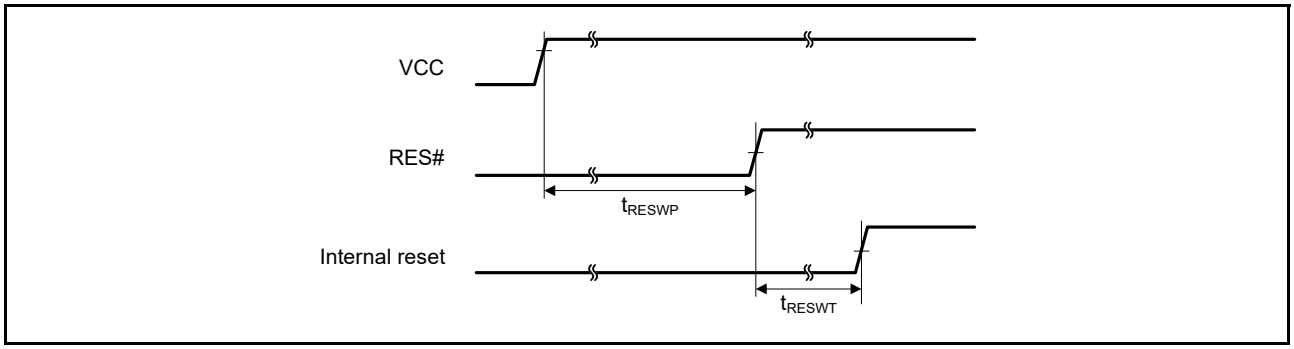


Figure 5.29 Reset Input Timing at Power-On

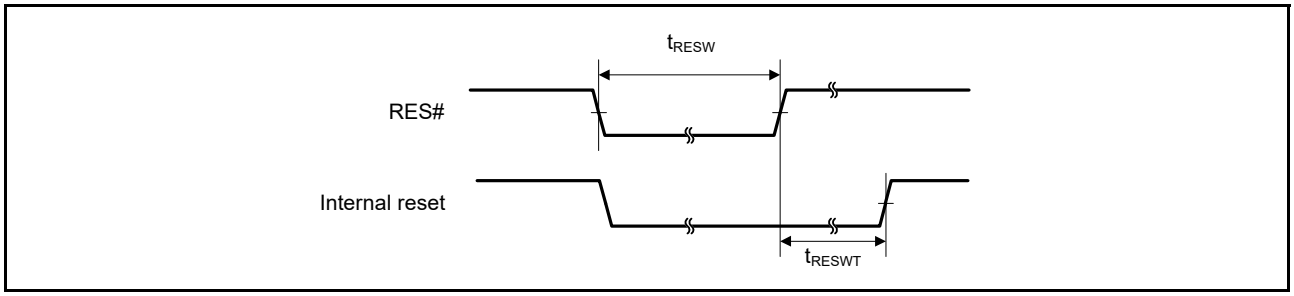


Figure 5.30 Reset Input Timing (1)

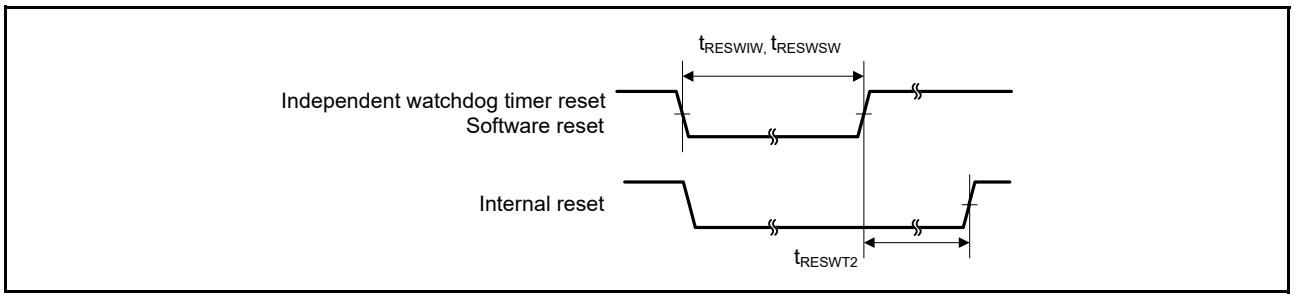


Figure 5.31 Reset Input Timing (2)

Table 5.19 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Middle-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 5.32
			Main clock oscillator and PLL circuit operating*3	t_{SBYPC}	—	2	3	ms	
		External clock input to main clock oscillator	Main clock oscillator operating*4	t_{SBYEX}	—	3	4	µs	
			Main clock oscillator and PLL circuit operating*5	t_{SBYPE}	—	65	85	µs	
		HOCO clock oscillator operating	HOCO clock oscillator operating 1 *6	t_{SBYHO}	—	40	50	µs	
			HOCO clock oscillator operating 2 *7		—	75	85	µs	
			HOCO clock oscillator and PLL circuit operating*8	t_{SBYPH}	—	110	125	µs	
		LOCO clock oscillator operating*9		t_{SBYLO}	—	5	7	µs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.

Note 2. When the frequency of the crystal is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 3. When the frequency of PLL is 48 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 12 MHz.

Note 4. When the frequency of the external clock is 12 MHz.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 5. When the frequency of PLL is 48 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 12 MHz.

Note 6. When the frequency of the high-speed on-chip oscillator is 32 MHz. When the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 05h. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 8 MHz.

Note 7. When the frequency of the high-speed on-chip oscillator is 64 MHz. Set the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 06h. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 8 MHz.

Note 8. When the frequency of the high-speed on-chip oscillator is 32 MHz, and the frequency of PLL is 80 MHz. When the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 05h. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 10 MHz.

Note 9. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

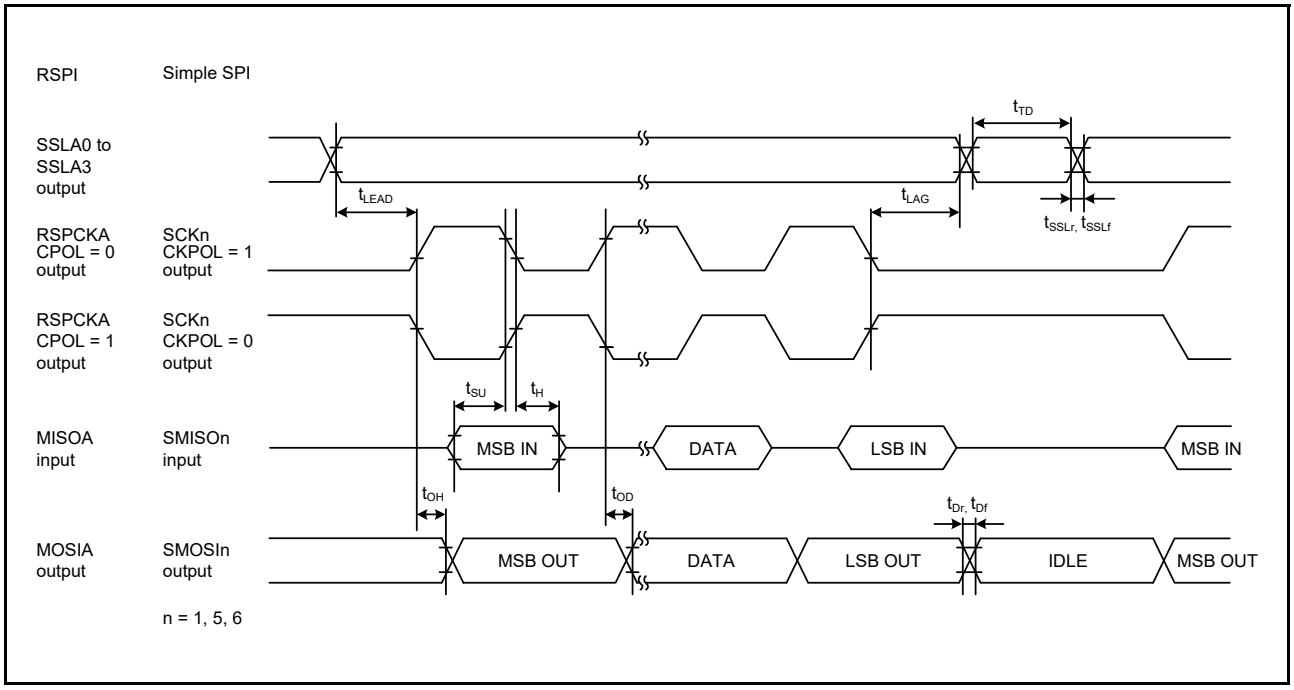


Figure 5.49 RSPI Timing (Master, CPHA = 1) and Simple SPI Clock Timing (Master, CKPH = 0)

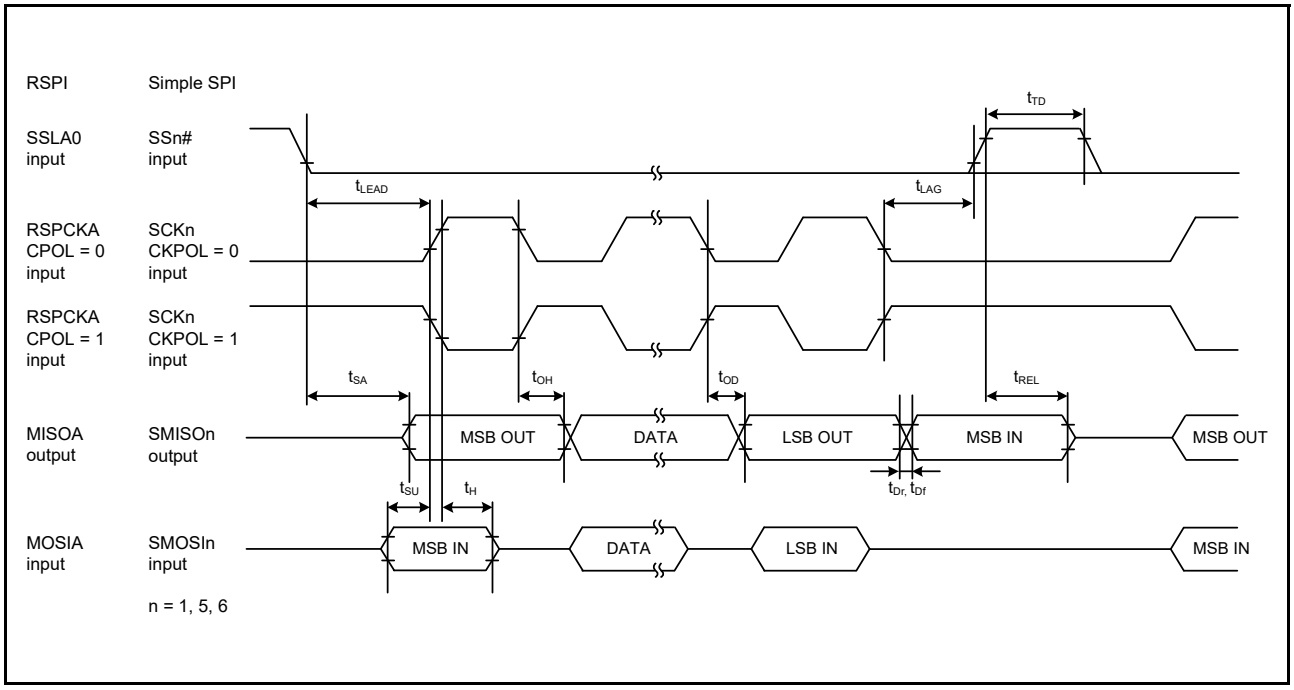


Figure 5.50 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1)

5.8 Power-On Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.36 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (1)

Conditions: VCC = 0 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	1.35	1.50	1.65	V	Figure 5.55, Figure 5.56
	Voltage detection circuit (LVD0)*1	V_{det0_0}	3.67	3.84	3.97	V	
		V_{det0_1}	2.70	2.82	3.00		
		V_{det0_2}	2.37	2.51	2.67		
	Voltage detection circuit (LVD1)*2	V_{det1_0}	4.12	4.29	4.42	V	Figure 5.58 At falling edge VCC
		V_{det1_1}	3.98	4.14	4.28		
		V_{det1_2}	3.86	4.02	4.16		
		V_{det1_3}	3.68	3.84	3.98		
		V_{det1_4}	2.99	3.10	3.29		
		V_{det1_5}	2.89	3.00	3.19		
		V_{det1_6}	2.79	2.90	3.09		
		V_{det1_7}	2.68	2.79	2.98		
		V_{det1_8}	2.57	2.68	2.87		
	Voltage detection circuit (LVD2)*3	V_{det2_0}	4.08	4.29	4.48		Figure 5.59 At falling edge VCC
		V_{det2_1}	3.95	4.14	4.35		
		V_{det2_2}	3.82	4.02	4.22		
		V_{det2_3}	3.62	3.84	4.02		

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol V_{det0_n} denotes the value of the LVDS0[1:0] bits.

Note 2. n in the symbol V_{det1_n} denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.

Note 3. n in the symbol V_{det2_n} denotes the value of the LVDLVLR.LVD2LVL[3:0] bits.

Table 5.37 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2)

Conditions: VCC = 0 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, Ta = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Wait time after power-on reset cancellation	At normal startup	t_{POR}	—	28.4	—	ms	Figure 5.56
Wait time after voltage monitoring 0 reset cancellation		t_{LVD0}	—	568	—	µs	Figure 5.57
Wait time after voltage monitoring 1 reset cancellation		t_{LVD1}	—	100	—	µs	Figure 5.58
Wait time after voltage monitoring 2 reset cancellation		t_{LVD2}	—	100	—	µs	Figure 5.59
Response delay time		t_{det}	—	—	350	µs	Figure 5.55
Minimum VCC down time*1		t_{VOFF}	350	—	—	µs	Figure 5.55, VCC = 1.0 V or above
Power-on reset enable time		$t_{W(POR)}$	1	—	—	ms	Figure 5.56, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$	—	—	300	µs	Figure 5.58, Figure 5.59
Hysteresis width (LVD0, LVD1 and LVD2)		V_{LVH}	—	70	—	mV	Vdet1_0 to 4 selected
			—	60	—		Vdet0_0 to 2 selected Vdet1_5 to 8 selected LVD2 selected

5.9 Oscillation Stop Detection Timing

Table 5.38 Oscillation Stop Detection Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 =AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, Ta = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.60

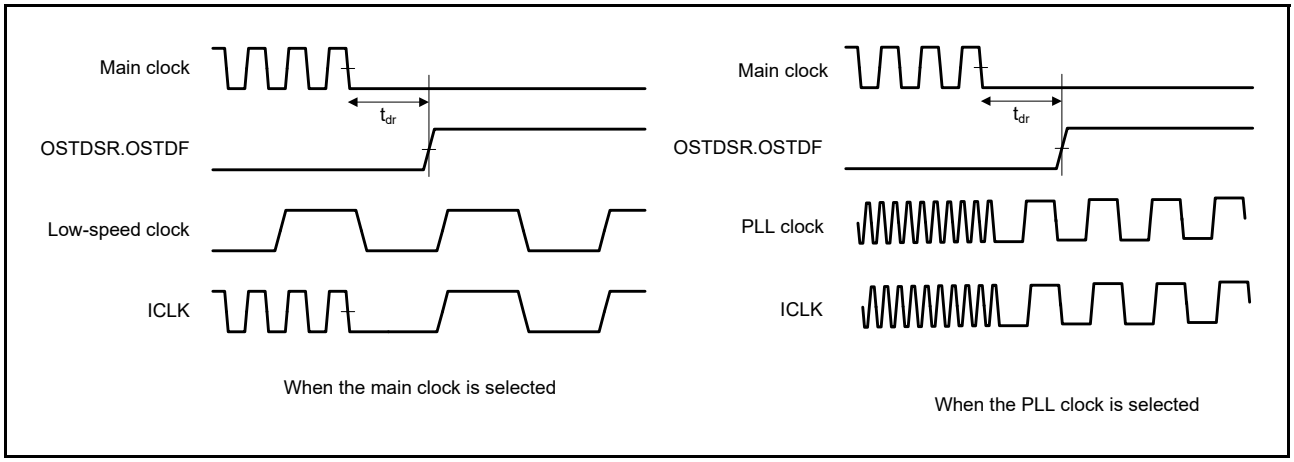
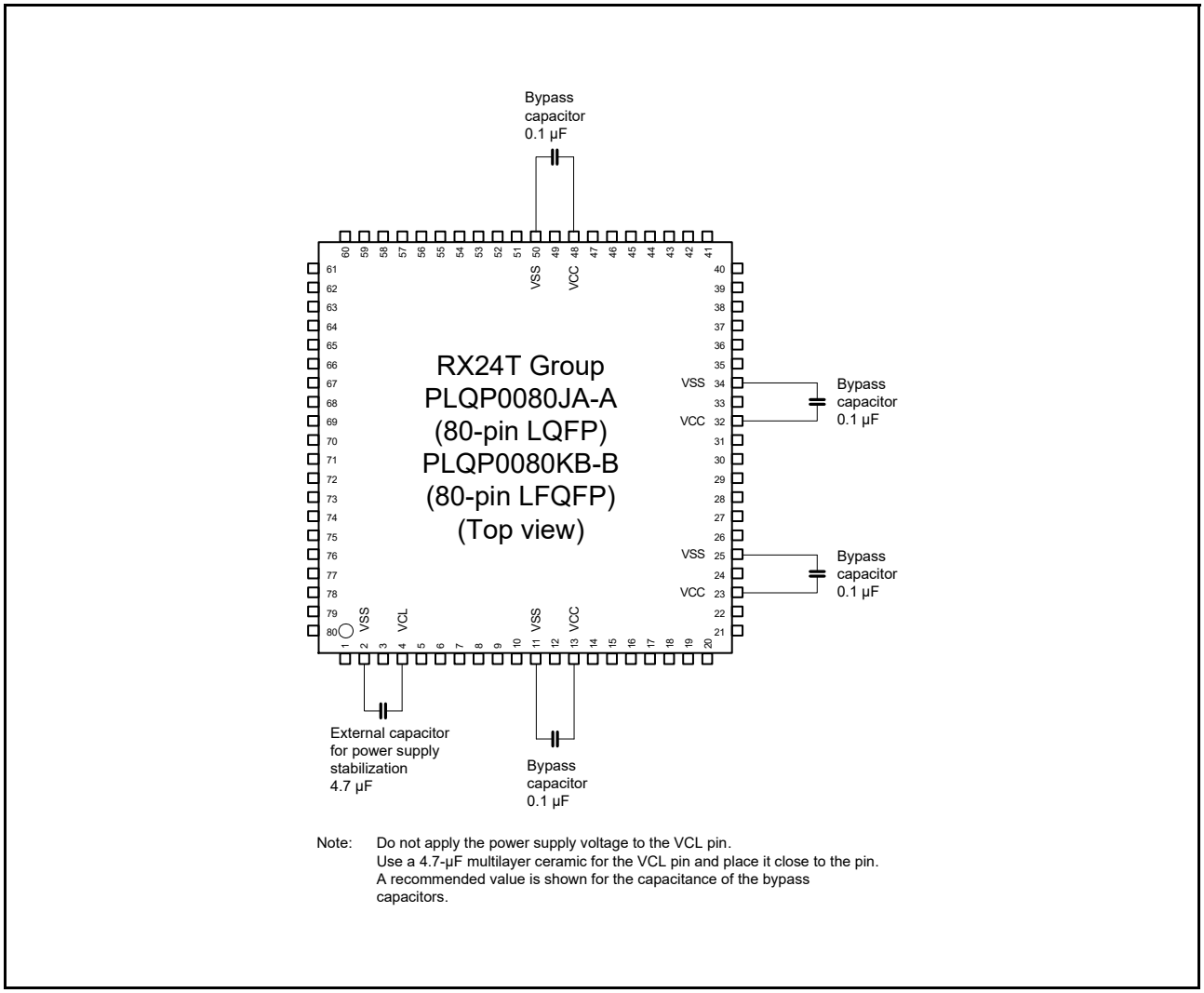


Figure 5.60 Oscillation Stop Detection Timing



Note: Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 5.62 Connecting Capacitors (80 Pins)

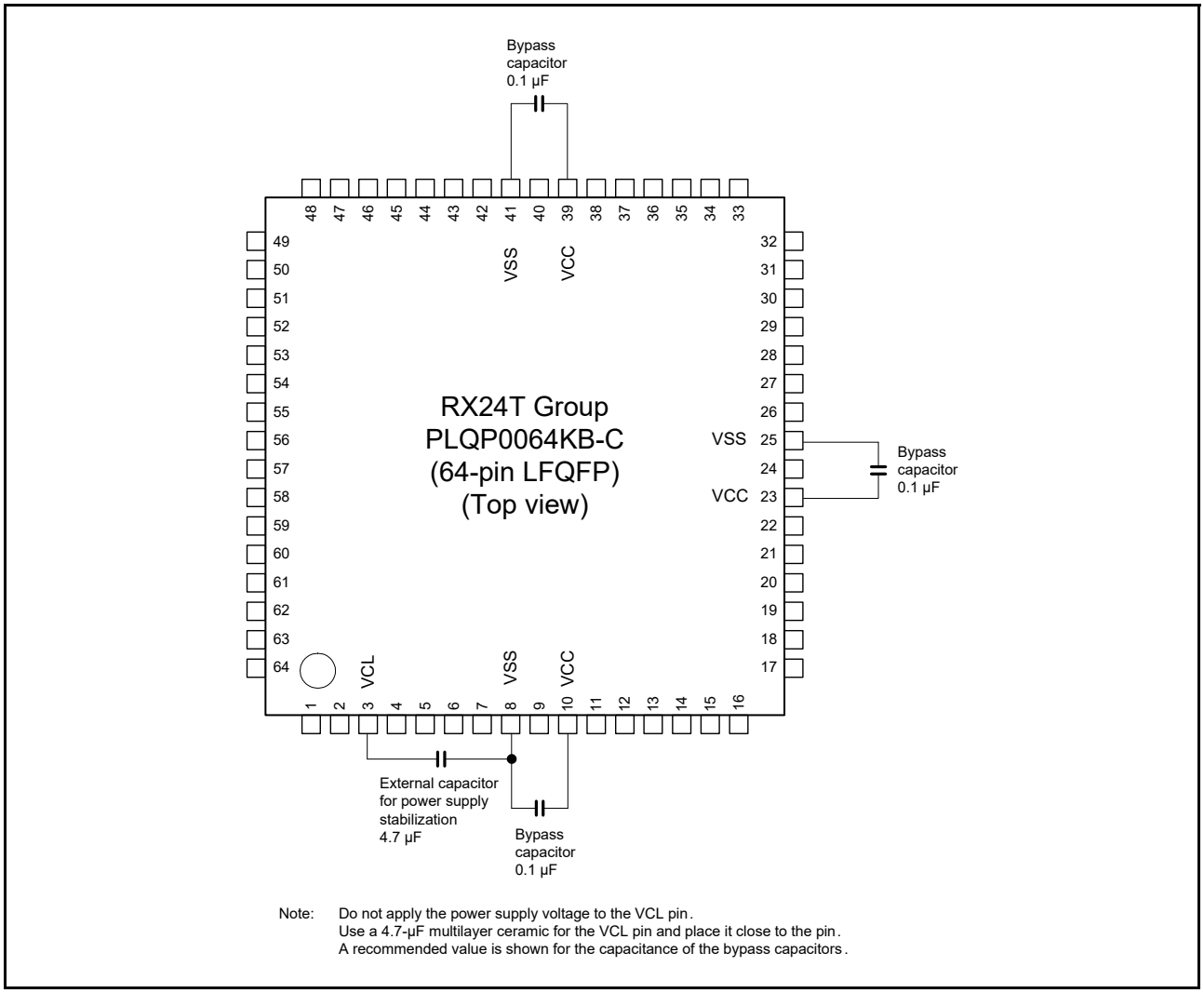


Figure 5.63 Connecting Capacitors (64 Pins)