Renesas Electronics America Inc - R5F524T8ADFN#30 Datasheet

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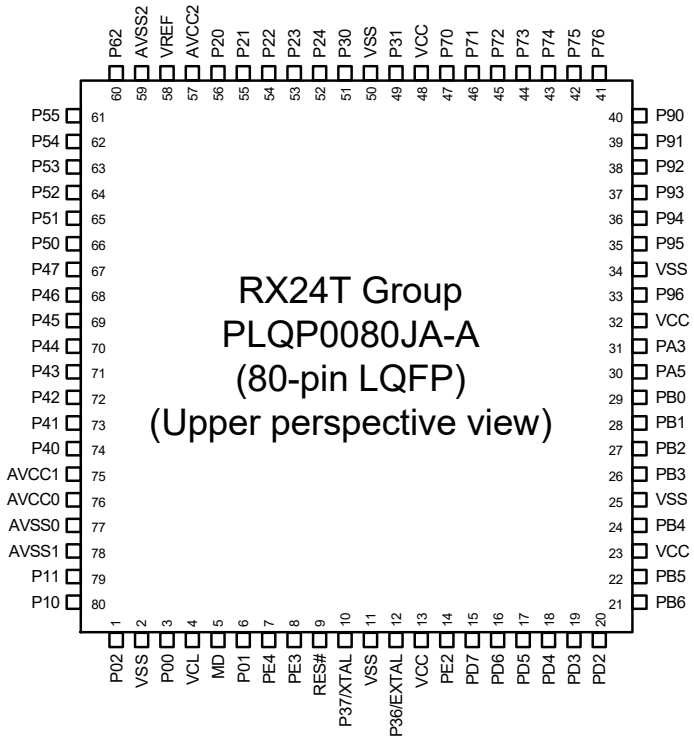
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 17x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f524t8adfn-30



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, refer to List of Pins and Pin Functions (80-Pin LQFP/LFQFP).

Figure 1.4 Pin Assignments of the 80-Pin LQFP

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version B) (1/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
1		PE5			IRQ0
2		P02	MTIOC9D, MTIOC9D#	CTS1#, RTS1#, SS1#	IRQ5, ADST0
3	VSS				
4		P00			IRQ2, ADST1
5	VCL				
6	MD				FINED
7		P01	POE12#		IRQ4, ADST2
8		PE4	MTCLKC, MTCLKC#, POE10#		IRQ1
9		PE3	MTCLKD, MTCLKD#, POE11#		IRQ2
10	RES#				
11	XTAL	P37			
12	VSS				
13	EXTAL	P36			
14	VCC				
15		PE2	POE10#		NMI
16		PE1	MTIOC9D, MTIOC9D#, TMO5	CTS5#, RTS5#, SS5#, SSLA3	
17		PE0	MTIOC9B, MTIOC9B#, TMCI1, TMCI5	RXD5, SMISO5, SSCL5, SSLA2	
18		PD7	MTIOC9A, MTIOC9A#, TMRI1, TMRI5, GTIOC3A, GTIOC3A#	TXD5, SMOSI5, SSDA5, SSLA1	
19		PD6	MTIOC9C, MTIOC9C#, TMO1, GTIOC3B, GTIOC3B#	CTS1#, RTS1#, SS1#, SSLA0	IRQ5, ADST0
20		PD5	TMRI0, TMRI6, GTECLKA	RXD1, SMISO1, SSCL1	IRQ3
21		PD4	TMCI0, TMCI6, GTECLKB	SCK1	IRQ2
22		PD3	TMO0, GTECLKC	TXD1, SMOSI1, SSDA1	
23		PD2	TMCI1, TMO4, GTIOC0A, GTIOC0A#	SCK5, MOSIA	
24		PD1	TMO2, GTIOC0B, GTIOC0B#	MISOA	
25		PD0	TMO6, GTIOC1A, GTIOC1A#	RSPCKA	
26		PB7	GTIOC1B, GTIOC1B#	SCK5	
27		PB6	GTIOC2A, GTIOC2A#	RXD5, SMISO5, SSCL5	IRQ5
28		PB5	GTIOC2B, GTIOC2B#	TXD5, SMOSI5, SSDA5	
29	VCC				
30		PB4	POE8#, GTETRG, GTECLKD	CTS5#, RTS5#, SS5#	IRQ3
31	VSS				
32		PB3	MTIOC0A, MTIOC0A#, CACREF	SCK6, RSPCKA	
33		PB2	MTIOC0B, MTIOC0B#, TMRI0, ADSM0	TXD6, SMOSI6, SSDA6, SDA0	
34		PB1	MTIOC0C, MTIOC0C#, TMCI0, ADSM1	RXD6, SMISO6, SSCL6, SCL0	
35		PB0	MTIOC0D, MTIOC0D#, TMO0	TXD6, SMOSI6, SSDA6, MOSIA	ADTRG2#
36		PA5	MTIOC1A, MTIOC1A#, TMCI3	RXD6, SMISO6, SSCL6, MISOA	IRQ1, ADTRG1#
37		PA4	MTIOC1B, MTIOC1B#, TMCI7	SCK6, RSPCKA	ADTRG0#
38		PA3	MTIOC2A, MTIOC2A#, TMRI7, GTADSM0	SSLA0	
39		PA2	MTIOC2B, MTIOC2B#, TMO7, GTADSM1	CTS6#, RTS6#, SS6#, SSLA1	
40		PA1	MTIOC6A, MTIOC6A#, TMO4	SSLA2, CRXD0	ADTRG0#
41		PA0	MTIOC6C, MTIOC6C#, TMO2	SSLA3, CTXD0	
42	VCC				
43		P96	POE4#		IRQ4
44	VSS				
45		P95	MTIOC6B, MTIOC6B#		
46		P94	MTIOC7A, MTIOC7A#		
47		P93	MTIOC7B, MTIOC7B#		
48		P92	MTIOC6D, MTIOC6D#		
49		P91	MTIOC7C, MTIOC7C#		
50		P90	MTIOC7D, MTIOC7D#		
51		P76	MTIOC4D, MTIOC4D#, GTIOC2B, GTIOC2B#		

Table 1.8 List of Pins and Pin Functions (64-Pin LFQFP) (2/2)

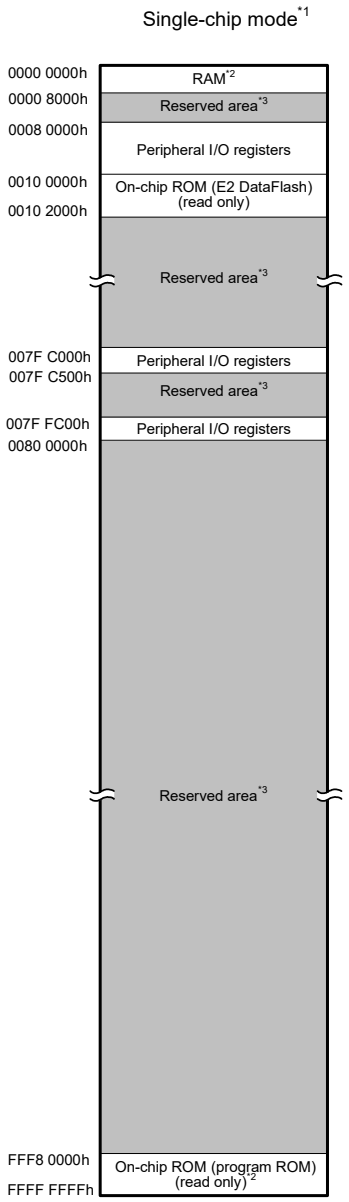
Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, CAC)	Communications (SCI, RSPI, RIIC)	Others
54		P46			AN102, CMPC12, CMPC13, CMPC30, CMPC31
55		P45			AN101, CMPC02, CMPC03, CMPC20, CMPC21
56		P44			AN100, CMPC10, CMPC11, CMPC32, CMPC33
57		P42			AN002
58		P41			AN001
59		P40			AN000, CMPC00, CMPC01, CMPC22, CMPC23
60	AVCC1				
61	AVCC0				
62	AVSS0				
63	AVSS1				
64		P11	MTIOC3A, MTCLKC, TMO3		IRQ1

(9) Floating-point status word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

2.3 Accumulator

The accumulator (ACC0 or ACC1) is a 72-bit register used for DSP instructions. The accumulator is handled as a 96-bit register for reading and writing. At this time, when bits 95 to 72 of the accumulator are read, the value where the value of bit 71 is sign extended is read. Writing to bits 95 to 72 of the accumulator is ignored. ACC0 is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in ACC0 is modified by execution of the instruction.
Use the MVTACGU, MVTACHI, and MVTACLO instructions for writing to the accumulator. The MVTACGU, MVTACHI, and MVTACLO instructions write data to bits 95 to 64, the higher-order 32 bits (bits 63 to 32), and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions for reading data from the accumulator. The MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions read data from the guard bits (bits 95 to 64), higher-order 32 bits (bits 63 to 32), the middle 32 bits (bits 47 to 16), and the lower-order 32 bits (bits 31 to 0), respectively.



Note 1. The address space in boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)		E2 DataFlash (bytes)	
Capacity	**Address**	**Capacity**	**Address**	**Capacity**	**Address**
512 K	FFF8 0000h to FFFF FFFFh	32 K	0000 0000h to 0000 7FFFh	8 K	0010 0000h to 0010 1FFFh
384 K	FFFA 0000h to FFFF FFFFh				
256 K	FFFC 0000h to FFFF FFFFh				
256 K	FFFC 0000h to FFFF FFFFh	16 K	0000 0000h to 0000 3FFFh		
128 K	FFFE 0000h to FFFF FFFFh				

Note: See Table 1.3 List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map in Each Operating Mode

Table 4.1 List of I/O Registers (Address Order) (3/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 7043h	ICU	Interrupt Request Register 067	IR067	8	8	2 ICLK
0008 7044h	ICU	Interrupt Request Register 068	IR068	8	8	2 ICLK
0008 7045h	ICU	Interrupt Request Register 069	IR069	8	8	2 ICLK
0008 7046h	ICU	Interrupt Request Register 070	IR070	8	8	2 ICLK
0008 7047h	ICU	Interrupt Request Register 071	IR071	8	8	2 ICLK
0008 7058h	ICU	Interrupt Request Register 088	IR088	8	8	2 ICLK
0008 7059h	ICU	Interrupt Request Register 089	IR089	8	8	2 ICLK
0008 7062h	ICU	Interrupt Request Register 098*2	IR098	8	8	2 ICLK
0008 7063h	ICU	Interrupt Request Register 099*2	IR099	8	8	2 ICLK
0008 7064h	ICU	Interrupt Request Register 100*2	IR100	8	8	2 ICLK
0008 7065h	ICU	Interrupt Request Register 101*2	IR101	8	8	2 ICLK
0008 7066h	ICU	Interrupt Request Register 102	IR102	8	8	2 ICLK
0008 7067h	ICU	Interrupt Request Register 103	IR103	8	8	2 ICLK
0008 7068h	ICU	Interrupt Request Register 104	IR104	8	8	2 ICLK
0008 7069h	ICU	Interrupt Request Register 105	IR105	8	8	2 ICLK
0008 706Ah	ICU	Interrupt Request Register 106	IR106	8	8	2 ICLK
0008 706Bh	ICU	Interrupt Request Register 107	IR107	8	8	2 ICLK
0008 706Ch	ICU	Interrupt Request Register 108	IR108	8	8	2 ICLK
0008 706Dh	ICU	Interrupt Request Register 109	IR109	8	8	2 ICLK
0008 706Eh	ICU	Interrupt Request Register 110	IR110	8	8	2 ICLK
0008 706Fh	ICU	Interrupt Request Register 111	IR111	8	8	2 ICLK
0008 7070h	ICU	Interrupt Request Register 112	IR112	8	8	2 ICLK
0008 7071h	ICU	Interrupt Request Register 113	IR113	8	8	2 ICLK
0008 7072h	ICU	Interrupt Request Register 114	IR114	8	8	2 ICLK
0008 7073h	ICU	Interrupt Request Register 115	IR115	8	8	2 ICLK
0008 7074h	ICU	Interrupt Request Register 116	IR116	8	8	2 ICLK
0008 7075h	ICU	Interrupt Request Register 117	IR117	8	8	2 ICLK
0008 7076h	ICU	Interrupt Request Register 118	IR118	8	8	2 ICLK
0008 7077h	ICU	Interrupt Request Register 119	IR119	8	8	2 ICLK
0008 7078h	ICU	Interrupt Request Register 120	IR120	8	8	2 ICLK
0008 7079h	ICU	Interrupt Request Register 121	IR121	8	8	2 ICLK
0008 707Ah	ICU	Interrupt Request Register 122	IR122	8	8	2 ICLK
0008 707Bh	ICU	Interrupt Request Register 123	IR123	8	8	2 ICLK
0008 707Ch	ICU	Interrupt Request Register 124	IR124	8	8	2 ICLK
0008 707Dh	ICU	Interrupt Request Register 125	IR125	8	8	2 ICLK
0008 707Eh	ICU	Interrupt Request Register 126	IR126	8	8	2 ICLK
0008 707Fh	ICU	Interrupt Request Register 127	IR127	8	8	2 ICLK
0008 7080h	ICU	Interrupt Request Register 128	IR128	8	8	2 ICLK
0008 7081h	ICU	Interrupt Request Register 129	IR129	8	8	2 ICLK
0008 7082h	ICU	Interrupt Request Register 130	IR130	8	8	2 ICLK
0008 7083h	ICU	Interrupt Request Register 131	IR131	8	8	2 ICLK
0008 7084h	ICU	Interrupt Request Register 132	IR132	8	8	2 ICLK
0008 7085h	ICU	Interrupt Request Register 133	IR133	8	8	2 ICLK
0008 7086h	ICU	Interrupt Request Register 134	IR134	8	8	2 ICLK
0008 7087h	ICU	Interrupt Request Register 135	IR135	8	8	2 ICLK
0008 7088h	ICU	Interrupt Request Register 136	IR136	8	8	2 ICLK
0008 7089h	ICU	Interrupt Request Register 137	IR137	8	8	2 ICLK
0008 708Ah	ICU	Interrupt Request Register 138	IR138	8	8	2 ICLK
0008 708Bh	ICU	Interrupt Request Register 139	IR139	8	8	2 ICLK
0008 708Ch	ICU	Interrupt Request Register 140	IR140	8	8	2 ICLK
0008 708Dh	ICU	Interrupt Request Register 141	IR141	8	8	2 ICLK
0008 708Eh	ICU	Interrupt Request Register 142	IR142	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (4/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 708Fh	ICU	Interrupt Request Register 143	IR143	8	8	2 ICLK
0008 7090h	ICU	Interrupt Request Register 144	IR144	8	8	2 ICLK
0008 7091h	ICU	Interrupt Request Register 145	IR145	8	8	2 ICLK
0008 7092h	ICU	Interrupt Request Register 146	IR146	8	8	2 ICLK
0008 7095h	ICU	Interrupt Request Register 149	IR149	8	8	2 ICLK
0008 7096h	ICU	Interrupt Request Register 150	IR150	8	8	2 ICLK
0008 7097h	ICU	Interrupt Request Register 151	IR151	8	8	2 ICLK
0008 7098h	ICU	Interrupt Request Register 152	IR152	8	8	2 ICLK
0008 7099h	ICU	Interrupt Request Register 153	IR153	8	8	2 ICLK
0008 709Fh	ICU	Interrupt Request Register 159	IR159	8	8	2 ICLK
0008 70A0h	ICU	Interrupt Request Register 160	IR160	8	8	2 ICLK
0008 70A1h	ICU	Interrupt Request Register 161	IR161	8	8	2 ICLK
0008 70A2h	ICU	Interrupt Request Register 162	IR162	8	8	2 ICLK
0008 70A3h	ICU	Interrupt Request Register 163	IR163	8	8	2 ICLK
0008 70A4h	ICU	Interrupt Request Register 164	IR164	8	8	2 ICLK
0008 70A5h	ICU	Interrupt Request Register 165	IR165	8	8	2 ICLK
0008 70A8h	ICU	Interrupt Request Register 168	IR168	8	8	2 ICLK
0008 70A9h	ICU	Interrupt Request Register 169	IR169	8	8	2 ICLK
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8	2 ICLK
0008 70ACh	ICU	Interrupt Request Register 172	IR172	8	8	2 ICLK
0008 70ADh	ICU	Interrupt Request Register 173	IR173	8	8	2 ICLK
0008 70AEh	ICU	Interrupt Request Register 174	IR174	8	8	2 ICLK
0008 70AFh	ICU	Interrupt Request Register 175	IR175	8	8	2 ICLK
0008 70B0h	ICU	Interrupt Request Register 176	IR176	8	8	2 ICLK
0008 70B1h	ICU	Interrupt Request Register 177	IR177	8	8	2 ICLK
0008 70B2h	ICU	Interrupt Request Register 178	IR178	8	8	2 ICLK
0008 70B3h	ICU	Interrupt Request Register 179	IR179	8	8	2 ICLK
0008 70B4h	ICU	Interrupt Request Register 180	IR180	8	8	2 ICLK
0008 70B5h	ICU	Interrupt Request Register 181	IR181	8	8	2 ICLK
0008 70B6h	ICU	Interrupt Request Register 182	IR182	8	8	2 ICLK
0008 70B7h	ICU	Interrupt Request Register 183	IR183	8	8	2 ICLK
0008 70B8h	ICU	Interrupt Request Register 184	IR184	8	8	2 ICLK
0008 70B9h	ICU	Interrupt Request Register 185	IR185	8	8	2 ICLK
0008 70BAh	ICU	Interrupt Request Register 186	IR186	8	8	2 ICLK
0008 70BBh	ICU	Interrupt Request Register 187	IR187	8	8	2 ICLK
0008 70BCh	ICU	Interrupt Request Register 188	IR188	8	8	2 ICLK
0008 70BDh	ICU	Interrupt Request Register 189	IR189	8	8	2 ICLK
0008 70BEh	ICU	Interrupt Request Register 190	IR190	8	8	2 ICLK
0008 70BFh	ICU	Interrupt Request Register 191	IR191	8	8	2 ICLK
0008 70C0h	ICU	Interrupt Request Register 192	IR192	8	8	2 ICLK
0008 70C1h	ICU	Interrupt Request Register 193	IR193	8	8	2 ICLK
0008 70C2h	ICU	Interrupt Request Register 194	IR194	8	8	2 ICLK
0008 70C3h	ICU	Interrupt Request Register 195	IR195	8	8	2 ICLK
0008 70C4h	ICU	Interrupt Request Register 196	IR196	8	8	2 ICLK
0008 70C5h	ICU	Interrupt Request Register 197	IR197	8	8	2 ICLK
0008 70CAh	ICU	Interrupt Request Register 202*2	IR202	8	8	2 ICLK
0008 70CBh	ICU	Interrupt Request Register 203*2	IR203	8	8	2 ICLK
0008 70CCh	ICU	Interrupt Request Register 204*2	IR204	8	8	2 ICLK
0008 70CDh	ICU	Interrupt Request Register 205*2	IR205	8	8	2 ICLK
0008 70CEh	ICU	Interrupt Request Register 206*2	IR206	8	8	2 ICLK
0008 70CFh	ICU	Interrupt Request Register 207*2	IR207	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (8/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 7207h	ICU	Interrupt Request Enable Register 07	IER07	8	8	2 ICLK
0008 7208h	ICU	Interrupt Request Enable Register 08	IER08	8	8	2 ICLK
0008 720Bh	ICU	Interrupt Request Enable Register 0B	IER0B	8	8	2 ICLK
0008 720Ch	ICU	Interrupt Request Enable Register 0C	IER0C	8	8	2 ICLK
0008 720Dh	ICU	Interrupt Request Enable Register 0D	IER0D	8	8	2 ICLK
0008 720Eh	ICU	Interrupt Request Enable Register 0E	IER0E	8	8	2 ICLK
0008 720Fh	ICU	Interrupt Request Enable Register 0F	IER0F	8	8	2 ICLK
0008 7210h	ICU	Interrupt Request Enable Register 10	IER10	8	8	2 ICLK
0008 7211h	ICU	Interrupt Request Enable Register 11	IER11	8	8	2 ICLK
0008 7212h	ICU	Interrupt Request Enable Register 12	IER12	8	8	2 ICLK
0008 7213h	ICU	Interrupt Request Enable Register 13	IER13	8	8	2 ICLK
0008 7214h	ICU	Interrupt Request Enable Register 14	IER14	8	8	2 ICLK
0008 7215h	ICU	Interrupt Request Enable Register 15	IER15	8	8	2 ICLK
0008 7216h	ICU	Interrupt Request Enable Register 16	IER16	8	8	2 ICLK
0008 7217h	ICU	Interrupt Request Enable Register 17	IER17	8	8	2 ICLK
0008 7218h	ICU	Interrupt Request Enable Register 18	IER18	8	8	2 ICLK
0008 7219h	ICU	Interrupt Request Enable Register 19*2	IER19	8	8	2 ICLK
0008 721Ah	ICU	Interrupt Request Enable Register 1A*2	IER1A	8	8	2 ICLK
0008 721Bh	ICU	Interrupt Request Enable Register 1B	IER1B	8	8	2 ICLK
0008 721Ch	ICU	Interrupt Request Enable Register 1C	IER1C	8	8	2 ICLK
0008 721Dh	ICU	Interrupt Request Enable Register 1D*2	IER1D	8	8	2 ICLK
0008 721Eh	ICU	Interrupt Request Enable Register 1E	IER1E	8	8	2 ICLK
0008 721Fh	ICU	Interrupt Request Enable Register 1F	IER1F	8	8	2 ICLK
0008 72E0h	ICU	Software Interrupt Generation Register	SWINTR	8	8	2 ICLK
0008 72F0h	ICU	Fast Interrupt Set Register	FIR	16	16	2 ICLK
0008 7300h	ICU	Interrupt Source Priority Register 000	IPR000	8	8	2 ICLK
0008 7302h	ICU	Interrupt Source Priority Register 002	IPR002	8	8	2 ICLK
0008 7303h	ICU	Interrupt Source Priority Register 003	IPR003	8	8	2 ICLK
0008 7304h	ICU	Interrupt Source Priority Register 004	IPR004	8	8	2 ICLK
0008 7305h	ICU	Interrupt Source Priority Register 005	IPR005	8	8	2 ICLK
0008 7306h	ICU	Interrupt Source Priority Register 006	IPR006	8	8	2 ICLK
0008 7307h	ICU	Interrupt Source Priority Register 007	IPR007	8	8	2 ICLK
0008 7320h	ICU	Interrupt Source Priority Register 032	IPR032	8	8	2 ICLK
0008 7321h	ICU	Interrupt Source Priority Register 033	IPR033	8	8	2 ICLK
0008 7322h	ICU	Interrupt Source Priority Register 034	IPR034	8	8	2 ICLK
0008 7328h	ICU	Interrupt Source Priority Register 040*2	IPR040	8	8	2 ICLK
0008 7329h	ICU	Interrupt Source Priority Register 041*2	IPR041	8	8	2 ICLK
0008 732Ch	ICU	Interrupt Source Priority Register 044	IPR044	8	8	2 ICLK
0008 7330h	ICU	Interrupt Source Priority Register 048*2	IPR048	8	8	2 ICLK
0008 7331h	ICU	Interrupt Source Priority Register 049*2	IPR049	8	8	2 ICLK
0008 7332h	ICU	Interrupt Source Priority Register 050*2	IPR050	8	8	2 ICLK
0008 7333h	ICU	Interrupt Source Priority Register 051*2	IPR051	8	8	2 ICLK
0008 7334h	ICU	Interrupt Source Priority Register 052*2	IPR052	8	8	2 ICLK
0008 7335h	ICU	Interrupt Source Priority Register 053*2	IPR053	8	8	2 ICLK
0008 7336h	ICU	Interrupt Source Priority Register 054*2	IPR054	8	8	2 ICLK
0008 7337h	ICU	Interrupt Source Priority Register 055*2	IPR055	8	8	2 ICLK
0008 7338h	ICU	Interrupt Source Priority Register 056*2	IPR056	8	8	2 ICLK
0008 7339h	ICU	Interrupt Source Priority Register 057	IPR057	8	8	2 ICLK
0008 733Bh	ICU	Interrupt Source Priority Register 059*2	IPR059	8	8	2 ICLK
0008 733Ch	ICU	Interrupt Source Priority Register 060*2	IPR060	8	8	2 ICLK
0008 733Dh	ICU	Interrupt Source Priority Register 061*2	IPR061	8	8	2 ICLK
0008 733Eh	ICU	Interrupt Source Priority Register 062*2	IPR062	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (15/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 94D4h	S12AD2	A/D Channel Select Register C0	ADANSC0	16	16	2 or 3 PCLKB
0008 94D9h	S12AD2	A/D Group C Trigger Select Register	ADGCTRGR	8	8	2 or 3 PCLKB
0008 94DFh	S12AD2	A/D Sampling State Register O	ADSSTRO	8	8	2 or 3 PCLKB
0008 94E0h	S12AD2	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB
0008 94E1h	S12AD2	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB
0008 94E2h	S12AD2	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB
0008 94E3h	S12AD2	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB
0008 94E4h	S12AD2	A/D Sampling State Register 4	ADSSTR4	8	8	2 or 3 PCLKB
0008 94E5h	S12AD2	A/D Sampling State Register 5	ADSSTR5	8	8	2 or 3 PCLKB
0008 94E6h	S12AD2	A/D Sampling State Register 6	ADSSTR6	8	8	2 or 3 PCLKB
0008 94E7h	S12AD2	A/D Sampling State Register 7	ADSSTR7	8	8	2 or 3 PCLKB
0008 94E8h	S12AD2	A/D Sampling State Register 8	ADSSTR8	8	8	2 or 3 PCLKB
0008 94E9h	S12AD2	A/D Sampling State Register 9	ADSSTR9	8	8	2 or 3 PCLKB
0008 94EAh	S12AD2	A/D Sampling State Register 10	ADSSTR10	8	8	2 or 3 PCLKB
0008 94EBh	S12AD2	A/D Sampling State Register 11	ADSSTR11	8	8	2 or 3 PCLKB
0008 A020h	SCI1	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A021h	SCI1	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A022h	SCI1	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A023h	SCI1	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A024h	SCI1	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A025h	SCI1	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A026h	SMCI1	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A027h	SCI1	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A028h	SCI1	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A029h	SCI1	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A02Ah	SCI1	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A02Bh	SCI1	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A02Ch	SCI1	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A02Dh	SCI1	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A02Eh	SCI1	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB
0008 A02Eh	SCI1	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB
0008 A02Fh	SCI1	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 A030h	SCI1	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB
0008 A030h	SCI1	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 A031h	SCI1	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 A032h	SCI1	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 A0A0h	SCI5	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A0A1h	SCI5	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A0A2h	SCI5	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A0A3h	SCI5	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A0A4h	SCI5	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A0A5h	SCI5	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A0A6h	SMCI5	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A0A7h	SCI5	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A0A8h	SCI5	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A0A9h	SCI5	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A0AAh	SCI5	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A0ABh	SCI5	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A0ACh	SCI5	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A0ADh	SCI5	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A0AEh	SCI5	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB
0008 A0AEh	SCI5	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (26/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
000A 8462h	RSCAN	Receive Buffer Register 12AH*2	RMIDH12	16	16	2 or 3 PCLKB
000A 8464h	RSCAN	Receive Buffer Register 12BL*2	RMTS12	16	16	2 or 3 PCLKB
000A 8466h	RSCAN	Receive Buffer Register 12BH*2	RMPTR12	16	16	2 or 3 PCLKB
000A 8468h	RSCAN	Receive Buffer Register 12CL*2	RMDF012	16	16	2 or 3 PCLKB
000A 846Ah	RSCAN	Receive Buffer Register 12CH*2	RMDF112	16	16	2 or 3 PCLKB
000A 846Ch	RSCAN	Receive Buffer Register 12DL*2	RMDF212	16	16	2 or 3 PCLKB
000A 846Eh	RSCAN	Receive Buffer Register 12DH*2	RMDF312	16	16	2 or 3 PCLKB
000A 8470h	RSCAN	Receive Buffer Register 13AL*2	RMIDL13	16	16	2 or 3 PCLKB
000A 8472h	RSCAN	Receive Buffer Register 13AH*2	RMIDH13	16	16	2 or 3 PCLKB
000A 8474h	RSCAN	Receive Buffer Register 13BL*2	RMTS13	16	16	2 or 3 PCLKB
000A 8476h	RSCAN	Receive Buffer Register 13BH*2	RMPTR13	16	16	2 or 3 PCLKB
000A 8478h	RSCAN	Receive Buffer Register 13CL*2	RMDF013	16	16	2 or 3 PCLKB
000A 847Ah	RSCAN	Receive Buffer Register 13CH*2	RMDF113	16	16	2 or 3 PCLKB
000A 847Ch	RSCAN	Receive Buffer Register 13DL*2	RMDF213	16	16	2 or 3 PCLKB
000A 847Eh	RSCAN	Receive Buffer Register 13DH*2	RMDF313	16	16	2 or 3 PCLKB
000A 8480h	RSCAN	Receive Buffer Register 14AL*2	RMIDL14	16	16	2 or 3 PCLKB
000A 8482h	RSCAN	Receive Buffer Register 14AH*2	RMIDH14	16	16	2 or 3 PCLKB
000A 8484h	RSCAN	Receive Buffer Register 14BL*2	RMTS14	16	16	2 or 3 PCLKB
000A 8486h	RSCAN	Receive Buffer Register 14BH*2	RMPTR14	16	16	2 or 3 PCLKB
000A 8488h	RSCAN	Receive Buffer Register 14CL*2	RMDF014	16	16	2 or 3 PCLKB
000A 848Ah	RSCAN	Receive Buffer Register 14CH*2	RMDF114	16	16	2 or 3 PCLKB
000A 848Ch	RSCAN	Receive Buffer Register 14DL*2	RMDF214	16	16	2 or 3 PCLKB
000A 848Eh	RSCAN	Receive Buffer Register 14DH*2	RMDF314	16	16	2 or 3 PCLKB
000A 8490h	RSCAN	Receive Buffer Register 15AL*2	RMIDL15	16	16	2 or 3 PCLKB
000A 8492h	RSCAN	Receive Buffer Register 15AH*2	RMIDH15	16	16	2 or 3 PCLKB
000A 8494h	RSCAN	Receive Buffer Register 15BL*2	RMTS15	16	16	2 or 3 PCLKB
000A 8496h	RSCAN	Receive Buffer Register 15BH*2	RMPTR15	16	16	2 or 3 PCLKB
000A 8498h	RSCAN	Receive Buffer Register 15CL*2	RMDF015	16	16	2 or 3 PCLKB
000A 849Ah	RSCAN	Receive Buffer Register 15CH*2	RMDF115	16	16	2 or 3 PCLKB
000A 849Ch	RSCAN	Receive Buffer Register 15DL*2	RMDF215	16	16	2 or 3 PCLKB
000A 849Eh	RSCAN	Receive Buffer Register 15DH*2	RMDF315	16	16	2 or 3 PCLKB
000A 8580h to 000A 859Fh	RSCAN	RAM Test Register 0 to 15*2	RPGACC0 to 15	16	16	2 or 3 PCLKB
000A 85A0h	RSCAN	Receive FIFO Access Register 0AL*2	RFIDL0	16	16	2 or 3 PCLKB
000A 85A0h	RSCAN	RAM Test Register 16*2	RPGACC16	16	16	2 or 3 PCLKB
000A 85A2h	RSCAN	Receive FIFO Access Register 0AH*2	RFIDH0	16	16	2 or 3 PCLKB
000A 85A2h	RSCAN	RAM Test Register 17*2	RPGACC17	16	16	2 or 3 PCLKB
000A 85A4h	RSCAN	Receive FIFO Access Register 0BL*2	RFTS0	16	16	2 or 3 PCLKB
000A 85A4h	RSCAN	RAM Test Register 18*2	RPGACC18	16	16	2 or 3 PCLKB
000A 85A6h	RSCAN	Receive FIFO Access Register 0BH*2	RFPTR0	16	16	2 or 3 PCLKB
000A 85A6h	RSCAN	RAM Test Register 19*2	RPGACC19	16	16	2 or 3 PCLKB
000A 85A8h	RSCAN	Receive FIFO Access Register 0CL*2	RFDF00	16	16	2 or 3 PCLKB
000A 85A8h	RSCAN	RAM Test Register 20*2	RPGACC20	16	16	2 or 3 PCLKB
000A 85AAh	RSCAN	Receive FIFO Access Register 0CH*2	RFDF10	16	16	2 or 3 PCLKB
000A 85AAh	RSCAN	RAM Test Register 21*2	RPGACC21	16	16	2 or 3 PCLKB
000A 85ACh	RSCAN	Receive FIFO Access Register 0DL*2	RFDF20	16	16	2 or 3 PCLKB
000A 85ACh	RSCAN	RAM Test Register 22*2	RPGACC22	16	16	2 or 3 PCLKB
000A 85AEh	RSCAN	Receive FIFO Access Register 0DH*2	RFDF30	16	16	2 or 3 PCLKB
000A 85AEh	RSCAN	RAM Test Register 23*2	RPGACC23	16	16	2 or 3 PCLKB
000A 85B0h	RSCAN	Receive FIFO Access Register 1AL*2	RFIDL1	16	16	2 or 3 PCLKB
000A 85B0h	RSCAN	RAM Test Register 24*2	RPGACC24	16	16	2 or 3 PCLKB
000A 85B2h	RSCAN	Receive FIFO Access Register 1AH*2	RFIDH1	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (28/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000A 8614h	RSCAN	RAM Test Register 74*2	RPGACC74	16	16	2 or 3 PCLKB
000A 8616h	RSCAN0	Transmit Buffer Register 1BH*2	TMPTR1	16	16	2 or 3 PCLKB
000A 8616h	RSCAN	RAM Test Register 75*2	RPGACC75	16	16	2 or 3 PCLKB
000A 8618h	RSCAN0	Transmit Buffer Register 1CL*2	TMDF01	16	16	2 or 3 PCLKB
000A 8618h	RSCAN	RAM Test Register 76*2	RPGACC76	16	16	2 or 3 PCLKB
000A 861Ah	RSCAN0	Transmit Buffer Register 1CH*2	TMDF11	16	16	2 or 3 PCLKB
000A 861Ah	RSCAN	RAM Test Register 77*2	RPGACC77	16	16	2 or 3 PCLKB
000A 861Ch	RSCAN0	Transmit Buffer Register 1DL*2	TMDF21	16	16	2 or 3 PCLKB
000A 861Ch	RSCAN	RAM Test Register 78*2	RPGACC78	16	16	2 or 3 PCLKB
000A 861Eh	RSCAN0	Transmit Buffer Register 1DH*2	TMDF31	16	16	2 or 3 PCLKB
000A 861Eh	RSCAN	RAM Test Register 79*2	RPGACC79	16	16	2 or 3 PCLKB
000A 8620h	RSCAN0	Transmit Buffer Register 2AL*2	TMIDL2	16	16	2 or 3 PCLKB
000A 8620h	RSCAN	RAM Test Register 80*2	RPGACC80	16	16	2 or 3 PCLKB
000A 8622h	RSCAN0	Transmit Buffer Register 2AH*2	TMIDH2	16	16	2 or 3 PCLKB
000A 8622h	RSCAN	RAM Test Register 81*2	RPGACC81	16	16	2 or 3 PCLKB
000A 8624h	RSCAN	RAM Test Register 82*2	RPGACC82	16	16	2 or 3 PCLKB
000A 8626h	RSCAN0	Transmit Buffer Register 2BH*2	TMPTR2	16	16	2 or 3 PCLKB
000A 8626h	RSCAN	RAM Test Register 83*2	RPGACC83	16	16	2 or 3 PCLKB
000A 8628h	RSCAN0	Transmit Buffer Register 2CL*2	TMDF02	16	16	2 or 3 PCLKB
000A 8628h	RSCAN	RAM Test Register 84*2	RPGACC84	16	16	2 or 3 PCLKB
000A 862Ah	RSCAN0	Transmit Buffer Register 2CH*2	TMDF12	16	16	2 or 3 PCLKB
000A 862Ah	RSCAN	RAM Test Register 85*2	RPGACC85	16	16	2 or 3 PCLKB
000A 862Ch	RSCAN0	Transmit Buffer Register 2DL*2	TMDF22	16	16	2 or 3 PCLKB
000A 862Ch	RSCAN	RAM Test Register 86*2	RPGACC86	16	16	2 or 3 PCLKB
000A 862Eh	RSCAN0	Transmit Buffer Register 2DH*2	TMDF32	16	16	2 or 3 PCLKB
000A 862Eh	RSCAN	RAM Test Register 87*2	RPGACC87	16	16	2 or 3 PCLKB
000A 8630h	RSCAN0	Transmit Buffer Register 3AL*2	TMIDL3	16	16	2 or 3 PCLKB
000A 8630h	RSCAN	RAM Test Register 88*2	RPGACC88	16	16	2 or 3 PCLKB
000A 8632h	RSCAN0	Transmit Buffer Register 3AH*2	TMIDH3	16	16	2 or 3 PCLKB
000A 8632h	RSCAN	RAM Test Register 89*2	RPGACC89	16	16	2 or 3 PCLKB
000A 8634h	RSCAN	RAM Test Register 90*2	RPGACC90	16	16	2 or 3 PCLKB
000A 8636h	RSCAN0	Transmit Buffer Register 3BH*2	TMPTR3	16	16	2 or 3 PCLKB
000A 8636h	RSCAN	RAM Test Register 91*2	RPGACC91	16	16	2 or 3 PCLKB
000A 8638h	RSCAN0	Transmit Buffer Register 3CL*2	TMDF03	16	16	2 or 3 PCLKB
000A 8638h	RSCAN	RAM Test Register 92*2	RPGACC92	16	16	2 or 3 PCLKB
000A 863Ah	RSCAN0	Transmit Buffer Register 3CH*2	TMDF13	16	16	2 or 3 PCLKB
000A 863Ah	RSCAN	RAM Test Register 93*2	RPGACC93	16	16	2 or 3 PCLKB
000A 863Ch	RSCAN0	Transmit Buffer Register 3DL*2	TMDF23	16	16	2 or 3 PCLKB
000A 863Ch	RSCAN	RAM Test Register 94*2	RPGACC94	16	16	2 or 3 PCLKB
000A 863Eh	RSCAN0	Transmit Buffer Register 3DH*2	TMDF33	16	16	2 or 3 PCLKB
000A 863Eh	RSCAN	RAM Test Register 95*2	RPGACC95	16	16	2 or 3 PCLKB
000A 8640h to 000A 867Eh	RSCAN	RAM Test Register 96 to 127*2	RPGACC96 to 127	16	16	2 or 3 PCLKB
000A 8680h	RSCAN0	Transmit History Buffer Access Register*2	THLACC0	16	16	2 or 3 PCLKB
000C 1200h	MTU3	Timer Control Register	TCR	8	8, 16, 32	4 or 5 PCLKA
000C 1201h	MTU4	Timer Control Register	TCR	8	8	4 or 5 PCLKA
000C 1202h	MTU3	Timer Mode Register 1	TMDR1	8	8, 16	4 or 5 PCLKA
000C 1203h	MTU4	Timer Mode Register 1	TMDR1	8	8	4 or 5 PCLKA
000C 1204h	MTU3	Timer I/O Control Register H	TIORH	8	8, 16, 32	4 or 5 PCLKA
000C 1205h	MTU3	Timer I/O Control Register L	TIORL	8	8	4 or 5 PCLKA
000C 1206h	MTU4	Timer I/O Control Register H	TIORH	8	8, 16	4 or 5 PCLKA
000C 1207h	MTU4	Timer I/O Control Register L	TIORL	8	8	4 or 5 PCLKA

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = AVSS1 = AVSS2 = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC	–0.3 to +6.5	V
Input voltage	Port 4, port 5, port 6	V_{in}	–0.3 to VREF + 0.3	V
	Except for port 4, port 5, port 6 and ports for 5 V tolerant*1		–0.3 to VCC + 0.3	V
	Ports for 5 V tolerant*1		–0.3 to +6.5	V
Analog power supply voltage		AVCC0, AVCC1, AVCC2, VREF	–0.3 to +6.5	V
Analog input voltage	When AN000 to AN003, AN100 to AN103, AN200 to AN211 used	V_{AN}	–0.3 to VREF + 0.3	V
	When AN016, AN116, CVREFC0, CVREFC1 used		–0.3 to VCC + 0.3	
Operating temperature		T_{opr}	–40 to +85	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the AVCC1 and AVSS1 pins, between the AVCC2 and AVSS2 pins, between the VREF and AVSS2 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.
Connect the VCL pin to a VSS pin via a 4.7 µF capacitor. The capacitor must be placed close to the pin.
Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered.
The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.
Even if –0.3 to +6.5 V is input to 5-V tolerant ports, it will not cause problems such as damage to the MCU.
Note 1. Ports B1 and B2 are 5 V tolerant.

Table 5.2 Recommended Operating Voltage Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltages	VCC*1, *2		2.7	—	5.5	V
	VSS		—	0	—	
Analog power supply voltages	AVCC0, AVCC1, AVCC2, VREF*1, *2		VCC	—	5.5	V
	AVSS0, AVSS1, AVSS2		—	0	—	

Note 1. AVCC0/AVCC1/AVCC2/VREF and VCC can be set individually within the operating range.
Note 2. When powering on the VCC and AVCC0/AVCC1/AVCC2/VREF pins, power them on at the same time or the VCC pin first and then the AVCC0/AVCC1/AVCC2/VREF pin.

5.2 DC Characteristics

Table 5.3 DC Characteristics (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)	V_{IH}	VCC × 0.7	—	5.8	V	
	Ports B1, B2 (5 V tolerant)		VCC × 0.8	—	5.8		
	Ports 00 to 02, ports 10, 11, ports 20 to 24, ports 30 to 33, 36, 37, ports 70 to 76, ports 80 to 82, ports 90 to 96, ports A0 to A5, port B0, ports B3 to B7, ports D0 to D7, ports E0 to E5, RES#		VCC × 0.8	—	VCC + 0.3		
	Ports 40 to 47, ports 50 to 55, ports 60 to 65		VREF × 0.8	—	VREF + 0.3		
	RIIC input pin (except for SMBus)	V_{IL}	–0.3	—	VCC × 0.3		
	Ports 40 to 47, ports 50 to 55, ports 60 to 65		–0.3	—	VREF × 0.2		
	Other than RIIC input pin, Other than ports 40 to 47, 50 to 55, or 60 to 65		–0.3	—	VCC × 0.2		
	RIIC input pin (except for SMBus)	ΔV_T	VCC × 0.05	—	—		
	Ports 40 to 47, ports 50 to 55, ports 60 to 65		VREF × 0.1	—	—		
	Other than RIIC input pin, Other than ports 40 to 47, 50 to 55, or 60 to 65		VCC × 0.1	—	—		
Input level voltage (except for Schmitt trigger input pins)	MD	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL (external clock input)		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (SMBus)		2.1	—	VCC + 0.3		VCC ≤ 5.2 V
	MD	V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL (external clock input)		–0.3	—	VCC × 0.2		
	RIIC input pin (SMBus)		–0.3	—	0.8		VCC ≤ 5.2 V

Table 5.6 DC Characteristics (4)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item			Symbol	Chip Version A		Chip Version B		Unit	Test Conditions
				Typ.*3	Max.	Typ.*3	Max.		
Supply current*1	Software standby mode*2	T_a = 25°C	I_{CC}	1.0	55.0	1.5	15.0	µA	
		T_a = 55°C		1.5	60.0	3.0	38.0		
		T_a = 85°C		5.5	260.0	13.0	135.0		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 5 V.

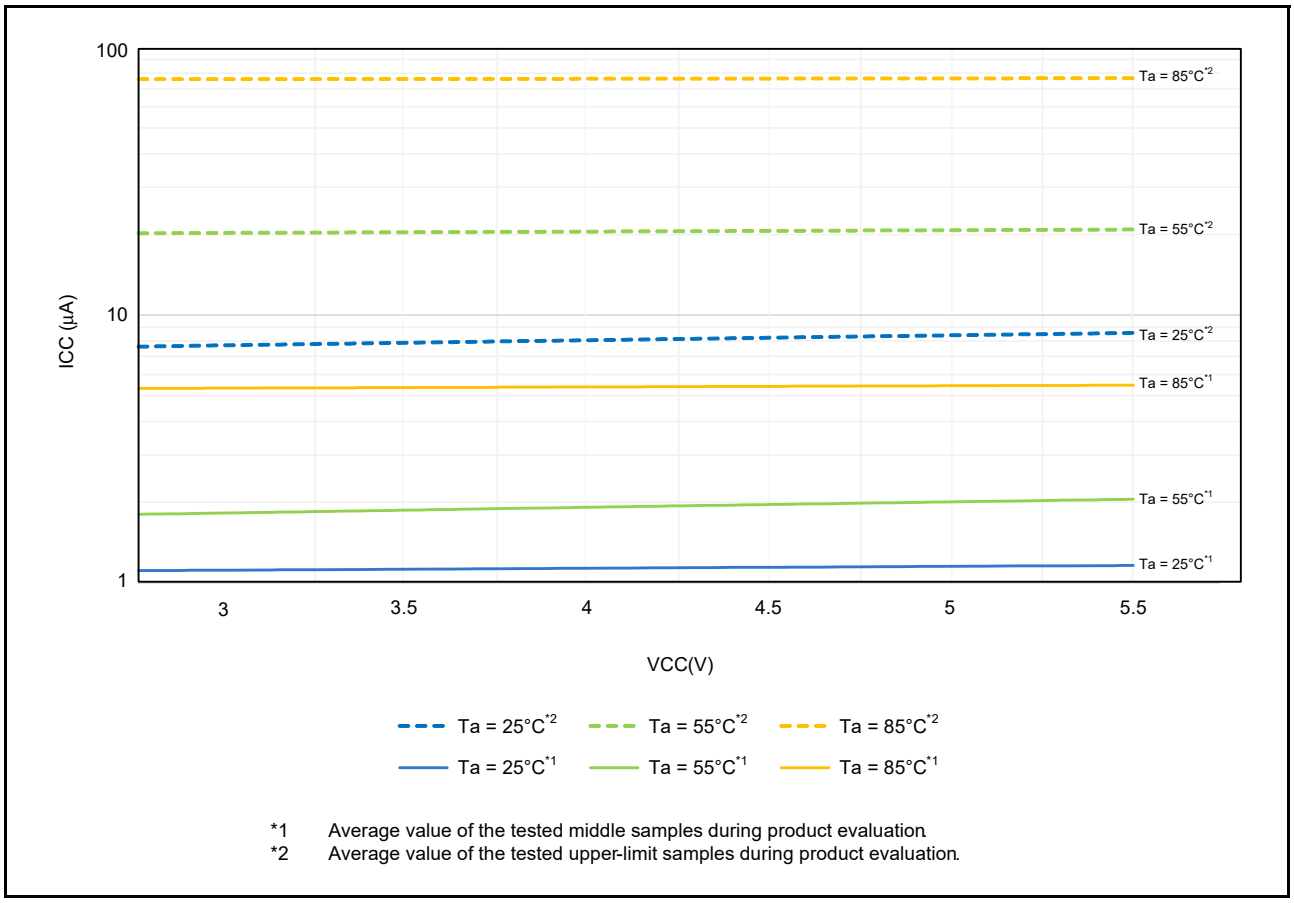


Figure 5.1 Voltage Dependency in Software Standby Mode (Chip Version A) (Reference Data)

5.3 AC Characteristics

5.3.1 Clock Timing

Table 5.14 Operating Frequency Value (High-Speed Operating Mode)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	min.	typ.	max.	Unit
Operating frequency	System clock (ICLK)	f_{max}	—	—	80	MHz
	FlashIF clock (FCLK)*1, *2		—	—	32	
	Peripheral module clock (PCLKA)		—	—	80	
	Peripheral module clock (PCLKB)		—	—	40	
	Peripheral module clock (PCLKD)		—	—	40	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.

Table 5.15 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	min.	typ.	max.	Unit
Operating frequency	System clock (ICLK)	f_{max}	—	—	12	MHz
	FlashIF clock (FCLK)*1, *2		—	—	12	
	Peripheral module clock (PCLKA)		—	—	12	
	Peripheral module clock (PCLKB)		—	—	12	
	Peripheral module clock (PCLKD)		—	—	12	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.

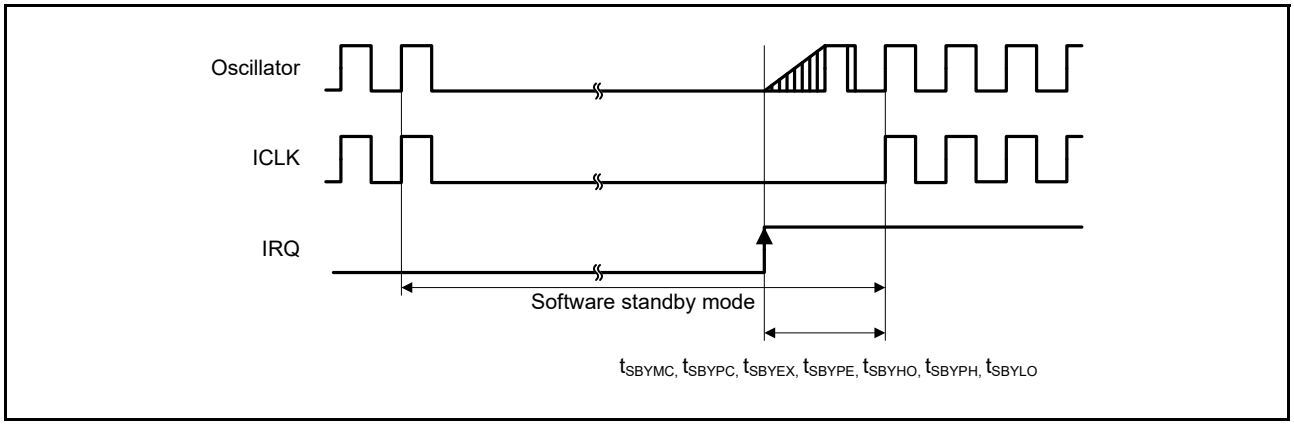


Figure 5.32 Software Standby Mode Recovery Timing

Table 5.20 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	t_{DSLP}	—	2	3.5	µs	Figure 5.33
	Middle-speed mode*3	t_{DSLP}	—	3	4	µs	

Note 1. Oscillators continue oscillating in deep sleep mode.
Note 2. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are 32 MHz.
Note 3. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are 12 MHz.

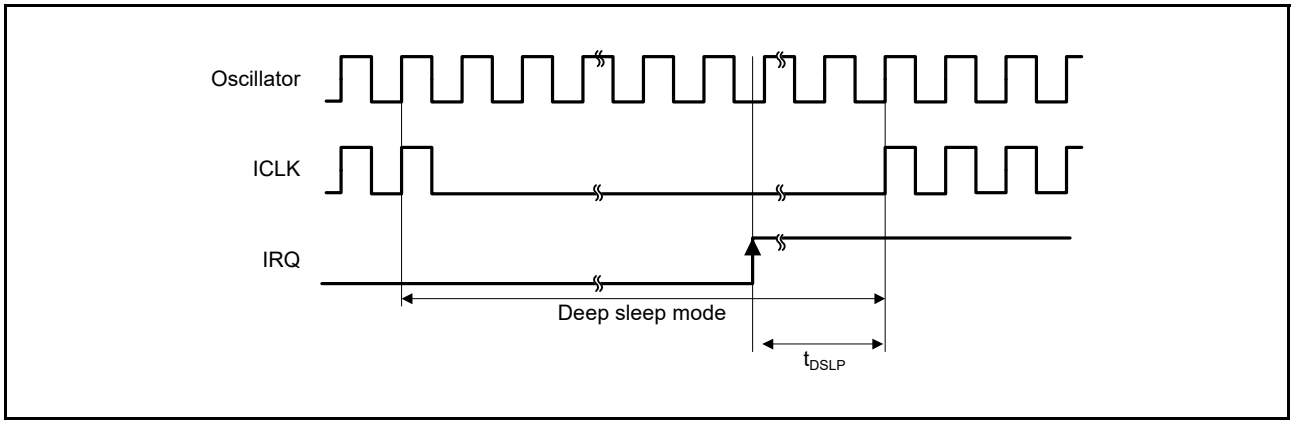


Figure 5.33 Deep Sleep Mode Recovery Timing

Table 5.21 Operating Mode Transition Time

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Mode before Transition	Mode after Transition	ICLK Frequency	Transition Time			Unit
			Min.	Typ.	Max.	
High-speed operating mode	Middle-speed operating modes	8 MHz	—	10	—	µs
Middle-speed operating modes	High-speed operating mode	8 MHz	—	37.5	—	µs

Note: Values when the frequencies of PCLKA, PCLKB, PCLKD, and FCLK are not divided.

Table 5.24 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 =AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C, C = 30pF

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	Figure 5.47
		Slave			6	—		
	RSPCK clock high pulse width	Master	VCC = 4.0 V or above	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 5$	—	ns	
			VCC = 2.7 V or above		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 8$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master	VCC = 4.0 V or above	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 5$	—	ns	
			VCC = 2.7 V or above		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 8$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	VCC = 4.0 V or above	t_{SPCKr}, t_{SPCKf}	—	6	ns	
			VCC = 2.7 V or above		—	10		
		Input			—	0.1	μs/V	
	Data input setup time	Master	VCC = 4.0 V or above	t_{SU}	10	—	ns	Figure 5.48 to Figure 5.51
			VCC = 2.7 V or above		26	—		
		Slave			20	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	0	—		
	SSL setup time	Master		t_{LEAD}	–30 + N*2 × t_{SPcyc}	—	ns	
		Slave			6	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	–30 + N*3 × t_{SPcyc}	—	ns	
		Slave			6	—	t_{Pcyc}	
	Data output delay time	Master	VCC = 4.0 V or above	t_{OD}	—	10	ns	
			VCC = 2.7 V or above		—	14		
		Slave			—	65		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$6 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output		t_{Dr}, t_{Df}	—	10	ns	
		Input			—	1	μs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	10	ns	
		Input			—	1	μs	
	Slave access time			t_{SA}	—	6	t_{Pcyc}	Figure 5.50, Figure 5.51
	Slave output release time			t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

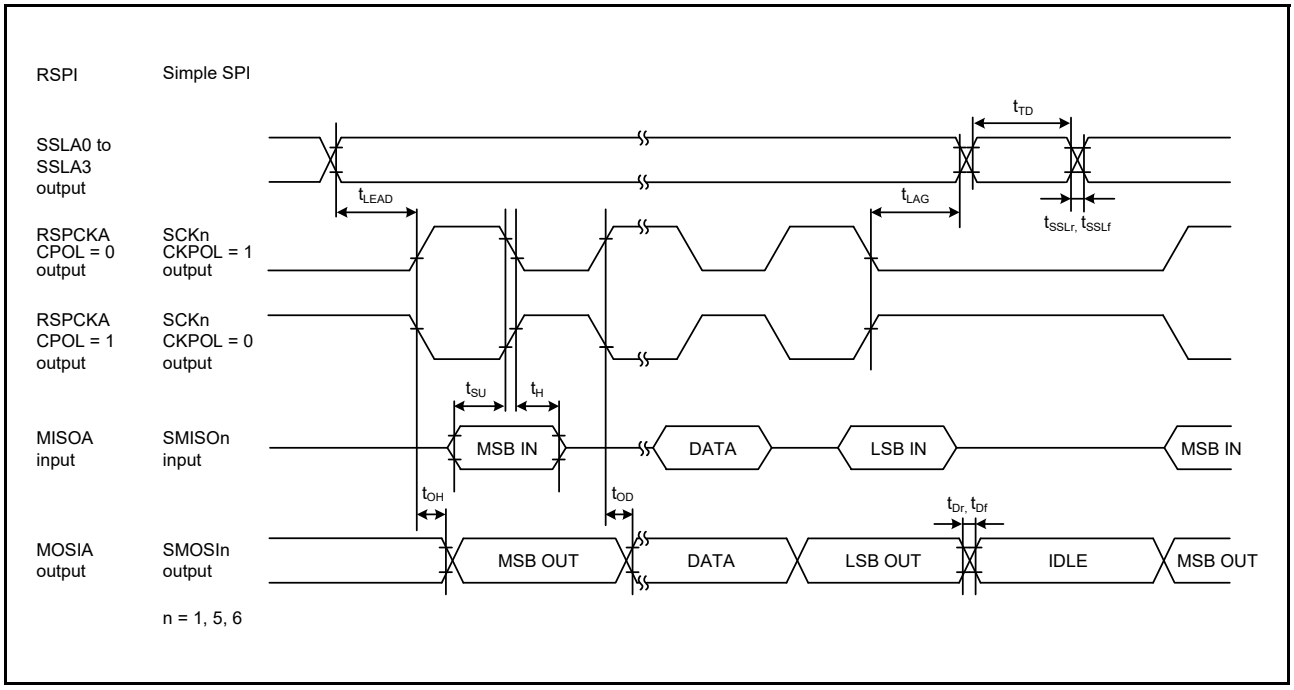


Figure 5.49 RSPI Timing (Master, CPHA = 1) and Simple SPI Clock Timing (Master, CKPH = 0)

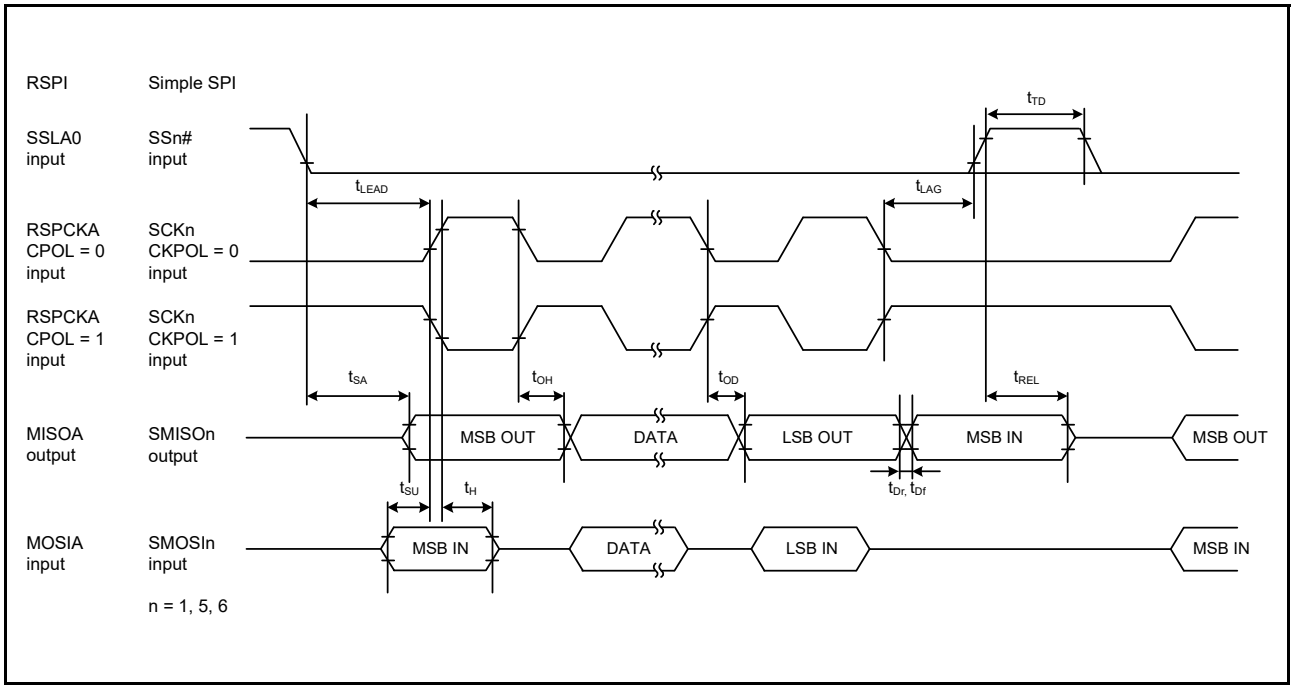


Figure 5.50 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1)

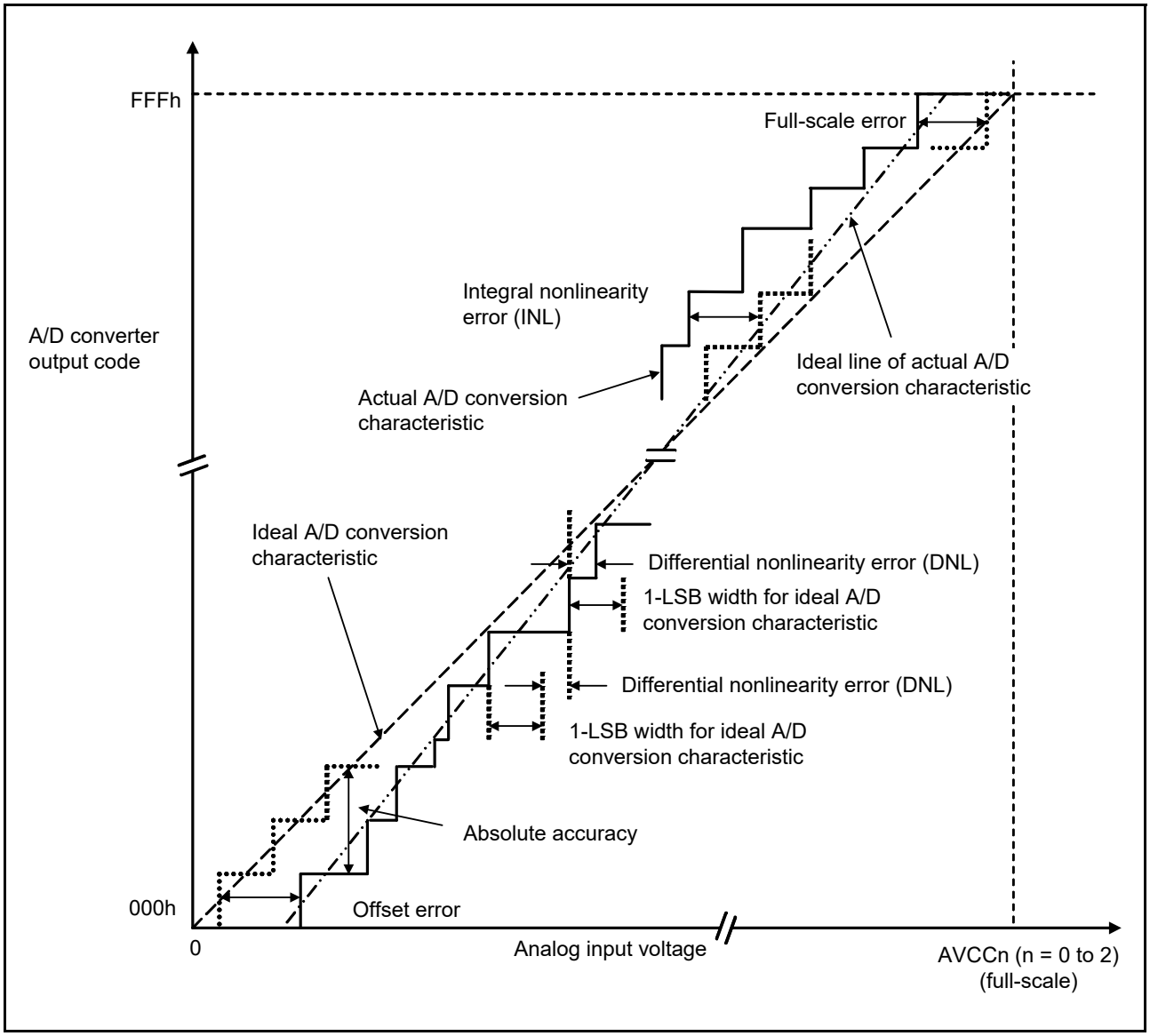


Figure 5.53 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (AVCCn (n = 0 to 2)) is 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

5.6 Comparator Characteristics

Table 5.33 Comparator Characteristics

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Offset voltage	V_{cioff}	—	—	40	mV	
Reference input voltage range	V_{cref}	0	—	VREF	V	
Response time	t_{cr}	—	—	200	ns	VOD = 100 mV CMPCTL.CDFS = 0
	t_{cf}	—	—	200	ns	
Stabilization wait time for input selection	t_{cwait}	300	—	—	ns	
Operation stabilization wait time	t_{cmp}		—	1	µs	

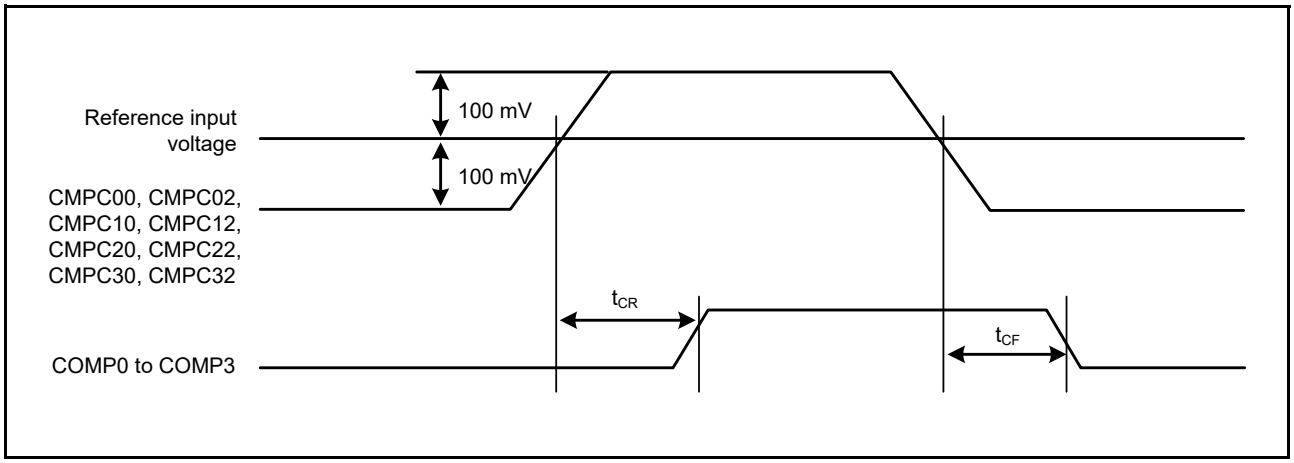


Figure 5.54 Comparator Response Time