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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 17x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f524t8adfn-31

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX24T Group			
		Chip Version B	Chip Version A		
		100 Pins	100 Pins	80 Pins	64Pins
Memory	ROM	512 K/384 K/ 256 Kbytes	256 K/128 Kbytes		
	RAM	32 Kbytes	16 Kbytes		
	E2 DataFlash	8 Kbytes			
Interrupts	External interrupts	NMI, IRQ0 to IRQ7			
DTC	Data transfer controller (DTCa)	Available			
Timers	Multi-function timer pulse unit 3 (MTU3d)	9 channels			
	General PWM timer (GPTB)	4 channels	Not supported		
	Port output enable 3 (POE3b)	Not supported	Available		
	Port output enable 3 (POE3A)	Available	Not supported		
	8-bit timer (TMR)	2 channels × 4 units			
	Compare match timer (CMT)	2 channels × 2 units			
	Independent watchdog timer (IWDTa)	Available			
Communications	Serial communications interfaces (SCIg) [including simple I^2C and simple SPI]	3 channels (SCI1, SCI5, SCI6)			
	I^2C bus interface (RIICa)	1 channel			
	Serial peripheral interface (RSPIb)	1 channel			
	CAN module (RSCAN)	1 channel	Not supported		
12-bit A/D converter (S12ADF) (Internal high-precision channel)		5 channels × 2 units, 12 channels × 1 unit (4 channels × 2 units, 12 channels × 1 unit)		5 channels × 2 units, 7 channels × 1 unit (4 channels × 2 units, 7 channels × 1 unit)	3 channels × 1 unit, 4 channels × 1 unit, 5 channels × 1 unit (3 channels × 1 unit, 3 channels × 1 unit, 5 channels × 1 unit)
	3 channels simultaneous sampling	3 channels/unit 1			
	Programmable gain amplifier	1 channel/unit 0, 3 channels/unit 1			
Comparator C (CMPC)		4 channels			
		Without reference voltage external input	With reference voltage external input		
8-bit D/A converter (DA)		Not supported	Available		
8-bit D/A converter (DAa)		Available	Not supported		
CRC calculator (CRC)		Available			
Packages		100-pin LFQFP	100-pin LFQFP	80-pin LFQFP/LQFP	64-pin LFQFP

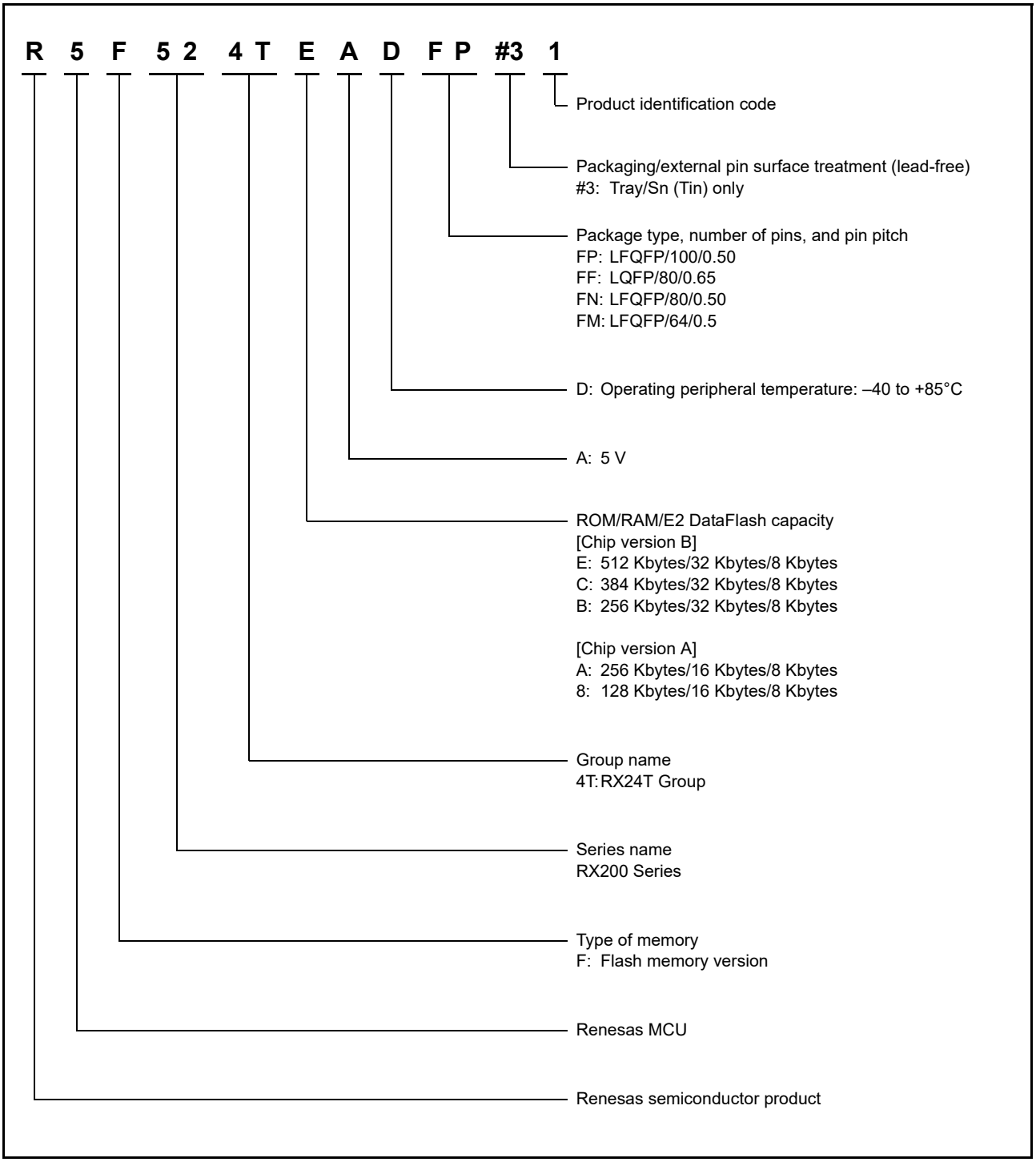


Figure 1.1 How to Read the Product Part Number

Table 1.6 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version A) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, CAC)	Communications (SCI, RSPI, RIIC)	Others
1		PE5			IRQ0
2		P02	MTIOC9D	CTS1#, RTS1#, SS1#	IRQ5, ADST0
3	VSS				
4		P00			IRQ2, ADST1
5	VCL				
6	MD				FINED
7		P01	POE12#		IRQ4, ADST2
8		PE4	MTCLKC, POE10#		IRQ1
9		PE3	MTCLKD, POE11#		IRQ2
10	RES#				
11	XTAL	P37			
12	VSS				
13	EXTAL	P36			
14	VCC				
15		PE2	POE10#		NMI
16		PE1	MTIOC9D, TMO5	CTS5#, RTS5#, SS5#, SSLA3	
17		PE0	MTIOC9B, TMCI1, TMCI5	SSLA2	
18		PD7	MTIOC9A, TMRI1, TMRI5	SSLA1	
19		PD6	MTIOC9C, TMO1	CTS1#, RTS1#, SS1#, SSLA0	IRQ5, ADST0
20		PD5	TMRI0, TMRI6	RXD1, SMISO1, SSCL1	IRQ3
21		PD4	TMCI0, TMCI6	SCK1	IRQ2
22		PD3	TMO0	TXD1, SMOSI1, SSDA1	
23		PD2	TMCI1, TMO4	SCK5, MOSIA	
24		PD1	TMO2	MISOA	
25		PD0	TMO6	RSPCKA	
26		PB7		SCK5	
27		PB6		RXD5, SMISO5, SSCL5	IRQ5
28		PB5		TXD5, SMOSI5, SSDA5	
29	VCC				
30		PB4	POE8#	CTS5#, RTS5#, SS5#	IRQ3
31	VSS				
32		PB3	MTIOC0A, CACREF	SCK6, RSPCKA	
33		PB2	MTIOC0B, TMRI0, ADSM0	TXD6, SMOSI6, SSDA6, SDA0	
34		PB1	MTIOC0C, TMCI0, ADSM1	RXD6, SMISO6, SSCL6, SCL0	
35		PB0	MTIOC0D, TMO0	TXD6, SMOSI6, SSDA6, MOSIA	ADTRG2#
36		PA5	MTIOC1A, TMCI3	RXD6, SMISO6, SSCL6, MISOA	IRQ1, ADTRG1#
37		PA4	MTIOC1B, TMCI7	SCK6, RSPCKA	ADTRG0#
38		PA3	MTIOC2A, TMRI7	SSLA0	
39		PA2	MTIOC2B, TMO7	CTS6#, RTS6#, SS6#, SSLA1	
40		PA1	MTIOC6A, TMO4	SSLA2	ADTRG0#
41		PA0	MTIOC6C, TMO2	SSLA3	
42	VCC				
43		P96	POE4#		IRQ4
44	VSS				
45		P95	MTIOC6B		
46		P94	MTIOC7A		
47		P93	MTIOC7B		
48		P92	MTIOC6D		
49		P91	MTIOC7C		
50		P90	MTIOC7D		
51		P76	MTIOC4D		
52		P75	MTIOC4C		
53		P74	MTIOC3D		
54		P73	MTIOC4B		

Table 1.6 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version A) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, CAC)	Communications (SCI, RSPI, RIIC)	Others
55		P72	MTIOC4A		
56		P71	MTIOC3B		
57		P70	POE0#		IRQ5
58		P33	MTIOC3A, MTCLKA, TMO0	SSLA3	
59		P32	MTIOC3C, MTCLKB, TMO6	SSLA2	
60	VCC				
61		P31	MTIOC0A, MTCLKC, TMRI6	SSLA1	IRQ6
62	VSS				
63		P30	MTIOC0B, MTCLKD, TMCI6	SSLA0	IRQ7, COMP3
64		P24	MTIC5U, TMCI2, TMO6	RSPCKA	COMP0
65		P23	MTIC5V, TMO2, CACREF	MOSIA	COMP1
66		P22	MTIC5W, TMRI2, TMO4	MISOA	ADTRG2#, COMP2
67		P21	MTCLKA, MTIOC9A, TMCI4		IRQ6, ADTRG1#, AN116, CVREFC1
68		P20	MTCLKB, MTIOC9C, TMRI4		IRQ7, ADTRG0#, AN016, CVREFC0
69		P65			AN205
70		P64			AN204
71	AVCC2				
72	VREF				
73	AVSS2				
74		P63			AN203, IRQ7
75		P62			AN202, IRQ6
76		P61			AN201, IRQ5
77		P60			AN200, IRQ4
78		P55			AN211, IRQ3
79		P54			AN210, IRQ2
80		P53			AN209, IRQ1
81		P52			AN208, IRQ0
82		P51			AN207
83		P50			AN206
84		P47			AN103
85		P46			AN102, CMPC12, CMPC13, CMPC30, CMPC31
86		P45			AN101, CMPC02, CMPC03, CMPC20, CMPC21
87		P44			AN100, CMPC10, CMPC11, CMPC32, CMPC33
88		P43			AN003
89		P42			AN002
90		P41			AN001
91		P40			AN000, CMPC00, CMPC01, CMPC22, CMPC23
92	AVCC1				
93	AVCC0				
94	AVSS0				
95	AVSS1				
96		P82	MTIC5U, TMO4	SCK6	
97		P81	MTIC5V, TMCI4	TXD6, SMOSI6, SSDA6	
98		P80	MTIC5W, TMRI4	RXD6, SMISO6, SSCL6	
99		P11	MTIOC3A, MTCLKC, TMO3		IRQ1
100		P10	MTIOC9B, MTCLKD, TMRI3, POE12#	CTS6#, RTS6#, SS6#	IRQ0

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen 32-bit general-purpose registers (R0 to R15). R0 to R15 can be used as data registers or address registers.
R0, a general-purpose register, also functions as the stack pointer (SP).
The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt stack pointer (ISP) and user stack pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Exception table register (EXTB)

The exception table register (EXTB) specifies the address where the exception vector table starts.
Set the EXTB to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(3) Interrupt table register (INTB)

The interrupt table register (INTB) specifies the address where the interrupt vector table starts.
Set the INTB to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(4) Program counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(5) Processor status word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(6) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(7) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(8) Fast interrupt vector register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(9) Floating-point status word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

2.3 Accumulator

The accumulator (ACC0 or ACC1) is a 72-bit register used for DSP instructions. The accumulator is handled as a 96-bit register for reading and writing. At this time, when bits 95 to 72 of the accumulator are read, the value where the value of bit 71 is sign extended is read. Writing to bits 95 to 72 of the accumulator is ignored. ACC0 is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in ACC0 is modified by execution of the instruction.
Use the MVTACGU, MVTACHI, and MVTACLO instructions for writing to the accumulator. The MVTACGU, MVTACHI, and MVTACLO instructions write data to bits 95 to 64, the higher-order 32 bits (bits 63 to 32), and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions for reading data from the accumulator. The MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions read data from the guard bits (bits 95 to 64), higher-order 32 bits (bits 63 to 32), the middle 32 bits (bits 47 to 16), and the lower-order 32 bits (bits 31 to 0), respectively.

Table 4.1 List of I/O Registers (Address Order) (2/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32	1 ICLK
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32	1 ICLK
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32	1 ICLK
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32	1 ICLK
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32	1 ICLK
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32	1 ICLK
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32	1 ICLK
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32	1 ICLK
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32	1 ICLK
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32	1 ICLK
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32	1 ICLK
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32	1 ICLK
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32	1 ICLK
0008 6520h	MPU	Region Search Address Register	MPSA	32	32	1 ICLK
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16	1 ICLK
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16	1 ICLK
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32	1 ICLK
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32	1 ICLK
0008 7010h	ICU	Interrupt Request Register 016	IR016	8	8	2 ICLK
0008 7017h	ICU	Interrupt Request Register 023	IR023	8	8	2 ICLK
0008 701Bh	ICU	Interrupt Request Register 027	IR027	8	8	2 ICLK
0008 701Ch	ICU	Interrupt Request Register 028	IR028	8	8	2 ICLK
0008 701Dh	ICU	Interrupt Request Register 029	IR029	8	8	2 ICLK
0008 701Eh	ICU	Interrupt Request Register 030	IR030	8	8	2 ICLK
0008 701Fh	ICU	Interrupt Request Register 031	IR031	8	8	2 ICLK
0008 7020h	ICU	Interrupt Request Register 032	IR032	8	8	2 ICLK
0008 7021h	ICU	Interrupt Request Register 033	IR033	8	8	2 ICLK
0008 7022h	ICU	Interrupt Request Register 034	IR034	8	8	2 ICLK
0008 7028h	ICU	Interrupt Request Register 040*2	IR040	8	8	2 ICLK
0008 7029h	ICU	Interrupt Request Register 041*2	IR041	8	8	2 ICLK
0008 702Ch	ICU	Interrupt Request Register 044	IR044	8	8	2 ICLK
0008 702Dh	ICU	Interrupt Request Register 045	IR045	8	8	2 ICLK
0008 702Eh	ICU	Interrupt Request Register 046	IR046	8	8	2 ICLK
0008 702Fh	ICU	Interrupt Request Register 047	IR047	8	8	2 ICLK
0008 7030h	ICU	Interrupt Request Register 048*2	IR048	8	8	2 ICLK
0008 7031h	ICU	Interrupt Request Register 049*2	IR049	8	8	2 ICLK
0008 7032h	ICU	Interrupt Request Register 050*2	IR050	8	8	2 ICLK
0008 7033h	ICU	Interrupt Request Register 051*2	IR051	8	8	2 ICLK
0008 7034h	ICU	Interrupt Request Register 052*2	IR052	8	8	2 ICLK
0008 7035h	ICU	Interrupt Request Register 053*2	IR053	8	8	2 ICLK
0008 7036h	ICU	Interrupt Request Register 054*2	IR054	8	8	2 ICLK
0008 7037h	ICU	Interrupt Request Register 055*2	IR055	8	8	2 ICLK
0008 7038h	ICU	Interrupt Request Register 056*2	IR056	8	8	2 ICLK
0008 7039h	ICU	Interrupt Request Register 057	IR057	8	8	2 ICLK
0008 703Bh	ICU	Interrupt Request Register 059*2	IR059	8	8	2 ICLK
0008 703Ch	ICU	Interrupt Request Register 060*2	IR060	8	8	2 ICLK
0008 703Dh	ICU	Interrupt Request Register 061*2	IR061	8	8	2 ICLK
0008 703Eh	ICU	Interrupt Request Register 062*2	IR062	8	8	2 ICLK
0008 703Fh	ICU	Interrupt Request Register 063*2	IR063	8	8	2 ICLK
0008 7040h	ICU	Interrupt Request Register 064	IR064	8	8	2 ICLK
0008 7041h	ICU	Interrupt Request Register 065	IR065	8	8	2 ICLK
0008 7042h	ICU	Interrupt Request Register 066	IR066	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (9/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 733Fh	ICU	Interrupt Source Priority Register 063*2	IPR063	8	8	2 ICLK
0008 7340h	ICU	Interrupt Source Priority Register 064	IPR064	8	8	2 ICLK
0008 7341h	ICU	Interrupt Source Priority Register 065	IPR065	8	8	2 ICLK
0008 7342h	ICU	Interrupt Source Priority Register 066	IPR066	8	8	2 ICLK
0008 7343h	ICU	Interrupt Source Priority Register 067	IPR067	8	8	2 ICLK
0008 7344h	ICU	Interrupt Source Priority Register 068	IPR068	8	8	2 ICLK
0008 7345h	ICU	Interrupt Source Priority Register 069	IPR069	8	8	2 ICLK
0008 7346h	ICU	Interrupt Source Priority Register 070	IPR070	8	8	2 ICLK
0008 7347h	ICU	Interrupt Source Priority Register 071	IPR071	8	8	2 ICLK
0008 7358h	ICU	Interrupt Source Priority Register 088	IPR088	8	8	2 ICLK
0008 7359h	ICU	Interrupt Source Priority Register 089	IPR089	8	8	2 ICLK
0008 7362h	ICU	Interrupt Source Priority Register 098*2	IPR098	8	8	2 ICLK
0008 7363h	ICU	Interrupt Source Priority Register 099*2	IPR099	8	8	2 ICLK
0008 7364h	ICU	Interrupt Source Priority Register 100*2	IPR100	8	8	2 ICLK
0008 7365h	ICU	Interrupt Source Priority Register 101*2	IPR101	8	8	2 ICLK
0008 7366h	ICU	Interrupt Source Priority Register 102	IPR102	8	8	2 ICLK
0008 7367h	ICU	Interrupt Source Priority Register 103	IPR103	8	8	2 ICLK
0008 7368h	ICU	Interrupt Source Priority Register 104	IPR104	8	8	2 ICLK
0008 7369h	ICU	Interrupt Source Priority Register 105	IPR105	8	8	2 ICLK
0008 736Ah	ICU	Interrupt Source Priority Register 106	IPR106	8	8	2 ICLK
0008 736Bh	ICU	Interrupt Source Priority Register 107	IPR107	8	8	2 ICLK
0008 736Ch	ICU	Interrupt Source Priority Register 108	IPR108	8	8	2 ICLK
0008 736Dh	ICU	Interrupt Source Priority Register 109	IPR109	8	8	2 ICLK
0008 736Eh	ICU	Interrupt Source Priority Register 110	IPR110	8	8	2 ICLK
0008 736Fh	ICU	Interrupt Source Priority Register 111	IPR111	8	8	2 ICLK
0008 7370h	ICU	Interrupt Source Priority Register 112	IPR112	8	8	2 ICLK
0008 7371h	ICU	Interrupt Source Priority Register 113	IPR113	8	8	2 ICLK
0008 7372h	ICU	Interrupt Source Priority Register 114	IPR114	8	8	2 ICLK
0008 7376h	ICU	Interrupt Source Priority Register 118	IPR118	8	8	2 ICLK
0008 7379h	ICU	Interrupt Source Priority Register 121	IPR121	8	8	2 ICLK
0008 737Bh	ICU	Interrupt Source Priority Register 123	IPR123	8	8	2 ICLK
0008 737Dh	ICU	Interrupt Source Priority Register 125	IPR125	8	8	2 ICLK
0008 737Fh	ICU	Interrupt Source Priority Register 127	IPR127	8	8	2 ICLK
0008 7381h	ICU	Interrupt Source Priority Register 129	IPR129	8	8	2 ICLK
0008 7385h	ICU	Interrupt Source Priority Register 133	IPR133	8	8	2 ICLK
0008 7386h	ICU	Interrupt Source Priority Register 134	IPR134	8	8	2 ICLK
0008 738Ah	ICU	Interrupt Source Priority Register 138	IPR138	8	8	2 ICLK
0008 738Bh	ICU	Interrupt Source Priority Register 139	IPR139	8	8	2 ICLK
0008 738Eh	ICU	Interrupt Source Priority Register 142	IPR142	8	8	2 ICLK
0008 7392h	ICU	Interrupt Source Priority Register 146	IPR146	8	8	2 ICLK
0008 7395h	ICU	Interrupt Source Priority Register 149	IPR149	8	8	2 ICLK
0008 7397h	ICU	Interrupt Source Priority Register 151	IPR151	8	8	2 ICLK
0008 7399h	ICU	Interrupt Source Priority Register 153	IPR153	8	8	2 ICLK
0008 739Fh	ICU	Interrupt Source Priority Register 159	IPR159	8	8	2 ICLK
0008 73A3h	ICU	Interrupt Source Priority Register 163	IPR163	8	8	2 ICLK
0008 73A8h	ICU	Interrupt Source Priority Register 168	IPR168	8	8	2 ICLK
0008 73ADh	ICU	Interrupt Source Priority Register 173	IPR173	8	8	2 ICLK
0008 73AEh	ICU	Interrupt Source Priority Register 174	IPR174	8	8	2 ICLK
0008 73B1h	ICU	Interrupt Source Priority Register 177	IPR177	8	8	2 ICLK
0008 73B4h	ICU	Interrupt Source Priority Register 180	IPR180	8	8	2 ICLK
0008 73B7h	ICU	Interrupt Source Priority Register 183	IPR183	8	8	2 ICLK
0008 73BAh	ICU	Interrupt Source Priority Register 186	IPR186	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (27/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000A 85B2h	RSCAN	RAM Test Register 25*2	RPGACC25	16	16	2 or 3 PCLKB
000A 85B4h	RSCAN	Receive FIFO Access Register 1BL*2	RFTS1	16	16	2 or 3 PCLKB
000A 85B4h	RSCAN	RAM Test Register 26*2	RPGACC26	16	16	2 or 3 PCLKB
000A 85B6h	RSCAN	Receive FIFO Access Register 1BH*2	RFPTR1	16	16	2 or 3 PCLKB
000A 85B6h	RSCAN	RAM Test Register 27*2	RPGACC27	16	16	2 or 3 PCLKB
000A 85B8h	RSCAN	Receive FIFO Access Register 1CL*2	RFDF01	16	16	2 or 3 PCLKB
000A 85B8h	RSCAN	RAM Test Register 28*2	RPGACC28	16	16	2 or 3 PCLKB
000A 85BAh	RSCAN	Receive FIFO Access Register 1CH*2	RFDF11	16	16	2 or 3 PCLKB
000A 85BAh	RSCAN	RAM Test Register 29*2	RPGACC29	16	16	2 or 3 PCLKB
000A 85BCh	RSCAN	Receive FIFO Access Register 1DL*2	RFDF21	16	16	2 or 3 PCLKB
000A 85BCh	RSCAN	RAM Test Register 30*2	RPGACC30	16	16	2 or 3 PCLKB
000A 85BEh	RSCAN	Receive FIFO Access Register 1DH*2	RFDF31	16	16	2 or 3 PCLKB
000A 85BEh	RSCAN	RAM Test Register 31*2	RPGACC31	16	16	2 or 3 PCLKB
000A 85C0h to 000A 85DEh	RSCAN	RAM Test Register 32 to 47*2	RPGACC32 to 47	16	16	2 or 3 PCLKB
000A 85E0h	RSCAN0	Transmit/Receive FIFO Access Register 0AL*2	CFIDL0	16	16	2 or 3 PCLKB
000A 85E0h	RSCAN	RAM Test Register 48*2	RPGACC48	16	16	2 or 3 PCLKB
000A 85E2h	RSCAN0	Transmit/Receive FIFO Access Register 0AH*2	CFIDH0	16	16	2 or 3 PCLKB
000A 85E2h	RSCAN	RAM Test Register 49*2	RPGACC49	16	16	2 or 3 PCLKB
000A 85E4h	RSCAN0	Transmit/Receive FIFO Access Register 0BL*2	CFTS0	16	16	2 or 3 PCLKB
000A 85E4h	RSCAN	RAM Test Register 50*2	RPGACC50	16	16	2 or 3 PCLKB
000A 85E6h	RSCAN0	Transmit/Receive FIFO Access Register 0BH*2	CFPTR0	16	16	2 or 3 PCLKB
000A 85E6h	RSCAN	RAM Test Register 51*2	RPGACC51	16	16	2 or 3 PCLKB
000A 85E8h	RSCAN0	Transmit/Receive FIFO Access Register 0CL*2	CFDF00	16	16	2 or 3 PCLKB
000A 85E8h	RSCAN	RAM Test Register 52*2	RPGACC52	16	16	2 or 3 PCLKB
000A 85EAh	RSCAN0	Transmit/Receive FIFO Access Register 0CH*2	CFDF10	16	16	2 or 3 PCLKB
000A 85EAh	RSCAN	RAM Test Register 53*2	RPGACC53	16	16	2 or 3 PCLKB
000A 85ECh	RSCAN0	Transmit/Receive FIFO Access Register 0DL*2	CFDF20	16	16	2 or 3 PCLKB
000A 85ECh	RSCAN	RAM Test Register 54*2	RPGACC54	16	16	2 or 3 PCLKB
000A 85EEh	RSCAN0	Transmit/Receive FIFO Access Register 0DH*2	CFDF30	16	16	2 or 3 PCLKB
000A 85EEh	RSCAN	RAM Test Register 55*2	RPGACC55	16	16	2 or 3 PCLKB
000A 85F0h to 000A 85FEh	RSCAN	RAM Test Register 56 to 63*2	RPGACC56 to 63	16	16	2 or 3 PCLKB
000A 8600h	RSCAN0	Transmit Buffer Register 0AL*2	TMIDL0	16	16	2 or 3 PCLKB
000A 8600h	RSCAN	RAM Test Register 64*2	RPGACC64	16	16	2 or 3 PCLKB
000A 8602h	RSCAN0	Transmit Buffer Register 0AH*2	TMIDH0	16	16	2 or 3 PCLKB
000A 8602h	RSCAN	RAM Test Register 65*2	RPGACC65	16	16	2 or 3 PCLKB
000A 8604h	RSCAN	RAM Test Register 66*2	RPGACC66	16	16	2 or 3 PCLKB
000A 8606h	RSCAN0	Transmit Buffer Register 0BH*2	TMPTR0	16	16	2 or 3 PCLKB
000A 8606h	RSCAN	RAM Test Register 67*2	RPGACC67	16	16	2 or 3 PCLKB
000A 8608h	RSCAN0	Transmit Buffer Register 0CL*2	TMDF00	16	16	2 or 3 PCLKB
000A 8608h	RSCAN	RAM Test Register 68*2	RPGACC68	16	16	2 or 3 PCLKB
000A 860Ah	RSCAN0	Transmit Buffer Register 0CH*2	TMDF10	16	16	2 or 3 PCLKB
000A 860Ah	RSCAN	RAM Test Register 69*2	RPGACC69	16	16	2 or 3 PCLKB
000A 860Ch	RSCAN0	Transmit Buffer Register 0DL*2	TMDF20	16	16	2 or 3 PCLKB
000A 860Ch	RSCAN	RAM Test Register 70*2	RPGACC70	16	16	2 or 3 PCLKB
000A 860Eh	RSCAN0	Transmit Buffer Register 0DH*2	TMDF30	16	16	2 or 3 PCLKB
000A 860Eh	RSCAN	RAM Test Register 71*2	RPGACC71	16	16	2 or 3 PCLKB
000A 8610h	RSCAN0	Transmit Buffer Register 1AL*2	TMIDL1	16	16	2 or 3 PCLKB
000A 8610h	RSCAN	RAM Test Register 72*2	RPGACC72	16	16	2 or 3 PCLKB
000A 8612h	RSCAN0	Transmit Buffer Register 1AH*2	TMIDH1	16	16	2 or 3 PCLKB
000A 8612h	RSCAN	RAM Test Register 73*2	RPGACC73	16	16	2 or 3 PCLKB

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = AVSS1 = AVSS2 = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC	–0.3 to +6.5	V
Input voltage	Port 4, port 5, port 6	V_{in}	–0.3 to VREF + 0.3	V
	Except for port 4, port 5, port 6 and ports for 5 V tolerant*1		–0.3 to VCC + 0.3	V
	Ports for 5 V tolerant*1		–0.3 to +6.5	V
Analog power supply voltage		AVCC0, AVCC1, AVCC2, VREF	–0.3 to +6.5	V
Analog input voltage	When AN000 to AN003, AN100 to AN103, AN200 to AN211 used	V_{AN}	–0.3 to VREF + 0.3	V
	When AN016, AN116, CVREFC0, CVREFC1 used		–0.3 to VCC + 0.3	
Operating temperature		T_{opr}	–40 to +85	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the AVCC1 and AVSS1 pins, between the AVCC2 and AVSS2 pins, between the VREF and AVSS2 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.
Connect the VCL pin to a VSS pin via a 4.7 µF capacitor. The capacitor must be placed close to the pin.
Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered.
The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.
Even if –0.3 to +6.5 V is input to 5-V tolerant ports, it will not cause problems such as damage to the MCU.
Note 1. Ports B1 and B2 are 5 V tolerant.

Table 5.2 Recommended Operating Voltage Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltages	VCC*1, *2		2.7	—	5.5	V
	VSS		—	0	—	
Analog power supply voltages	AVCC0, AVCC1, AVCC2, VREF*1, *2		VCC	—	5.5	V
	AVSS0, AVSS1, AVSS2		—	0	—	

Note 1. AVCC0/AVCC1/AVCC2/VREF and VCC can be set individually within the operating range.
Note 2. When powering on the VCC and AVCC0/AVCC1/AVCC2/VREF pins, power them on at the same time or the VCC pin first and then the AVCC0/AVCC1/AVCC2/VREF pin.

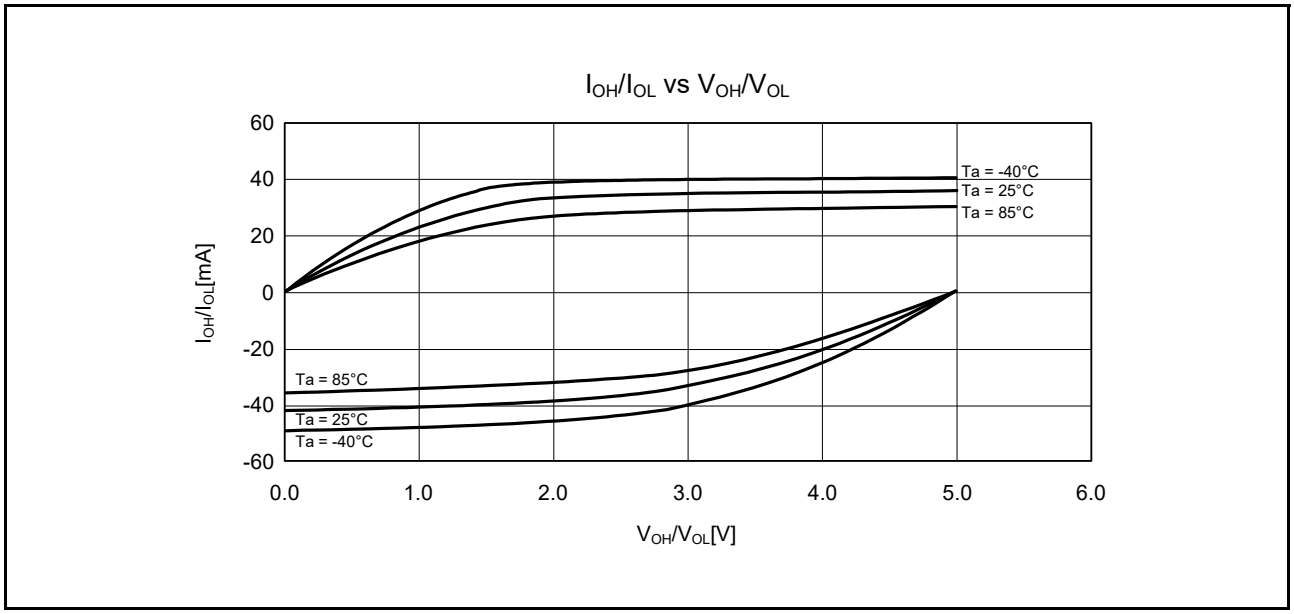


Figure 5.8 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.0 V when Normal Output is Selected (Reference Data)**

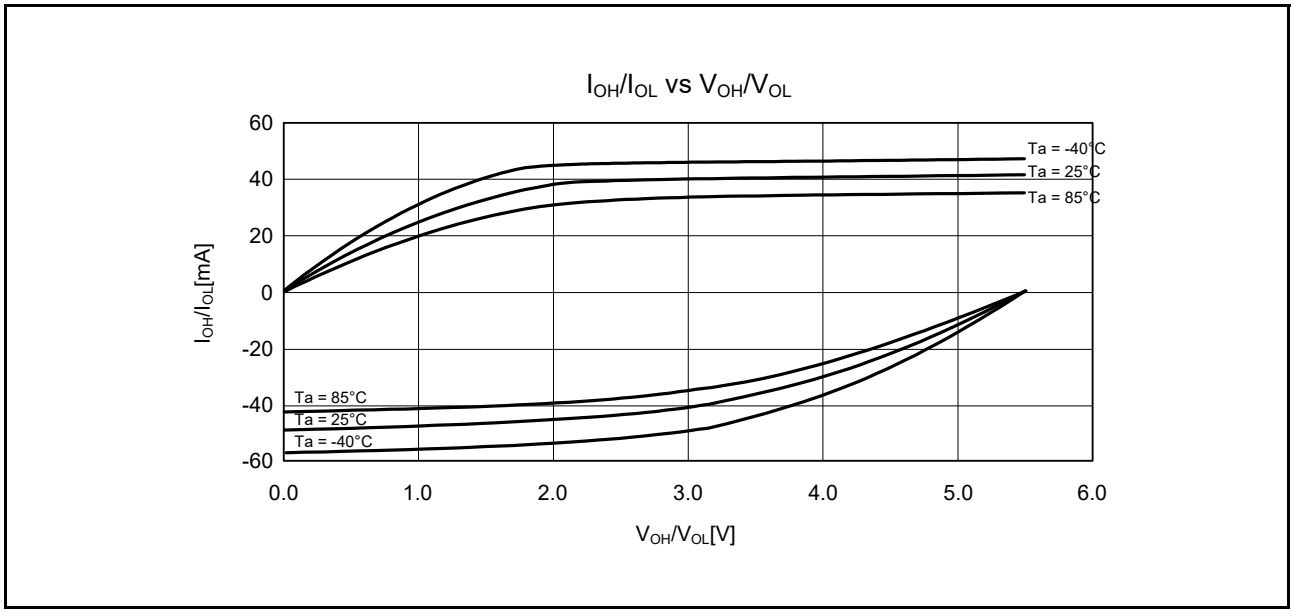


Figure 5.9 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.5 V when Normal Output is Selected (Reference Data)**

5.2.2 Standard I/O Pin Output Characteristics (2)

Figure 5.10 to Figure 5.13 show the characteristics when high-drive output is selected by the drive capacity control register.

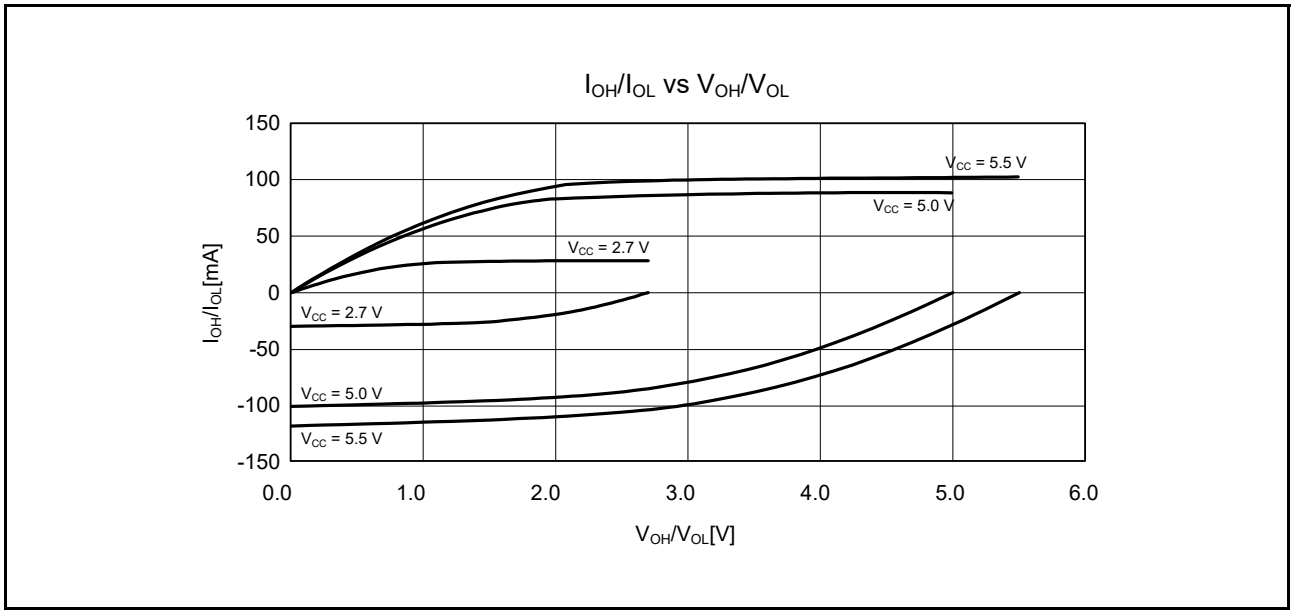


Figure 5.10 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at T_a = 25°C When Normal Output is Selected (Reference Data)

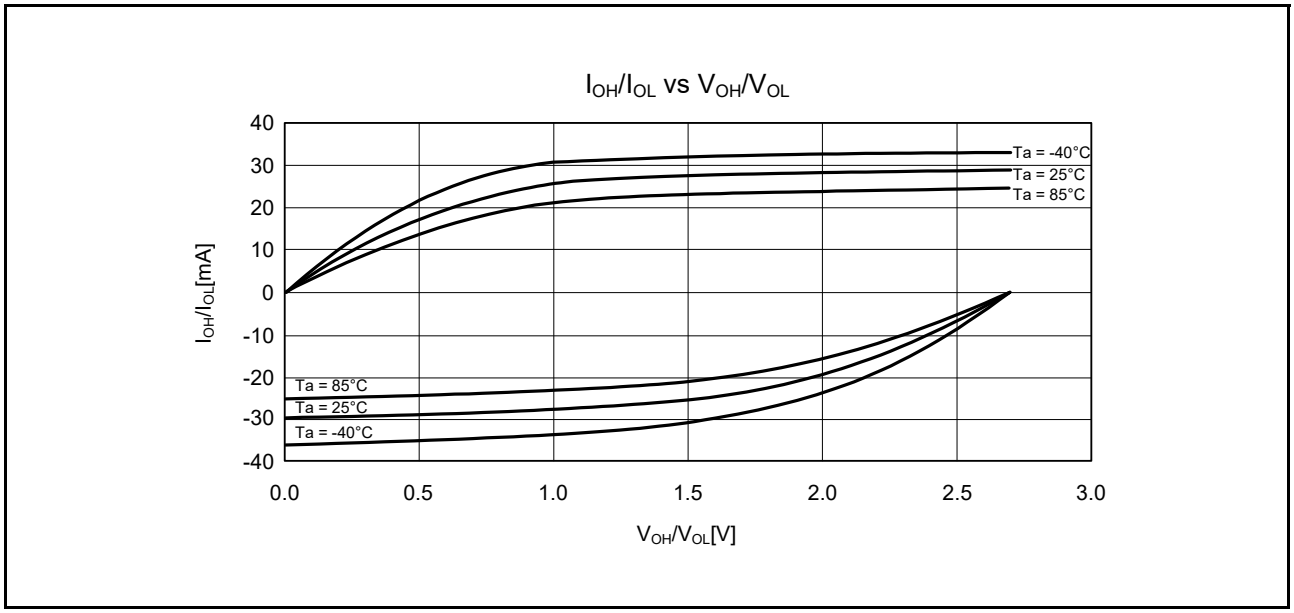


Figure 5.11 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V when Normal Output is Selected (Reference Data)

5.2.4 RIIC Pin Output Characteristics

Figure 5.18 to Figure 5.21 show the output characteristics of the RIIC pin.

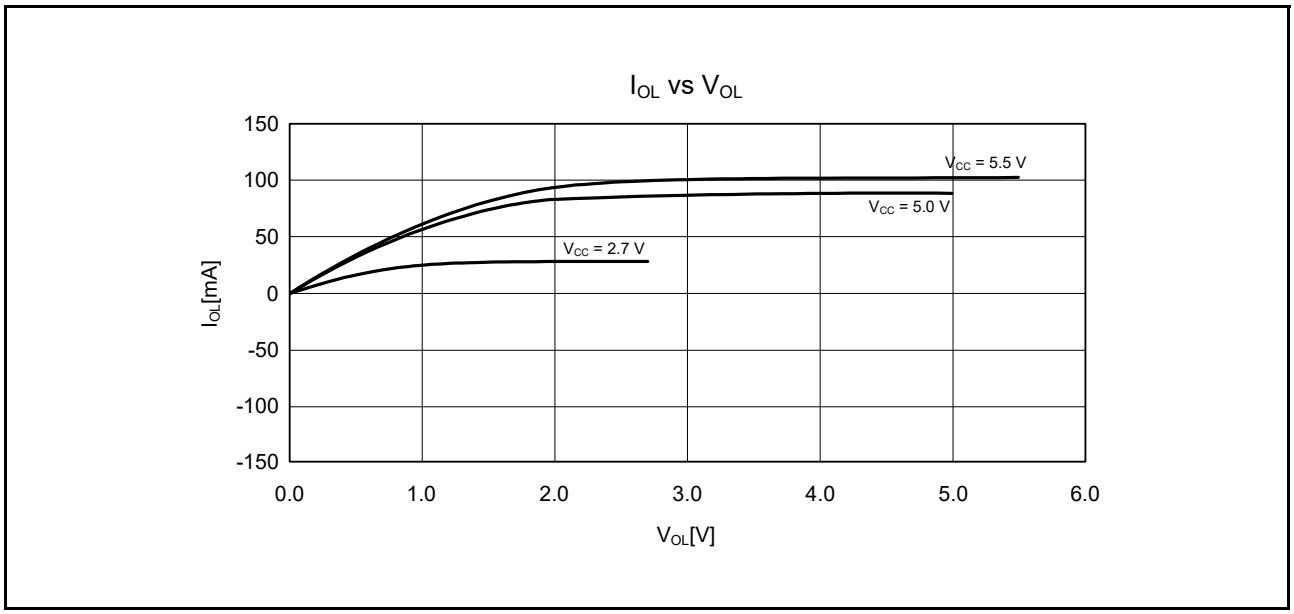


Figure 5.18 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at T_a = 25°C (Reference Data)

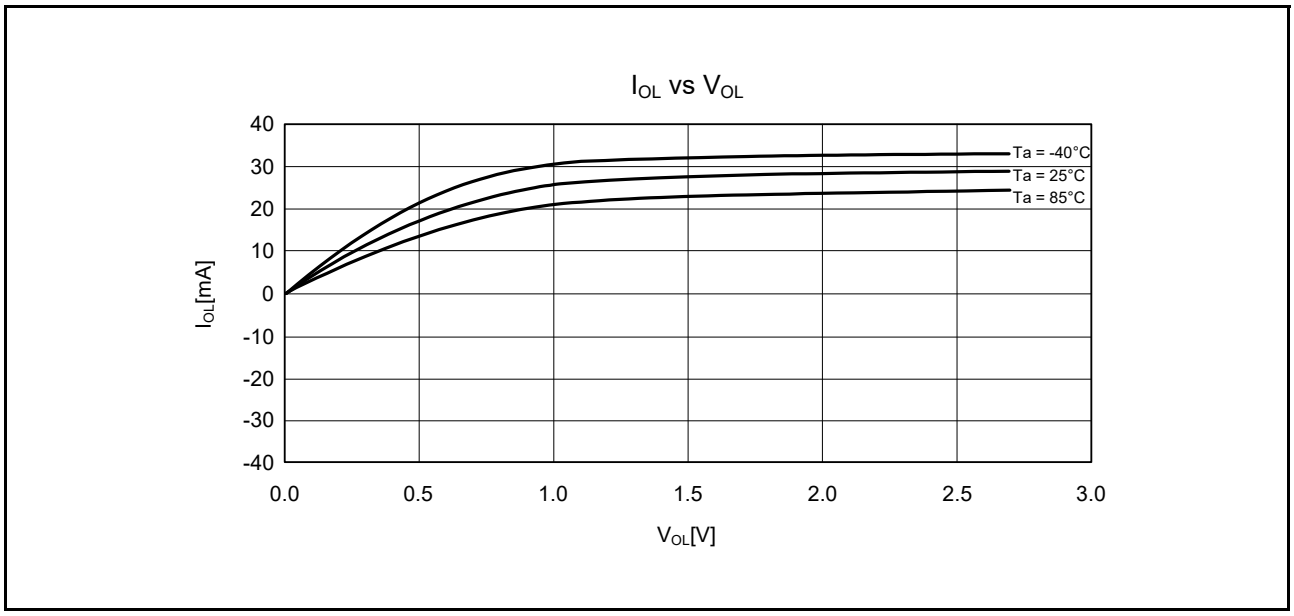


Figure 5.19 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)

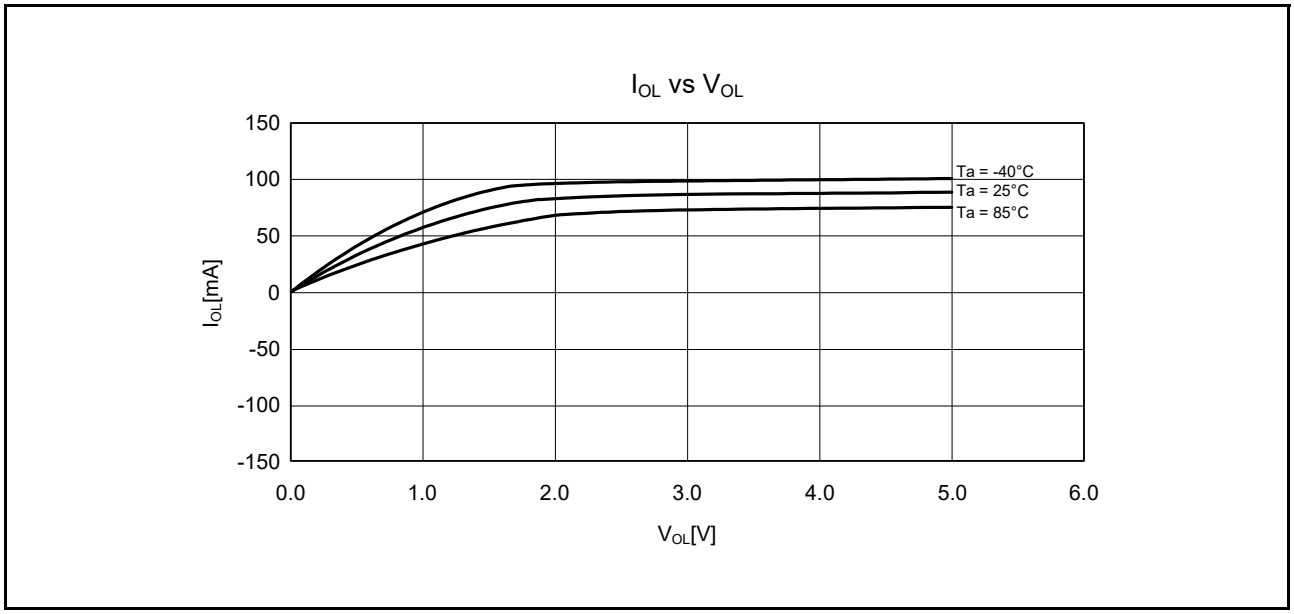


Figure 5.20 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 5.0 V (Reference Data)

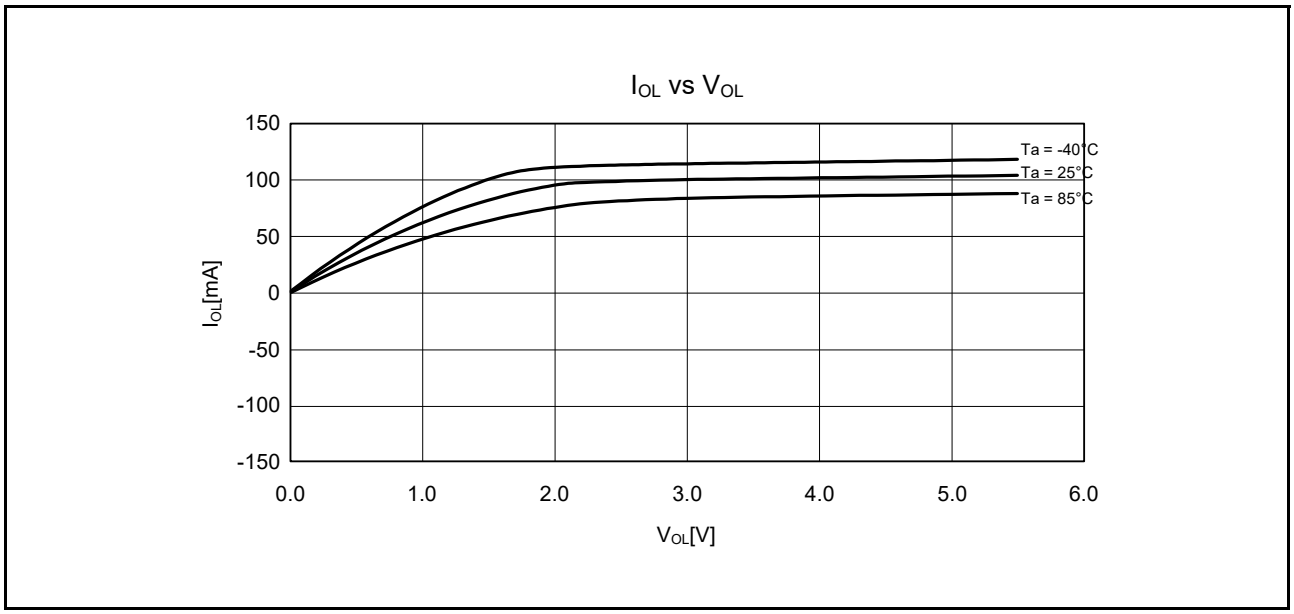


Figure 5.21 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 5.5 V (Reference Data)

Table 5.16 Clock Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{Xcyc}	50	—	—	ns	Figure 5.22
EXTAL external clock input high pulse width	t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width	t_{XL}	20	—	—	ns	
EXTAL external clock rise time	t_{Xr}	—	—	5	ns	
EXTAL external clock fall time	t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1	t_{XWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency	f_{MAIN}	1	—	20	MHz	
Main clock oscillation stabilization time (crystal)*2	$t_{MAINOSC}$	—	3	—	ms	Figure 5.23
Main clock oscillation stabilization time (ceramic resonator)*2	$t_{MAINOSC}$	—	50	—	μs	
LOCO clock oscillation frequency	f_{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	0.5	μs	Figure 5.24
HOCO clock oscillation frequency	f_{HOCO} (32MHz)	31.52	32	32.48	MHz	T_a = –40 to –20°C
		31.68	32	32.32	MHz	T_a = –20 to +75°C
		31.52	32	32.48	MHz	T_a = +75 to +85°C
	f_{HOCO} (64MHz)	63.04	64	64.96	MHz	T_a = –40 to –20°C
		63.36	64	64.64	MHz	T_a = –20 to +75°C
		63.04	64	64.96	MHz	T_a = +75 to +85°C
HOCO clock oscillation stabilization time	t_{HOCO} (32MHz)	—	—	37.1	μs	Figure 5.26
	t_{HOCO} (64MHz)	—	—	80.6	μs	Figure 5.26
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time	t_{ILOCO}	—	—	50	μs	Figure 5.27
PLL circuit oscillation frequency	f_{PLL}	40	—	80	MHz	
PLL clock oscillation stabilization time	t_{PLL}	—	—	50	μs	Figure 5.28
PLL free-running oscillation frequency	f_{PLLFR}	—	8	—	MHz	

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.

Note 2. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that is has become 1, and then start using the main clock.

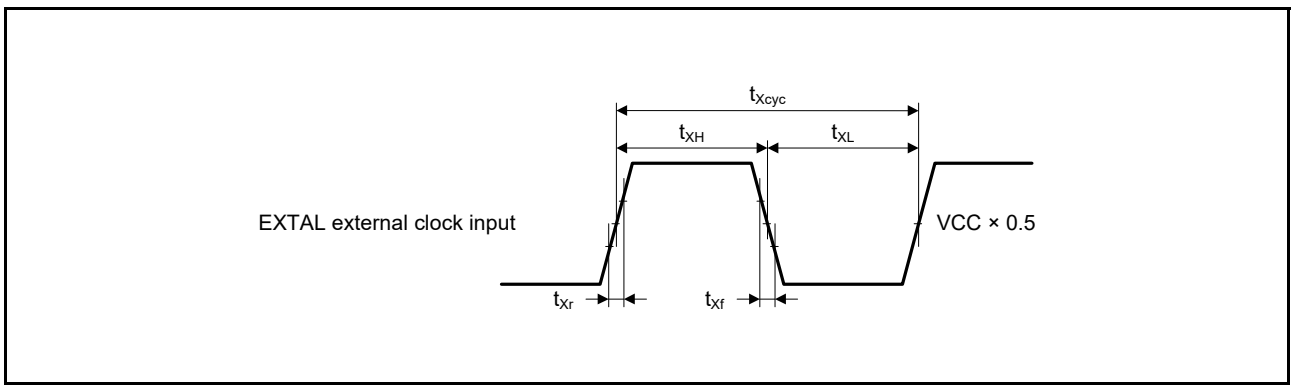


Figure 5.22 EXTAL External Clock Input Timing

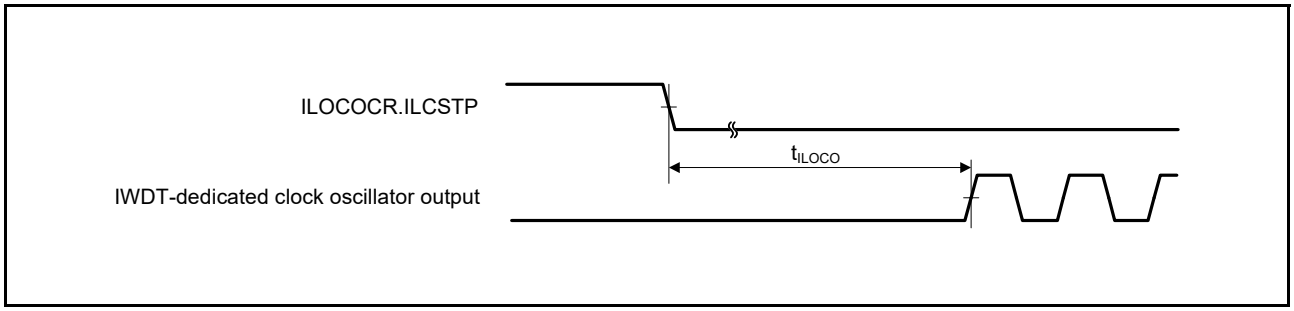


Figure 5.27 IWDT-Dedicated Clock Oscillation Start Timing

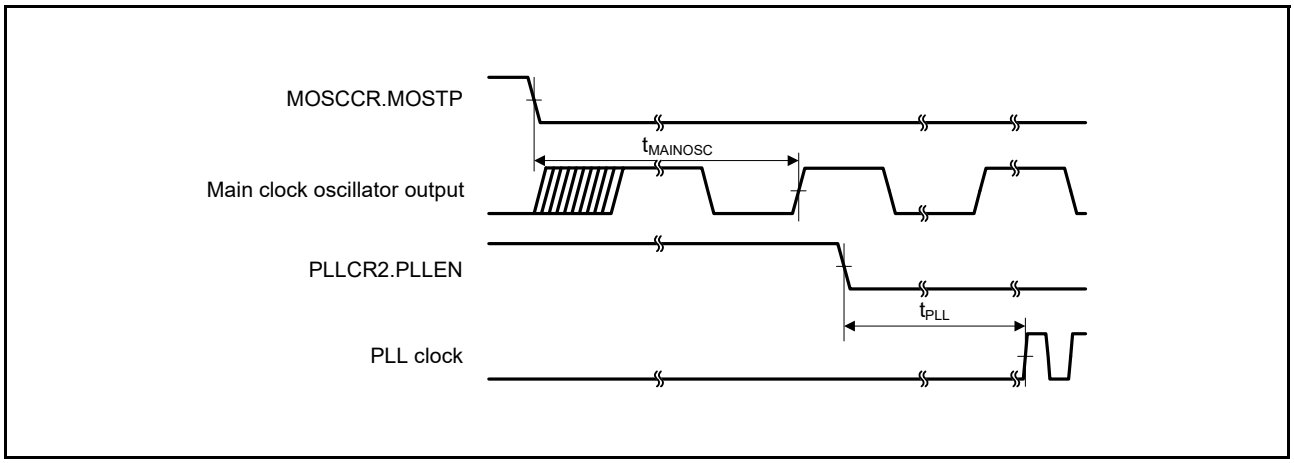


Figure 5.28 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

Table 5.25 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C, C = 30pF

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.47
	SCK clock cycle input (slave)			6	—	t_{Pcyc}	
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (master)	VCC = 4.0 V or above	t_{SU}	40	—	ns	Figure 5.48, Figure 5.49
		VCC = 2.7 V or above		65	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SS input setup time		t_{LEAD}	3	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	3	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	VCC = 4.0 V or above		—	40		
		VCC = 2.7 V or above		—	65		
	Data output hold time	Master	t_{OH}	–10	—	ns	
		Slave		–10	—		
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SS input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{Pcyc}	Figure 5.50, Figure 5.51
	Slave output release time		t_{REL}	—	6	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

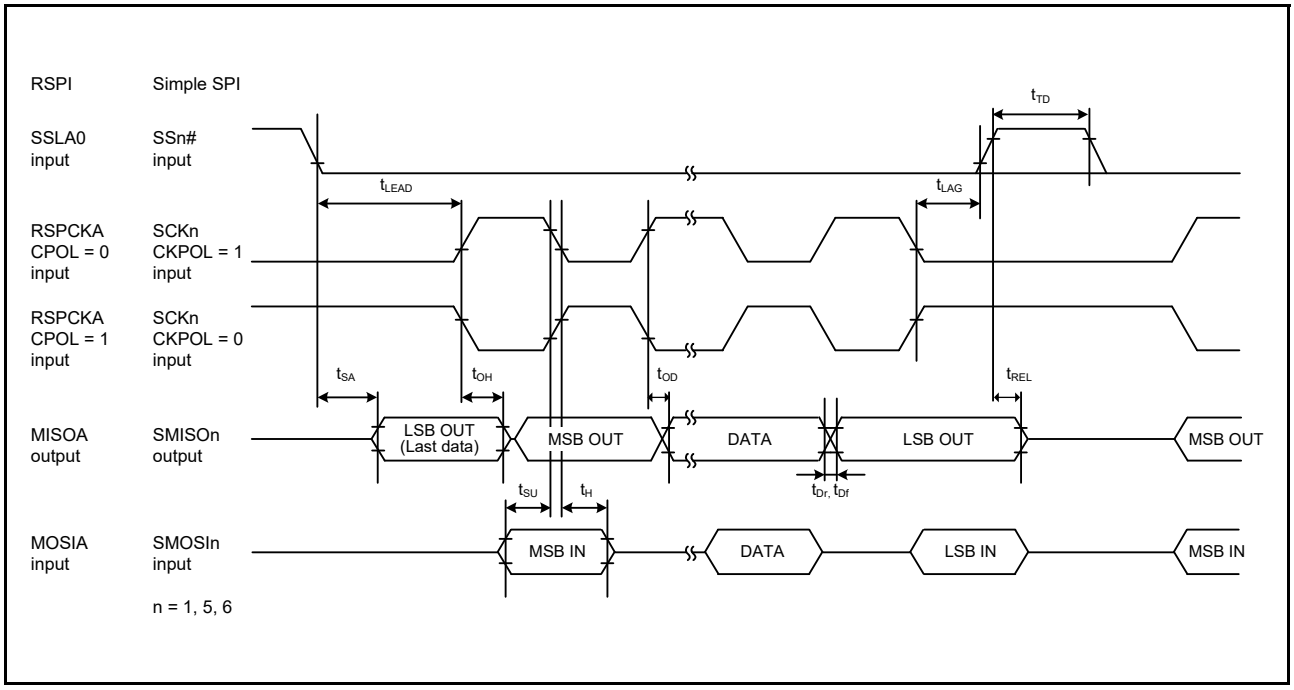
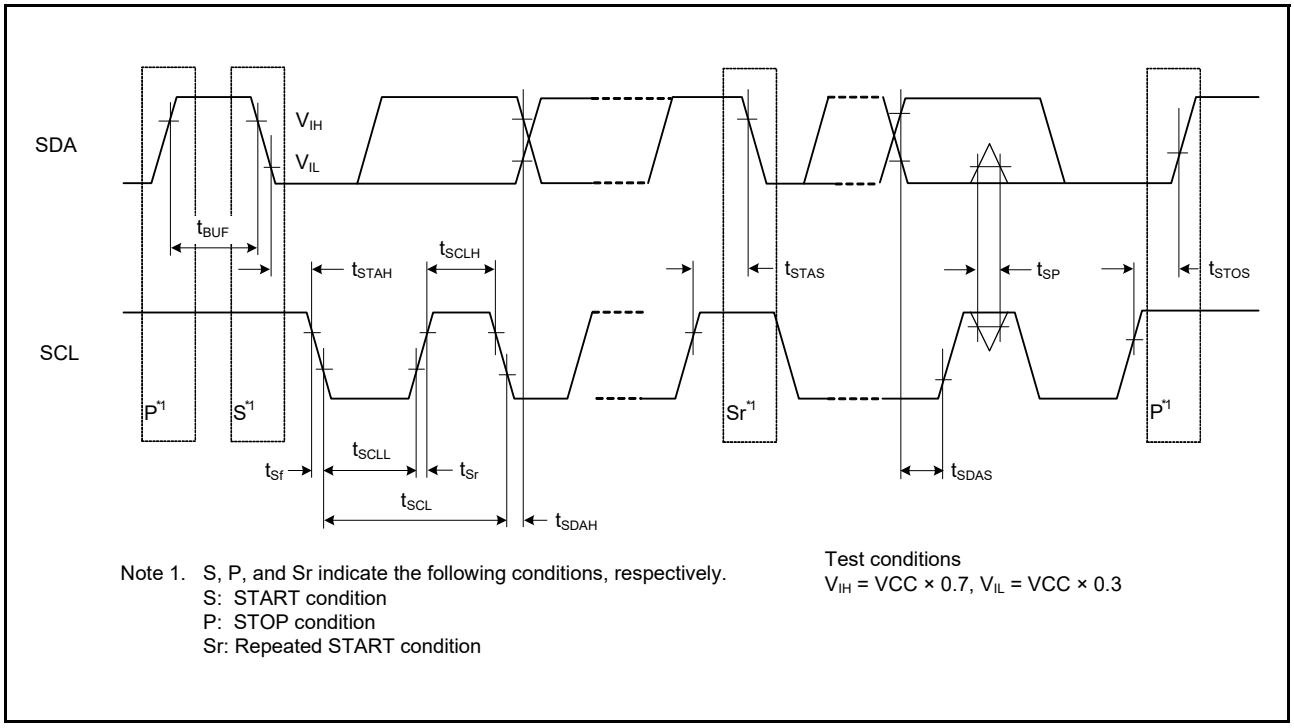


Figure 5.51 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0)



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: Repeated START condition

Test conditions
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3

Figure 5.52 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

Table 5.41 ROM (Flash Memory for Code Storage) Characteristics (3): Middle-Speed Operating Mode

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8-byte	t_{P8}	—	152.0	1367.0	—	97.9	936.0	µs
Erasure time	2-Kbyte	t_{E2K}	—	8.8	279.7	—	5.9	220.8	ms
	256-Kbyte (when block erase command used)	t_{E256K}	—	469.2	9816.9	—	100.5	2260.1	ms
	256-Kbyte (when all-block erase command used)	t_{EA256K}	—	464.0	9610.7	—	95.3	2053.7	ms
	512-Kbyte (when block erase command used)	t_{E512K}	—	928.0	19221.2	—	190.6	4107.3	ms
	512-Kbyte (when all-block erase command used)	t_{EA512K}	—	922.7	19015.0	—	185.4	3901.0	ms
Blank check time	8-byte	t_{BC8}	—	—	85.0	—	—	50.9	µs
	2-Kbyte	t_{BC2K}	—	—	1870.0	—	—	401.5	µs
Erase operation forcible stop time		t_{SED}	—	—	28.0	—	—	21.3	µs
Start-up area switching setting time		t_{SAS}	—	13.0	573.3	—	7.7	450.1	ms
Access window time		t_{AWS}	—	13.0	573.3	—	7.7	450.1	ms
ROM mode transition wait time 1		t_{DIS}	2.0	—	—	2.0	—	—	µs
ROM mode transition wait time 2		t_{MS}	3.0	—	—	3.0	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK should be ±3.5%.

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.