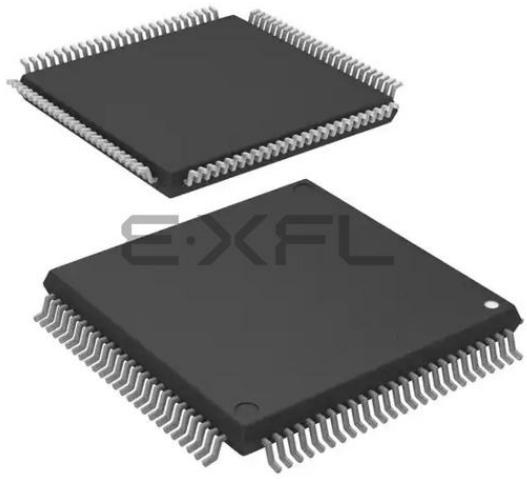
Renesas Electronics America Inc - R5F524T8ADFP#30 Datasheet



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Applications of "Embedded - Microcontrollers"

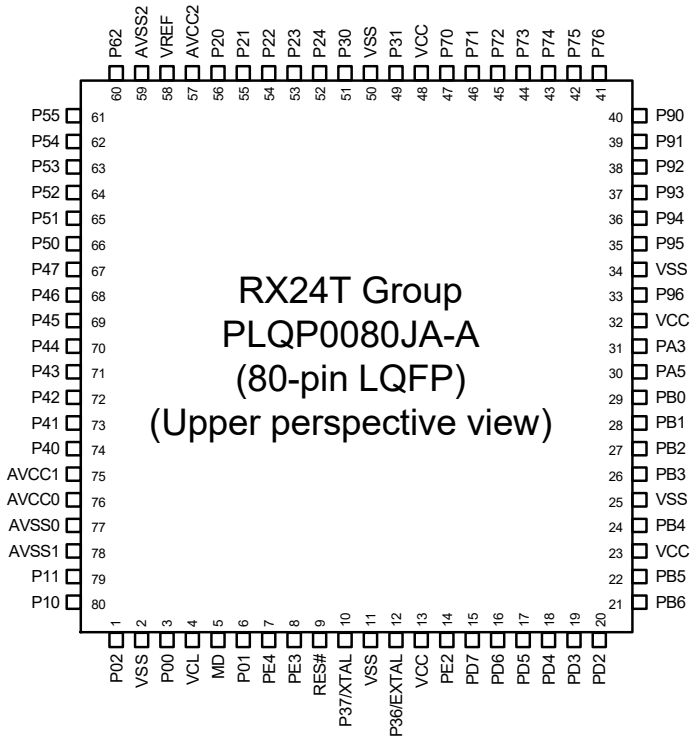
Details	
Product Status	Discontinued at Digi-Key
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 22x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f524t8adfp-30

Table 1.4 Pin Functions (2/4)

Classifications	Pin Name	I/O	Description
Multi-function timer pulse unit 3 (MTU3d)	MTIOC9A#, MTIOC9B#, MTIOC9C#, MTIOC9D#	I/O	The TGRA9 to TGRD9 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
	MTCLKA#, MTCLKB#, MTCLKC#, MTCLKD#	Input	Inverted input pins for the external clock.
	ADSM0, ADSM1	Output	A/D trigger output pins.
General PWM timer (GPTB)	GTIOC0A, GTIOC0B	I/O	The GPT0.GTGRA and GPT0.GTGRB input capture input/output compare output/PWM output pins
	GTIOC0A#, GTIOC0B#	I/O	The GPT0.GTGRA and GPT0.GTGRB input capture inverted input/output compare inverted output/PWM inverted output pins
	GTIOC1A, GTIOC1B	I/O	The GPT1.GTGRA and GPT1.GTGRB input capture input/output compare output/PWM output pins
	GTIOC1A#, GTIOC1B#	I/O	The GPT1.GTGRA and GPT1.GTGRB input capture inverted input/output compare inverted output/PWM inverted output pins
	GTIOC2A, GTIOC2B	I/O	The GPT2.GTGRA and GPT2.GTGRB input capture input/output compare output/PWM output pins
	GTIOC2A#, GTIOC2B#	I/O	The GPT2.GTGRA and GPT2.GTGRB input capture inverted input/output compare inverted output/PWM inverted output pins
	GTIOC3A, GTIOC3B	I/O	The GPT3.GTGRA and GPT3.GTGRB input capture input/output compare output/PWM output pins
	GTIOC3A#, GTIOC3B#	I/O	The GPT3.GTGRA and GPT3.GTGRB input capture inverted input/output compare inverted output/PWM inverted output pins
	GTETRG	Input	External trigger input pin for GPT0 to GPT3
	GTECLKA, GTECLKB, GTECLKC, GTECLKD	Input	Input pins A to D for the external clock
	GTADSM0, GTADSM1	Output	A/D conversion start request monitoring output pins
8-bit timer (TMR)	TMO0 to TMO7	Output	Compare match output pins.
	TMCI0 to TMCI7	Input	Input pins for the external clock to be input to the counter.
	TMRI0 to TMRI7	Input	Counter reset input pins.
Port output enable 3 (POE3b, POE3A)	POE0#, POE4#, POE8#, POE10#, POE11#, POE12#	Input	Input pins for request signals to switch the MTU and GPT pins between the high impedance state or operation as general I/O port pins
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK1, SCK5, SCK6	I/O	Input/output pins for the clock.
	RXD1, RXD5, RXD6	Input	Input pins for received data.
	TXD1, TXD5, TXD6	Output	Output pins for transmitted data.
	CTS1#, CTS5#, CTS6#	Input	Input pins for controlling the start of transmission and reception.
	RTS1#, RTS5#, RTS6#	Output	Output pins for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL1, SSCL5, SSCL6	I/O	Input/output pins for the I^2C clock.
	SSDA1, SSDA5, SSDA6	I/O	Input/output pins for the I^2C data.
	• Simple SPI mode		
	SCK1, SCK5, SCK6	I/O	Input/output pins for the clock.
	SMISO1, SMISO5, SMISO6	I/O	Input/output pins for slave transmit data.
	SMOSI1, SMOSI5, SMOSI6	I/O	Input/output pins for master transmit data.
	SS1#, SS5#, SS6#	Input	Chip-select input pins.

Table 1.4 Pin Functions (3/4)

Classifications	Pin Name	I/O	Description
I²C bus interface (RIICa)	SCL0	I/O	Input/output pin for I²C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA0	I/O	Input/output pin for I²C bus interface data. Bus can be directly driven by the N-channel open drain output.
Serial peripheral interface (RSPIb)	RSPCKA	I/O	Input/output pin for the RSPI clock.
	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master.
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave.
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI.
CAN module (RSCAN)	CRXD0	Input	Input pin
	CTXD0	Output	Output pin
12-bit A/D converter (S12ADF)	AN000 to AN003, AN016, AN100 to AN103, AN116, AN200 to AN211	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADST0, ADST1, ADST2	Output	Output pins for A/D conversion status.
	ADTRG0#, ADTRG1#, ADTRG2#	Input	Input pins for the external trigger signals that start the A/D conversion.
8-bit D/A converter (DAa)	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter
Comparator C (CMPC)	COMP0 to COMP3	Output	Comparator detection result output pins.
	CVREFC0, CVREFC1	Input	Analog reference voltage supply pins for comparator C.
	CMPC00 to CMPC03	Input	Analog input pin for CMPC0
	CMPC10 to CMPC13	Input	Analog input pin for CMPC1
	CMPC20 to CMPC23	Input	Analog input pin for CMPC2
	CMPC30 to CMPC33	Input	Analog input pin for CMPC3
Analog power supply	AVCC0	—	Analog power supply and reference power supply pin for 12-bit A/D converter unit 0. Connect the AVCC0 pin to AVCC1, AVCC2, or VREF when 12-bit A/D converter unit 0 is not used.
	AVSS0	—	Analog ground and reference ground pin for 12-bit A/D converter unit 0. Connect the AVSS0 pin to AVSS1 or AVSS2 when 12-bit A/D converter unit 0 is not used.
	AVCC1	—	Analog power supply and reference power supply pin for 12-bit A/D converter unit 1. Connect the AVCC1 pin to AVCC0, AVCC2, or VREF when 12-bit A/D converter unit 1 is not used.
	AVSS1	—	Analog ground and reference ground pin for 12-bit A/D converter unit 1. Connect the AVSS1 pin to AVSS0 or AVSS2 when 12-bit A/D converter unit 1 is not used.
	AVCC2	—	Analog power supply and reference power supply pin for 12-bit A/D converter unit 2. Connect the AVCC2 pin to AVCC0, AVCC1, or VREF when 12-bit A/D converter unit 2 is not used.
	AVSS2	—	Analog ground and reference ground pin for 12-bit A/D converter unit 2. Analog ground pin for comparator C and 8-bit D/A converter. Connect the AVSS2 pin to AVSS0 or AVSS1 when 12-bit A/D converter unit 2, comparator C and 8-bit D/A converter are not used.
	VREF	—	Analog power supply pin for comparator C and 8-bit D/A converter. For the 64-pin LFQFP package, the VREF pin is internally connected to AVCC2 and is shared. Connect the VREF pin to AVCC0, AVCC1, or AVCC2 when comparator C and 8-bit D/A converter are not used.



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, refer to List of Pins and Pin Functions (80-Pin LQFP/LFQFP).

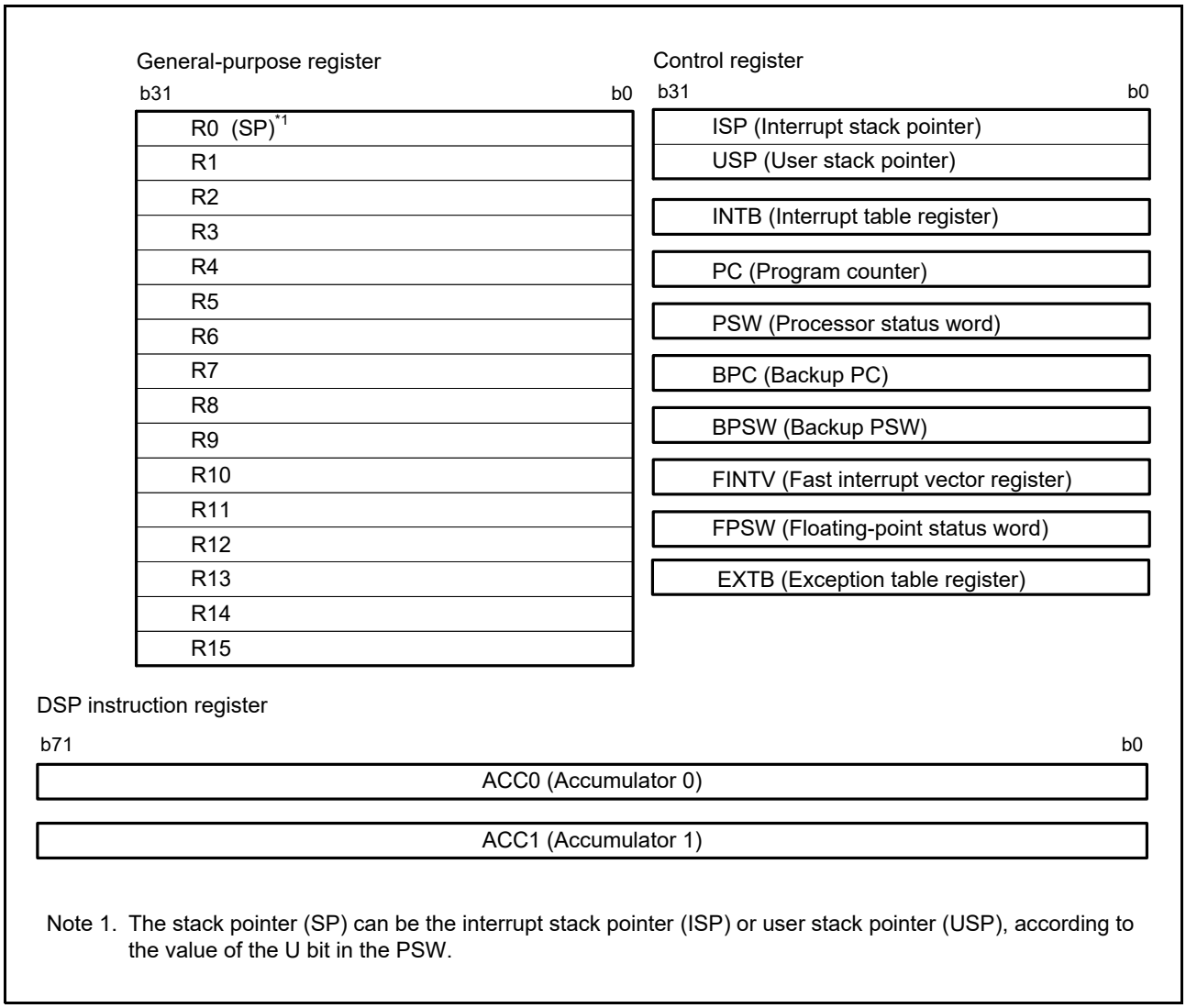
Figure 1.4 Pin Assignments of the 80-Pin LQFP

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version B) (2/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
52		P75	MTIOC4C, MTIOC4C#, GTIOC1B, GTIOC1B#		
53		P74	MTIOC3D, MTIOC3D#, GTIOC0B, GTIOC0B#		
54		P73	MTIOC4B, MTIOC4B#, GTIOC2A, GTIOC2A#		
55		P72	MTIOC4A, MTIOC4A#, GTIOC1A, GTIOC1A#		
56		P71	MTIOC3B, MTIOC3B#, GTIOC0A, GTIOC0A#		
57		P70	POE0#		IRQ5
58		P33	MTIOC3A, MTIOC3A#, MTCLKA, MTCLKA#, TMO0	SSLA3	
59		P32	MTIOC3C, MTIOC3C#, MTCLKB, MTCLKB#, TMO6	SSLA2	
60	VCC				
61		P31	MTIOC0A, MTIOC0A#, MTCLKC, MTCLKC#, TMRI6	SSLA1	IRQ6
62	VSS				
63		P30	MTIOC0B, MTIOC0B#, MTCLKD, MTCLKD#, TMCI6	SSLA0	IRQ7, COMP3
64		P24	MTIC5U, MTIC5U#, TMCI2, TMO6	RSPCKA	COMP0, DA0
65		P23	MTIC5V, MTIC5V#, TMO2, CACREF	MOSIA	COMP1, DA1
66		P22	MTIC5W, MTIC5W#, TMRI2, TMO4	MISOA	ADTRG2#, COMP2
67		P21	MTCLKA, MTCLKA#, MTIOC9A, MTIOC9A#, TMCI4		IRQ6, ADTRG1#, AN116
68		P20	MTCLKB, MTCLKB#, MTIOC9C, MTIOC9C#, TMRI4		IRQ7, ADTRG0#, AN016
69		P65			AN205
70		P64			AN204
71	AVCC2				
72	VREF				
73	AVSS2				
74		P63			AN203, IRQ7
75		P62			AN202, IRQ6
76		P61			AN201, IRQ5
77		P60			AN200, IRQ4
78		P55			AN211, IRQ3
79		P54			AN210, IRQ2
80		P53			AN209, IRQ1
81		P52			AN208, IRQ0
82		P51			AN207
83		P50			AN206
84		P47			AN103
85		P46			AN102, CMPC12, CMPC13, CMPC30, CMPC31
86		P45			AN101, CMPC02, CMPC03, CMPC20, CMPC21
87		P44			AN100, CMPC10, CMPC11, CMPC32, CMPC33
88		P43			AN003
89		P42			AN002
90		P41			AN001
91		P40			AN000, CMPC00, CMPC01, CMPC22, CMPC23
92	AVCC1				
93	AVCC0				

2. CPU

Figure 2.1 shows register set of the CPU.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW.

Figure 2.1 Register Set of the CPU

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK
0008 0031h	SYSTEM	Memory Wait Cycle Setting Register	MEMWAIT	8	8	3 ICLK
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK
0008 0036h	SYSTEM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3 ICLK
0008 0037h	SYSTEM	High-Speed On-Chip Oscillator Control Register 2	HOCOCR2	8	8	3 ICLK
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK
0008 00A5h	SYSTEM	High-Speed On-Chip Oscillator Wait Control Register	HOCOWTCR	8	8	3 ICLK
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK
0008 1000h	FLASH	ROM Cache Enable Register	ROMCE	16	16	3 ICLK
0008 1004h	FLASH	ROM Cache Invalidate Register	ROMCIV	16	16	3 ICLK
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2 ICLK
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2 ICLK
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK

Table 4.1 List of I/O Registers (Address Order) (7/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 71A1h	ICU	DTC Transfer Request Enable Register 161	DTCER161	8	8	2 ICLK
0008 71A2h	ICU	DTC Transfer Request Enable Register 162	DTCER162	8	8	2 ICLK
0008 71ADh	ICU	DTC Transfer Request Enable Register 173	DTCER173	8	8	2 ICLK
0008 71AEh	ICU	DTC Transfer Request Enable Register 174	DTCER174	8	8	2 ICLK
0008 71AFh	ICU	DTC Transfer Request Enable Register 175	DTCER175	8	8	2 ICLK
0008 71B1h	ICU	DTC Transfer Request Enable Register 177	DTCER177	8	8	2 ICLK
0008 71B2h	ICU	DTC Transfer Request Enable Register 178	DTCER178	8	8	2 ICLK
0008 71B4h	ICU	DTC Transfer Request Enable Register 180	DTCER180	8	8	2 ICLK
0008 71B5h	ICU	DTC Transfer Request Enable Register 181	DTCER181	8	8	2 ICLK
0008 71B7h	ICU	DTC Transfer Request Enable Register 183	DTCER183	8	8	2 ICLK
0008 71B8h	ICU	DTC Transfer Request Enable Register 184	DTCER184	8	8	2 ICLK
0008 71BAh	ICU	DTC Transfer Request Enable Register 186	DTCER186	8	8	2 ICLK
0008 71BBh	ICU	DTC Transfer Request Enable Register 187	DTCER187	8	8	2 ICLK
0008 71BDh	ICU	DTC Transfer Request Enable Register 189	DTCER189	8	8	2 ICLK
0008 71BEh	ICU	DTC Transfer Request Enable Register 190	DTCER190	8	8	2 ICLK
0008 71C0h	ICU	DTC Transfer Request Enable Register 192	DTCER192	8	8	2 ICLK
0008 71C1h	ICU	DTC Transfer Request Enable Register 193	DTCER193	8	8	2 ICLK
0008 71C3h	ICU	DTC Transfer Request Enable Register 195	DTCER195	8	8	2 ICLK
0008 71C4h	ICU	DTC Transfer Request Enable Register 196	DTCER196	8	8	2 ICLK
0008 71CBh	ICU	DTC Transfer Request Enable Register 203*2	DTCER203	8	8	2 ICLK
0008 71CCh	ICU	DTC Transfer Request Enable Register 204*2	DTCER204	8	8	2 ICLK
0008 71CDh	ICU	DTC Transfer Request Enable Register 205*2	DTCER205	8	8	2 ICLK
0008 71CEh	ICU	DTC Transfer Request Enable Register 206*2	DTCER206	8	8	2 ICLK
0008 71CFh	ICU	DTC Transfer Request Enable Register 207*2	DTCER207	8	8	2 ICLK
0008 71D0h	ICU	DTC Transfer Request Enable Register 208*2	DTCER208	8	8	2 ICLK
0008 71D1h	ICU	DTC Transfer Request Enable Register 209*2	DTCER209	8	8	2 ICLK
0008 71D2h	ICU	DTC Transfer Request Enable Register 210*2	DTCER210	8	8	2 ICLK
0008 71D4h	ICU	DTC Transfer Request Enable Register 212*2	DTCER212	8	8	2 ICLK
0008 71D5h	ICU	DTC Transfer Request Enable Register 213*2	DTCER213	8	8	2 ICLK
0008 71D6h	ICU	DTC Transfer Request Enable Register 214*2	DTCER214	8	8	2 ICLK
0008 71D7h	ICU	DTC Transfer Request Enable Register 215*2	DTCER215	8	8	2 ICLK
0008 71D8h	ICU	DTC Transfer Request Enable Register 216*2	DTCER216	8	8	2 ICLK
0008 71D9h	ICU	DTC Transfer Request Enable Register 217*2	DTCER217	8	8	2 ICLK
0008 71DBh	ICU	DTC Transfer Request Enable Register 219	DTCER219	8	8	2 ICLK
0008 71DCh	ICU	DTC Transfer Request Enable Register 220	DTCER220	8	8	2 ICLK
0008 71DFh	ICU	DTC Transfer Request Enable Register 223	DTCER223	8	8	2 ICLK
0008 71E0h	ICU	DTC Transfer Request Enable Register 224	DTCER224	8	8	2 ICLK
0008 71E3h	ICU	DTC Transfer Request Enable Register 227	DTCER227	8	8	2 ICLK
0008 71E4h	ICU	DTC Transfer Request Enable Register 228	DTCER228	8	8	2 ICLK
0008 71EEh	ICU	DTC Transfer Request Enable Register 238*2	DTCER238	8	8	2 ICLK
0008 71EFh	ICU	DTC Transfer Request Enable Register 239*2	DTCER239	8	8	2 ICLK
0008 71F1h	ICU	DTC Transfer Request Enable Register 241*2	DTCER241	8	8	2 ICLK
0008 71F2h	ICU	DTC Transfer Request Enable Register 242*2	DTCER242	8	8	2 ICLK
0008 71F3h	ICU	DTC Transfer Request Enable Register 243*2	DTCER243	8	8	2 ICLK
0008 71F4h	ICU	DTC Transfer Request Enable Register 244*2	DTCER244	8	8	2 ICLK
0008 71F7h	ICU	DTC Transfer Request Enable Register 247	DTCER247	8	8	2 ICLK
0008 71F8h	ICU	DTC Transfer Request Enable Register 248	DTCER248	8	8	2 ICLK
0008 7202h	ICU	Interrupt Request Enable Register 02	IER02	8	8	2 ICLK
0008 7203h	ICU	Interrupt Request Enable Register 03	IER03	8	8	2 ICLK
0008 7204h	ICU	Interrupt Request Enable Register 04	IER04	8	8	2 ICLK
0008 7205h	ICU	Interrupt Request Enable Register 05	IER05	8	8	2 ICLK
0008 7206h	ICU	Interrupt Request Enable Register 06*2	IER06	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (12/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 8227h	TMR5	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB
0008 8228h	TMR4	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8229h	TMR5	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB
0008 822Ah	TMR4	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 822Bh	TMR5	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB
0008 8230h	TMR6	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8231h	TMR7	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8232h	TMR6	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8233h	TMR7	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8234h	TMR6	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8235h	TMR7	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB
0008 8236h	TMR6	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8237h	TMR7	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB
0008 8238h	TMR6	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8239h	TMR7	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB
0008 823Ah	TMR6	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 823Bh	TMR7	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2 or 3 PCLKB
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2 or 3 PCLKB
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2 or 3 PCLKB
0008 8300h	RIIC0	I²C-bus Control Register 1	ICCR1	8	8	2 or 3 PCLKB
0008 8301h	RIIC0	I²C-bus Control Register 2	ICCR2	8	8	2 or 3 PCLKB
0008 8302h	RIIC0	I²C-bus Mode Register 1	ICMR1	8	8	2 or 3 PCLKB
0008 8303h	RIIC0	I²C-bus Mode Register 2	ICMR2	8	8	2 or 3 PCLKB
0008 8304h	RIIC0	I²C-bus Mode Register 3	ICMR3	8	8	2 or 3 PCLKB
0008 8305h	RIIC0	I²C-bus Function Enable Register	ICFER	8	8	2 or 3 PCLKB
0008 8306h	RIIC0	I²C-bus Status Enable Register	ICSER	8	8	2 or 3 PCLKB
0008 8307h	RIIC0	I²C-bus Interrupt Enable Register	ICIER	8	8	2 or 3 PCLKB
0008 8308h	RIIC0	I²C-bus Status Register 1	ICSR1	8	8	2 or 3 PCLKB
0008 8309h	RIIC0	I²C-bus Status Register 2	ICSR2	8	8	2 or 3 PCLKB
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 or 3 PCLKB
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2 or 3 PCLKB
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2 or 3 PCLKB
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2 or 3 PCLKB
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2 or 3 PCLKB
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2 or 3 PCLKB
0008 8310h	RIIC0	I²C-bus Bit Rate Low-Level Register	ICBRL	8	8	2 or 3 PCLKB
0008 8311h	RIIC0	I²C-bus Bit Rate High-Level Register	ICBRH	8	8	2 or 3 PCLKB
0008 8312h	RIIC0	I²C-bus Transmit Data Register	ICDRT	8	8	2 or 3 PCLKB
0008 8313h	RIIC0	I²C-bus Receive Data Register	ICDRR	8	8	2 or 3 PCLKB
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2 or 3 PCLKB
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2 or 3 PCLKB
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2 or 3 PCLKB
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2 or 3 PCLKB
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2 or 3 PCLKB
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2 or 3 PCLKB
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2 or 3 PCLKB
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2 or 3 PCLKB
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2 or 3 PCLKB
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2 or 3 PCLKB
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2 or 3 PCLKB
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (14/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 9214h	S12AD1	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB
0008 9216h	S12AD1	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB
0008 9218h	S12AD1	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB
0008 921Eh	S12AD1	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB
0008 9220h	S12AD1	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB
0008 9222h	S12AD1	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB
0008 9224h	S12AD1	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB
0008 9226h	S12AD1	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB
0008 9240h	S12AD1	A/D Data Register 16	ADDR16	16	16	2 or 3 PCLKB
0008 9266h	S12AD1	A/D Sample-and-hold Circuit Control Register	ADSHCR	16	16	2 or 3 PCLKB
0008 927Ah	S12AD1	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB
0008 9280h	S12AD1	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB
0008 9284h	S12AD1	A/D Data Duplication Register A	ADDBLDRA	16	16	2 or 3 PCLKB
0008 9286h	S12AD1	A/D Data Duplication Register B	ADDBLDRB	16	16	2 or 3 PCLKB
0008 92D4h	S12AD1	A/D Channel Select Register C0	ADANSC0	16	16	2 or 3 PCLKB
0008 92D6h	S12AD1	A/D Channel Select Register C1	ADANSC1	16	16	2 or 3 PCLKB
0008 92D9h	S12AD1	A/D Group C Trigger Select Register	ADGCTRGR	8	8	2 or 3 PCLKB
0008 92DDh	S12AD1	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB
0008 92E0h	S12AD1	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB
0008 92E1h	S12AD1	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB
0008 92E2h	S12AD1	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB
0008 92E3h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB
0008 93A0h	S12AD1	A/D Programmable Gain Amplifier Control Register	ADPGACR	16	16	2 or 3 PCLKB
0008 93A2h	S12AD1	A/D Programmable Gain Amplifier Gain Setting Register 0	ADPGAGS0	16	16	2 or 3 PCLKB
0008 9400h	S12AD2	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB
0008 9404h	S12AD2	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB
0008 9408h	S12AD2	A/D-Converted Value Addition/Average Function Channel Select Register 0	ADADS0	16	16	2 or 3 PCLKB
0008 940Ch	S12AD2	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB
0008 940Eh	S12AD2	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB
0008 9410h	S12AD2	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB
0008 9412h	S12AD2	A/D Conversion Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB
0008 9414h	S12AD2	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB
0008 9418h	S12AD2	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB
0008 941Ch	S12AD2	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB
0008 941Eh	S12AD2	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB
0008 9420h	S12AD2	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB
0008 9422h	S12AD2	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB
0008 9424h	S12AD2	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB
0008 9426h	S12AD2	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB
0008 9428h	S12AD2	A/D Data Register 4	ADDR4	16	16	2 or 3 PCLKB
0008 942Ah	S12AD2	A/D Data Register 5	ADDR5	16	16	2 or 3 PCLKB
0008 942Ch	S12AD2	A/D Data Register 6	ADDR6	16	16	2 or 3 PCLKB
0008 942Eh	S12AD2	A/D Data Register 7	ADDR7	16	16	2 or 3 PCLKB
0008 9430h	S12AD2	A/D Data Register 8	ADDR8	16	16	2 or 3 PCLKB
0008 9432h	S12AD2	A/D Data Register 9	ADDR9	16	16	2 or 3 PCLKB
0008 9434h	S12AD2	A/D Data Register 10	ADDR10	16	16	2 or 3 PCLKB
0008 9436h	S12AD2	A/D Data Register 11	ADDR11	16	16	2 or 3 PCLKB
0008 947Ah	S12AD2	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB
0008 9480h	S12AD2	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB
0008 9484h	S12AD2	A/D Data Duplication Register A	ADDBLDRA	16	16	2 or 3 PCLKB
0008 9486h	S12AD2	A/D Data Duplication Register B	ADDBLDRB	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (18/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 C09Ah	PORTD	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C09Bh	PORTD	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C09Dh	PORTE	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C0C0h	PORT0	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C1h	PORT1	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C2h	PORT2	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C3h	PORT3	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C4h	PORT4	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C5h	PORT5	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C6h	PORT6	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C7h	PORT7	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C8h	PORT8	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C9h	PORT9	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CAh	PORTA	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CBh	PORTB	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CDh	PORTD	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CEh	PORTE	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0E0h	PORT0	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E1h	PORT1	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E2h	PORT2	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E3h	PORT3	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E7h	PORT7	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E8h	PORT8	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E9h	PORT9	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EAh	PORTA	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EBh	PORTB	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EDh	PORTD	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EEh	PORTE	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C11Fh	MPC	Write-Protect Register	PWPR	8	8	2 or 3 PCLKB
0008 C140h	MPC	P00 Pin Function Control Register	P00PFS	8	8	2 or 3 PCLKB
0008 C141h	MPC	P01 Pin Function Control Register	P01PFS	8	8	2 or 3 PCLKB
0008 C142h	MPC	P02 Pin Function Control Register	P02PFS	8	8	2 or 3 PCLKB
0008 C148h	MPC	P10 Pin Function Control Register	P10PFS	8	8	2 or 3 PCLKB
0008 C149h	MPC	P11 Pin Function Control Register	P11PFS	8	8	2 or 3 PCLKB
0008 C150h	MPC	P20 Pin Function Control Register	P20PFS	8	8	2 or 3 PCLKB
0008 C151h	MPC	P21 Pin Function Control Register	P21PFS	8	8	2 or 3 PCLKB
0008 C152h	MPC	P22 Pin Function Control Register	P22PFS	8	8	2 or 3 PCLKB
0008 C153h	MPC	P23 Pin Function Control Register	P23PFS	8	8	2 or 3 PCLKB
0008 C154h	MPC	P24 Pin Function Control Register	P24PFS	8	8	2 or 3 PCLKB
0008 C158h	MPC	P30 Pin Function Control Register	P30PFS	8	8	2 or 3 PCLKB
0008 C159h	MPC	P31 Pin Function Control Register	P31PFS	8	8	2 or 3 PCLKB
0008 C15Ah	MPC	P32 Pin Function Control Register	P32PFS	8	8	2 or 3 PCLKB
0008 C15Bh	MPC	P33 Pin Function Control Register	P33PFS	8	8	2 or 3 PCLKB
0008 C160h	MPC	P40 Pin Function Control Register	P40PFS	8	8	2 or 3 PCLKB
0008 C161h	MPC	P41 Pin Function Control Register	P41PFS	8	8	2 or 3 PCLKB
0008 C162h	MPC	P42 Pin Function Control Register	P42PFS	8	8	2 or 3 PCLKB
0008 C163h	MPC	P43 Pin Function Control Register	P43PFS	8	8	2 or 3 PCLKB
0008 C164h	MPC	P44 Pin Function Control Register	P44PFS	8	8	2 or 3 PCLKB
0008 C165h	MPC	P45 Pin Function Control Register	P45PFS	8	8	2 or 3 PCLKB
0008 C166h	MPC	P46 Pin Function Control Register	P46PFS	8	8	2 or 3 PCLKB
0008 C167h	MPC	P47 Pin Function Control Register	P47PFS	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (22/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000A 836Dh	RSCAN0	Transmit Buffer Status Register 1*2	TMSTS1	8	8	1 or 2 PCLKB
000A 836Eh	RSCAN0	Transmit Buffer Status Register 2*2	TMSTS2	8	8	1 or 2 PCLKB
000A 836Fh	RSCAN0	Transmit Buffer Status Register 3*2	TMSTS3	8	8	1 or 2 PCLKB
000A 8374h	RSCAN0	Transmit Buffer Transmit Request Status Register*2	TMTRSTS	16	16	2 or 3 PCLKB
000A 8376h	RSCAN0	Transmit Buffer Transmit Complete Status Register*2	TMTCSTS	16	16	2 or 3 PCLKB
000A 8378h	RSCAN0	Transmit Buffer Transmit Abort Status Register*2	TMTASTS	16	16	2 or 3 PCLKB
000A 837Ah	RSCAN0	Transmit Buffer Interrupt Enable Register*2	TMIEC	16	16	2 or 3 PCLKB
000A 837Ch	RSCAN0	Transmit History Buffer Control Register*2	THLCC0	16	16	2 or 3 PCLKB
000A 8380h	RSCAN0	Transmit History Buffer Status Register*2	THLSTS0	16	16	2 or 3 PCLKB
000A 8384h	RSCAN0	Transmit History Buffer Pointer Control Register*2	THLPCTR0	16	16	2 or 3 PCLKB
000A 8388h	RSCAN	Global Transmit Interrupt Status Register*2	GTINTSTS	16	16	2 or 3 PCLKB
000A 838Ah	RSCAN	Global RAM Window Control Register*2	GRWCR	16	16	2 or 3 PCLKB
000A 838Ch	RSCAN	Global Test Configuration Register*2	GTSTCFG	16	16	2 or 3 PCLKB
000A 838Eh	RSCAN	Global Test Control Register*2	GTSTCTRL	8	8	1 or 2 PCLKB
000A 8394h	RSCAN	Global Test Protection Unlock Register*2	GLOCKK	16	16	2 or 3 PCLKB
000A 83A0h	RSCAN	Receive Rule Entry Register 0AL*2	GAFLIDL0	16	16	2 or 3 PCLKB
000A 83A0h	RSCAN	Receive Buffer Register 0AL*2	RMIDL0	16	16	2 or 3 PCLKB
000A 83A2h	RSCAN	Receive Rule Entry Register 0AH*2	GAFLIDH0	16	16	2 or 3 PCLKB
000A 83A2h	RSCAN	Receive Buffer Register 0AH*2	RMIDH0	16	16	2 or 3 PCLKB
000A 83A4h	RSCAN	Receive Rule Entry Register 0BL*2	GAFLML0	16	16	2 or 3 PCLKB
000A 83A4h	RSCAN	Receive Buffer Register 0BL*2	RMTS0	16	16	2 or 3 PCLKB
000A 83A6h	RSCAN	Receive Rule Entry Register 0BH*2	GAFLMH0	16	16	2 or 3 PCLKB
000A 83A6h	RSCAN	Receive Buffer Register 0BH*2	RMPTR0	16	16	2 or 3 PCLKB
000A 83A8h	RSCAN	Receive Rule Entry Register 0CL*2	GAFLPL0	16	16	2 or 3 PCLKB
000A 83A8h	RSCAN	Receive Buffer Register 0CL*2	RMDF00	16	16	2 or 3 PCLKB
000A 83AAh	RSCAN	Receive Rule Entry Register 0CH*2	GAFLPH0	16	16	2 or 3 PCLKB
000A 83AAh	RSCAN	Receive Buffer Register 0CH*2	RMDF10	16	16	2 or 3 PCLKB
000A 83ACh	RSCAN	Receive Rule Entry Register 1AL*2	GAFLIDL1	16	16	2 or 3 PCLKB
000A 83ACh	RSCAN	Receive Buffer Register 0DL*2	RMDF20	16	16	2 or 3 PCLKB
000A 83AEh	RSCAN	Receive Rule Entry Register 1AH*2	GAFLIDH1	16	16	2 or 3 PCLKB
000A 83AEh	RSCAN	Receive Buffer Register 0DH*2	RMDF30	16	16	2 or 3 PCLKB
000A 83B0h	RSCAN	Receive Rule Entry Register 1BL*2	GAFLML1	16	16	2 or 3 PCLKB
000A 83B0h	RSCAN	Receive Buffer Register 1AL*2	RMIDL1	16	16	2 or 3 PCLKB
000A 83B2h	RSCAN	Receive Rule Entry Register 1BH*2	GAFLMH1	16	16	2 or 3 PCLKB
000A 83B2h	RSCAN	Receive Buffer Register 1AH*2	RMIDH1	16	16	2 or 3 PCLKB
000A 83B4h	RSCAN	Receive Rule Entry Register 1CL*2	GAFLPL1	16	16	2 or 3 PCLKB
000A 83B4h	RSCAN	Receive Buffer Register 1BL*2	RMTS1	16	16	2 or 3 PCLKB
000A 83B6h	RSCAN	Receive Rule Entry Register 1CH*2	GAFLPH1	16	16	2 or 3 PCLKB
000A 83B6h	RSCAN	Receive Buffer Register 1BH*2	RMPTR1	16	16	2 or 3 PCLKB
000A 83B8h	RSCAN	Receive Rule Entry Register 2AL*2	GAFLIDL2	16	16	2 or 3 PCLKB
000A 83B8h	RSCAN	Receive Buffer Register 1CL*2	RMDF01	16	16	2 or 3 PCLKB
000A 83BAh	RSCAN	Receive Rule Entry Register 2AH*2	GAFLIDH2	16	16	2 or 3 PCLKB
000A 83BAh	RSCAN	Receive Buffer Register 1CH*2	RMDF11	16	16	2 or 3 PCLKB
000A 83BCh	RSCAN	Receive Rule Entry Register 2BL*2	GAFLML2	16	16	2 or 3 PCLKB
000A 83BCh	RSCAN	Receive Buffer Register 1DL*2	RMDF21	16	16	2 or 3 PCLKB
000A 83BEh	RSCAN	Receive Rule Entry Register 2BH*2	GAFLMH2	16	16	2 or 3 PCLKB
000A 83BEh	RSCAN	Receive Buffer Register 1DH*2	RMDF31	16	16	2 or 3 PCLKB
000A 83C0h	RSCAN	Receive Rule Entry Register 2CL*2	GAFLPL2	16	16	2 or 3 PCLKB
000A 83C0h	RSCAN	Receive Buffer Register 2AL*2	RMIDL2	16	16	2 or 3 PCLKB
000A 83C2h	RSCAN	Receive Rule Entry Register 2CH*2	GAFLPH2	16	16	2 or 3 PCLKB
000A 83C2h	RSCAN	Receive Buffer Register 2AH*2	RMIDH2	16	16	2 or 3 PCLKB
000A 83C4h	RSCAN	Receive Rule Entry Register 3AL*2	GAFLIDL3	16	16	2 or 3 PCLKB

5.2 DC Characteristics

Table 5.3 DC Characteristics (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)	V_{IH}	VCC × 0.7	—	5.8	V	
	Ports B1, B2 (5 V tolerant)		VCC × 0.8	—	5.8		
	Ports 00 to 02, ports 10, 11, ports 20 to 24, ports 30 to 33, 36, 37, ports 70 to 76, ports 80 to 82, ports 90 to 96, ports A0 to A5, port B0, ports B3 to B7, ports D0 to D7, ports E0 to E5, RES#		VCC × 0.8	—	VCC + 0.3		
	Ports 40 to 47, ports 50 to 55, ports 60 to 65		VREF × 0.8	—	VREF + 0.3		
	RIIC input pin (except for SMBus)	V_{IL}	–0.3	—	VCC × 0.3		
	Ports 40 to 47, ports 50 to 55, ports 60 to 65		–0.3	—	VREF × 0.2		
	Other than RIIC input pin, Other than ports 40 to 47, 50 to 55, or 60 to 65		–0.3	—	VCC × 0.2		
	RIIC input pin (except for SMBus)	ΔV_T	VCC × 0.05	—	—		
	Ports 40 to 47, ports 50 to 55, ports 60 to 65		VREF × 0.1	—	—		
	Other than RIIC input pin, Other than ports 40 to 47, 50 to 55, or 60 to 65		VCC × 0.1	—	—		
Input level voltage (except for Schmitt trigger input pins)	MD	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL (external clock input)		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (SMBus)		2.1	—	VCC + 0.3		VCC ≤ 5.2 V
	MD	V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL (external clock input)		–0.3	—	VCC × 0.2		
	RIIC input pin (SMBus)		–0.3	—	0.8		VCC ≤ 5.2 V

Table 5.7 DC Characteristics (5)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total consumption power*1	Pd	—	570	mW	

Note 1. Total power dissipated by the entire chip (including output currents)

Table 5.8 DC Characteristics (6)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

	Item		Symbol	Min.	Typ.*2	Max.	Unit	Test Conditions
Analog power supply current	A/D unit 0	During A/D conversion (programmable gain amplifier in use)	I_{AVCC}	—	1.5	2.5	mA	
		During A/D conversion (programmable gain amplifier not in use)		—	1.0	1.8		
	A/D unit 1	During A/D conversion (sample-and-hold circuits in use, programmable gain amplifier in use)		—	4.6	6.9		
		During A/D conversion (sample-and-hold circuits in use, programmable gain amplifier not in use)		—	3.1	4.8		
		During A/D conversion (sample-and-hold circuits not in use, programmable gain amplifier in use)		—	2.5	3.9		
		During A/D conversion (sample-and-hold circuits not in use, programmable gain amplifier not in use)		—	1.0	1.8		
	A/D unit 2			—	1.0	1.8		
	During D/A conversion (per channel)*1			—	0.7	1.0		
	Waiting for A/D or D/A conversion (all units)			—	—	2.2	µA	
	Waiting for A/D conversion (all units)			—	—	1.2	µA	
Comparator C operating current*3	Comparator enabled		I_{CMP}	—	40.0	60.0	µA	

Note 1. The value of the D/A converter is the value of the power supply current including the reference current.
Note 2. When VCC =AVCC0 = AVCC1 = AVCC2 = VREF = 5 V.
Note 3. Current consumed only by the comparator C module.

Table 5.9 DC Characteristics (7)

Conditions: VCC = 0 V to AVCC0, AVCC0 = AVCC1 = AVCC2 = VREF = 0 V to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power-on VCC rising gradient	At normal startup	SrVCC	0.02	—	20	ms/V	
	Voltage monitoring 0 reset enabled at startup*1, *2		0.02	—	—		

Note 1. When OFS1.LVDAS = 0.
Note 2. Turn on the power supply voltage according to the normal startup rising gradient because the register settings set by OFS1 are not read in boot mode.

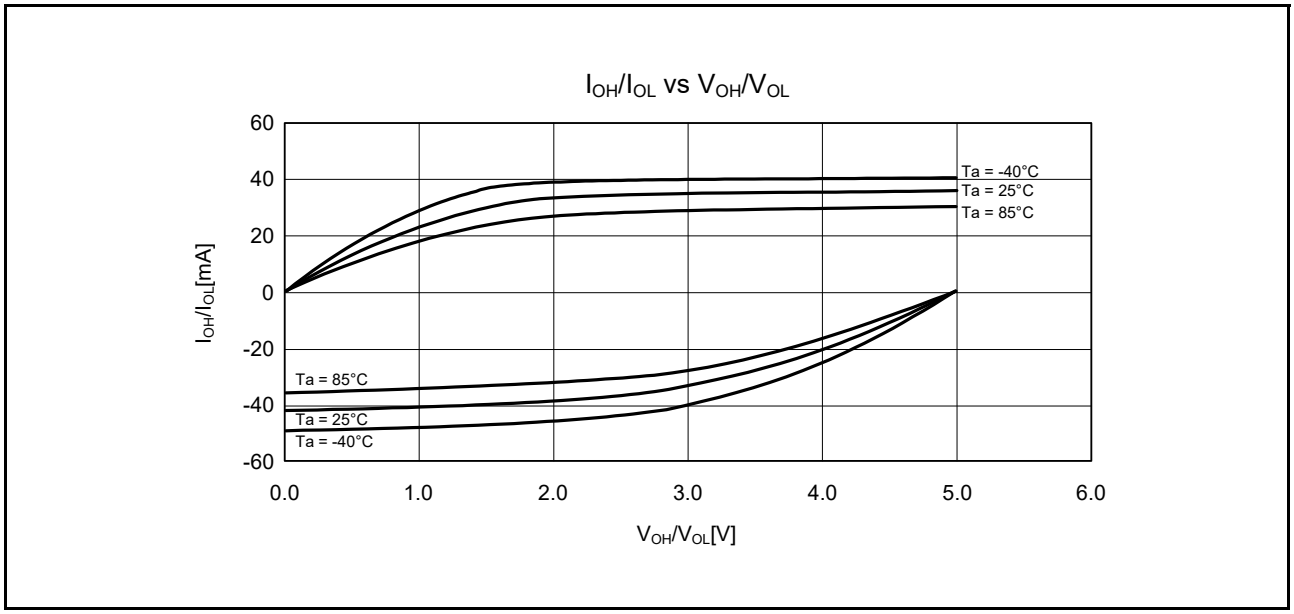


Figure 5.8 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.0 V when Normal Output is Selected (Reference Data)**

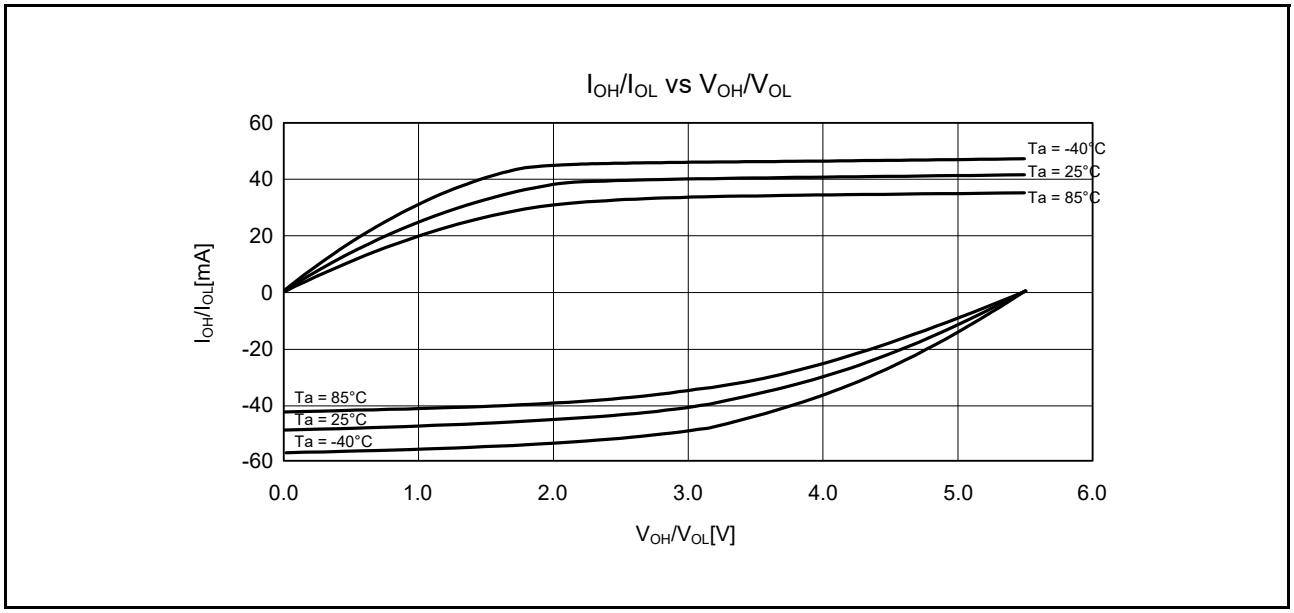


Figure 5.9 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.5 V when Normal Output is Selected (Reference Data)**

5.2.3 Standard I/O Pin Output Characteristics (3)

Figure 5.14 to Figure 5.17 show the output characteristics of the large current ports.

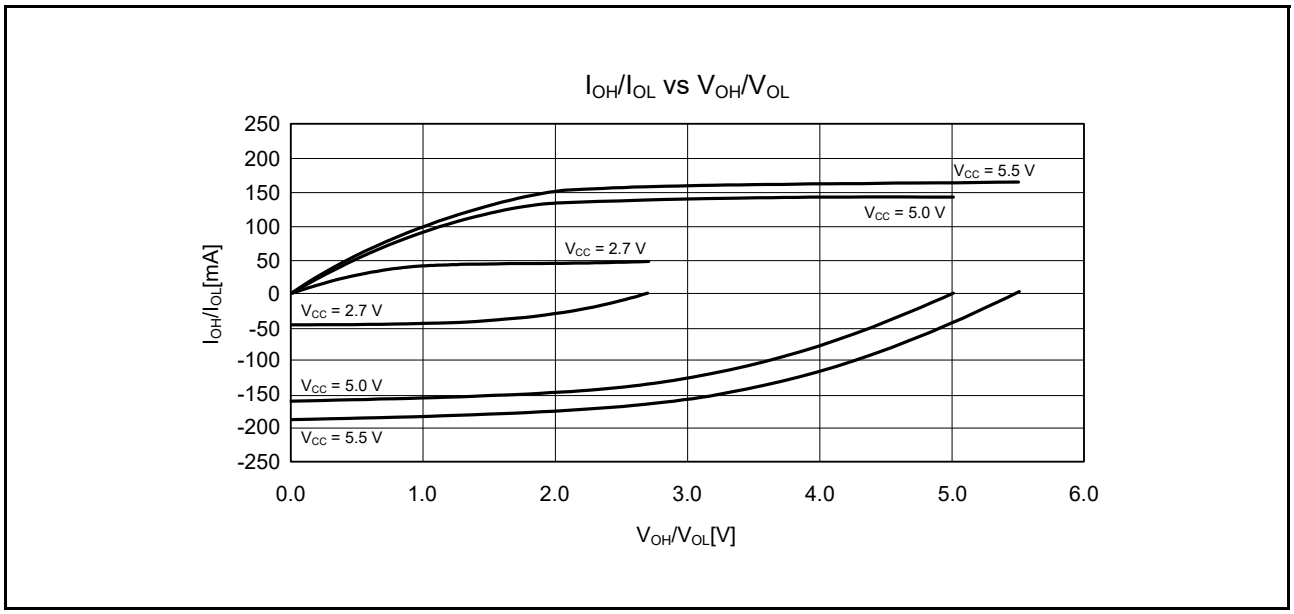


Figure 5.14 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics of Large Current Ports at T_a = 25°C (Reference Data)

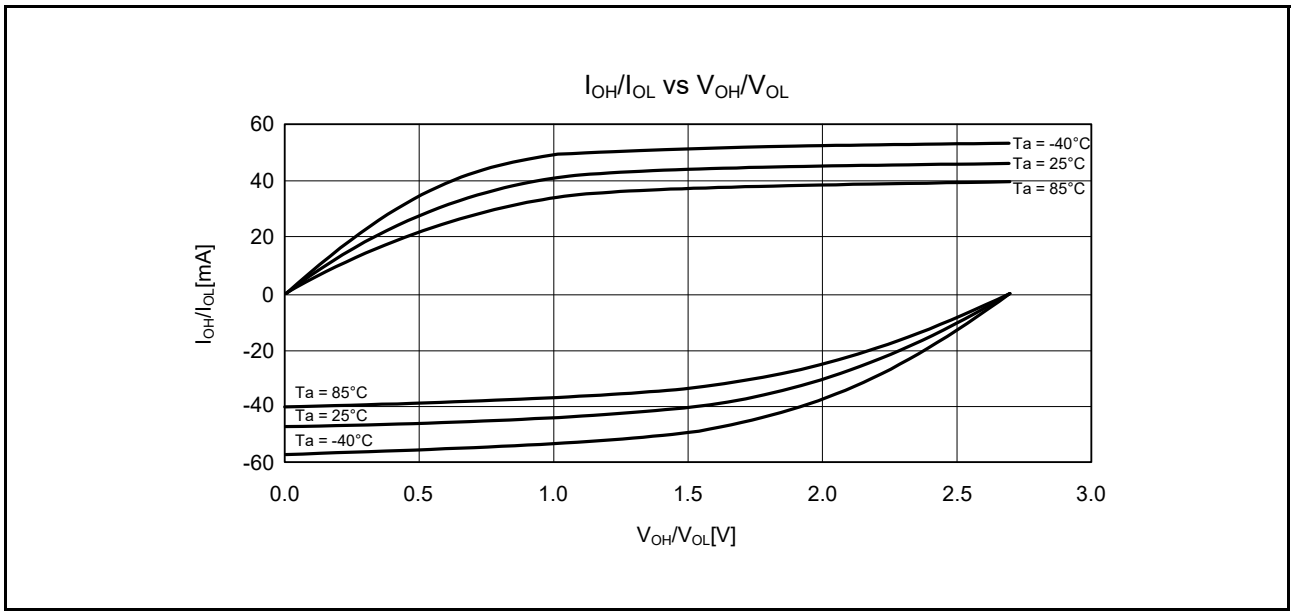


Figure 5.15 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Large Current Ports at VCC = 2.7 V (Reference Data)

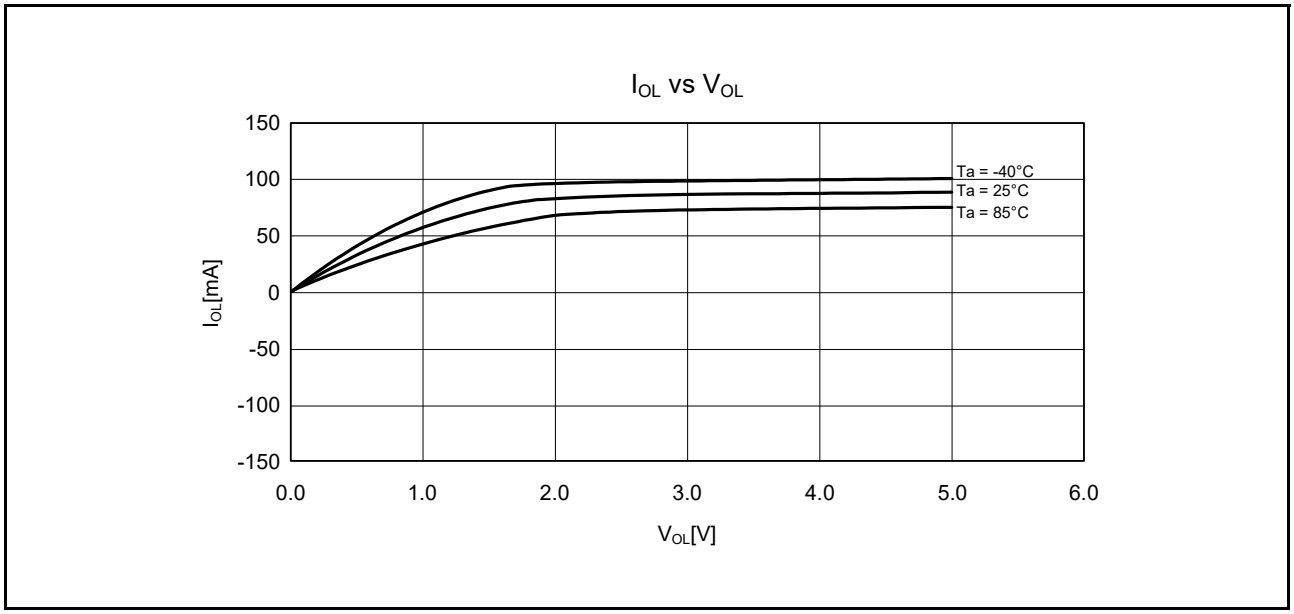


Figure 5.20 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 5.0 V (Reference Data)

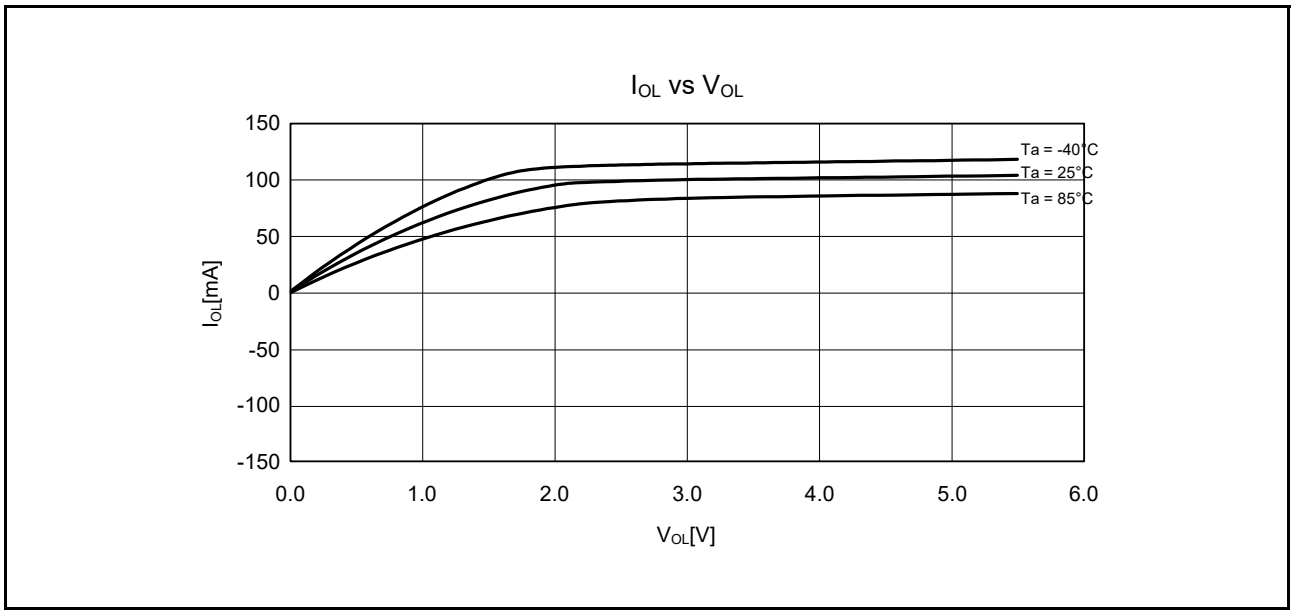


Figure 5.21 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 5.5 V (Reference Data)

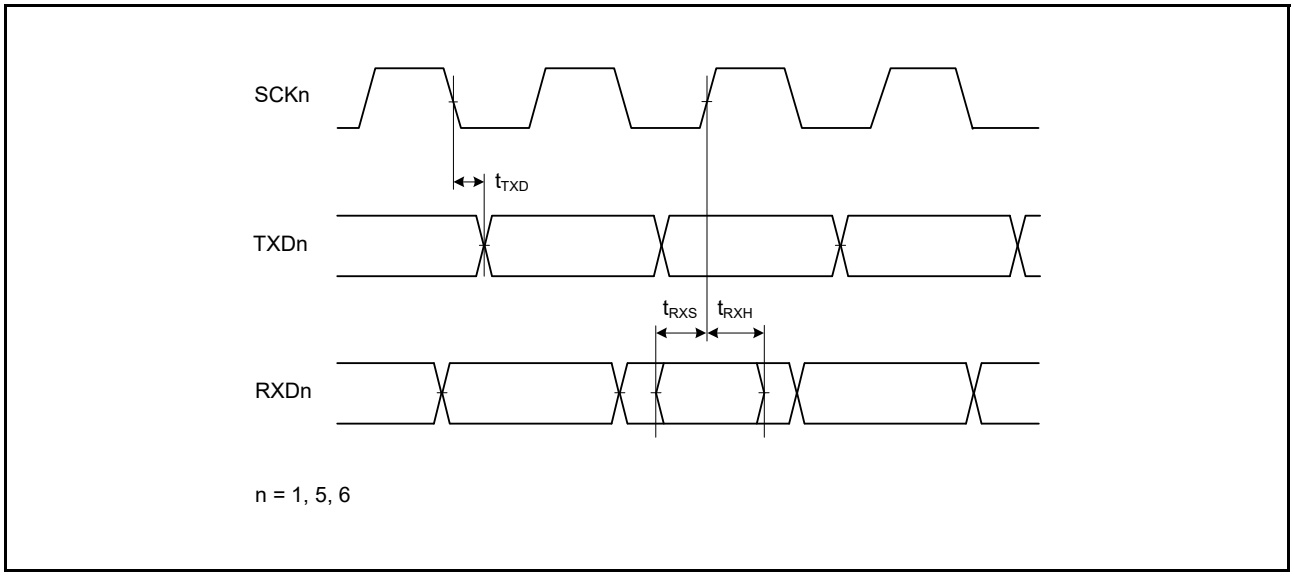


Figure 5.45 SCI Input/Output Timing: Clock Synchronous Mode

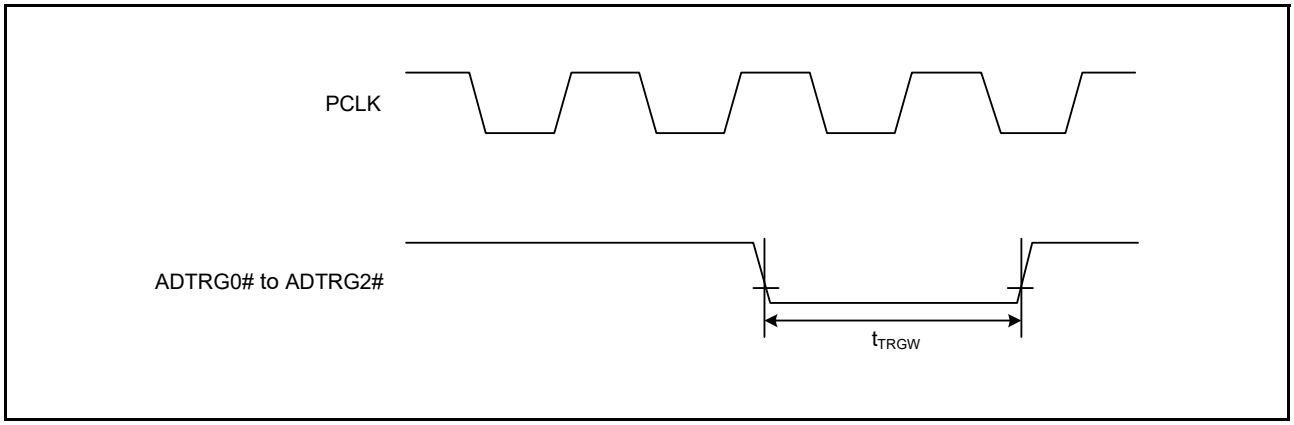


Figure 5.46 A/D Converter External Trigger Input Timing

5.7 D/A Conversion Characteristics

Table 5.34 Characteristics of D/A Conversion (Chip Version A)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	—	8	Bit	
Conversion time	t_{DCONV}	—	—	3.0	µs	
Absolute accuracy	—	—	—	±3.0	LSB	

Table 5.35 Characteristics of D/A Conversion (Chip Version B)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	—	8	Bit	
Conversion time	t_{DCONV}	—	—	3.0	µs	
Absolute accuracy	—	—	—	±3.0	LSB	
Output load resistance	—	4	—	—	MΩ	
Output load capacity	—	—	—	35	pF	
Output resistance	—	—	9.0	—	kΩ	

Note: When using ports 23 and 24 as DA0 and DA1 outputs, make sure that VCC ≥ DA output voltage.

REVISION HISTORY	RX24T Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Nov 30, 2015	—	First edition, issued	
2.00	Apr 14, 2017	All	Chip version B, added The name of the previous product, changed to chip version A according to the above The specification of the HOCO, added The 64-pin package, added The specification of the voltage detection 0 level select bit, changed	TN-RX*-A171A/E
		5. Electrical Characteristics		
		—	The characteristics of HOCO-/GPT-/RSCAN-related and chip version B, added	
		72	Table 5.3 DC Characteristics (1): ports 36 and 37, added	
		78	Table 5.8 DC Characteristics (6), changed	
		100	Table 5.25 Timing of On-Chip Peripheral Modules (3), changed	TN-RX*-A170A/E
		115	Table 5.34 Characteristics of D/A Conversion (Chip Version A), changed	TN-RX*-A170A/E
		125	Figure 5.63 Connecting Capacitors (64 Pins), added	
		Appendix 1. Package Dimensions		
		126	Figure A 100-Pin LFQFP (PLQP0100KB-B), package part number, changed	
		128	Figure C 80-Pin LFQFP (PLQP0080KB-B), package part number, changed	
		129	Figure D 64-Pin LFQFP (PLQP0064KB-C), added	

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