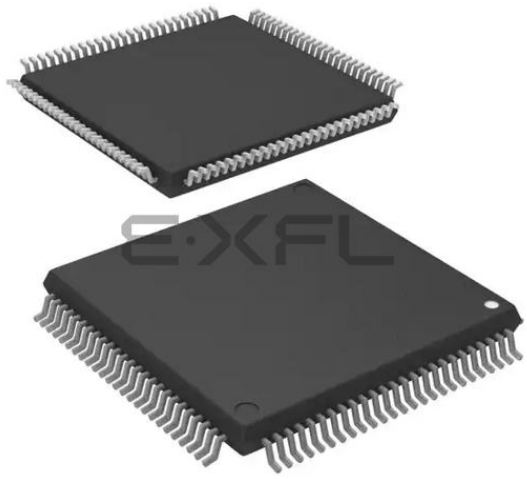
Renesas Electronics America Inc - R5F524T8ADFP#31 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 22x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f524t8adfp-31

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX24T Group			
		Chip Version B	Chip Version A		
		100 Pins	100 Pins	80 Pins	64Pins
Memory	ROM	512 K/384 K/ 256 Kbytes	256 K/128 Kbytes		
	RAM	32 Kbytes	16 Kbytes		
	E2 DataFlash	8 Kbytes			
Interrupts	External interrupts	NMI, IRQ0 to IRQ7			
DTC	Data transfer controller (DTCa)	Available			
Timers	Multi-function timer pulse unit 3 (MTU3d)	9 channels			
	General PWM timer (GPTB)	4 channels	Not supported		
	Port output enable 3 (POE3b)	Not supported	Available		
	Port output enable 3 (POE3A)	Available	Not supported		
	8-bit timer (TMR)	2 channels × 4 units			
	Compare match timer (CMT)	2 channels × 2 units			
	Independent watchdog timer (IWDTa)	Available			
Communications	Serial communications interfaces (SCIg) [including simple I^2C and simple SPI]	3 channels (SCI1, SCI5, SCI6)			
	I^2C bus interface (RIICa)	1 channel			
	Serial peripheral interface (RSPIb)	1 channel			
	CAN module (RSCAN)	1 channel	Not supported		
12-bit A/D converter (S12ADF) (Internal high-precision channel)		5 channels × 2 units, 12 channels × 1 unit (4 channels × 2 units, 12 channels × 1 unit)		5 channels × 2 units, 7 channels × 1 unit (4 channels × 2 units, 7 channels × 1 unit)	3 channels × 1 unit, 4 channels × 1 unit, 5 channels × 1 unit (3 channels × 1 unit, 3 channels × 1 unit, 5 channels × 1 unit)
	3 channels simultaneous sampling	3 channels/unit 1			
	Programmable gain amplifier	1 channel/unit 0, 3 channels/unit 1			
Comparator C (CMPC)		4 channels			
		Without reference voltage external input	With reference voltage external input		
8-bit D/A converter (DA)		Not supported	Available		
8-bit D/A converter (DAa)		Available	Not supported		
CRC calculator (CRC)		Available			
Packages		100-pin LFQFP	100-pin LFQFP	80-pin LFQFP/LQFP	64-pin LFQFP

Table 1.4 Pin Functions (3/4)

Classifications	Pin Name	I/O	Description
I²C bus interface (RIICa)	SCL0	I/O	Input/output pin for I²C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA0	I/O	Input/output pin for I²C bus interface data. Bus can be directly driven by the N-channel open drain output.
Serial peripheral interface (RSPIb)	RSPCKA	I/O	Input/output pin for the RSPI clock.
	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master.
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave.
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI.
CAN module (RSCAN)	CRXD0	Input	Input pin
	CTXD0	Output	Output pin
12-bit A/D converter (S12ADF)	AN000 to AN003, AN016, AN100 to AN103, AN116, AN200 to AN211	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADST0, ADST1, ADST2	Output	Output pins for A/D conversion status.
	ADTRG0#, ADTRG1#, ADTRG2#	Input	Input pins for the external trigger signals that start the A/D conversion.
8-bit D/A converter (DAa)	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter
Comparator C (CMPC)	COMP0 to COMP3	Output	Comparator detection result output pins.
	CVREFC0, CVREFC1	Input	Analog reference voltage supply pins for comparator C.
	CMPC00 to CMPC03	Input	Analog input pin for CMPC0
	CMPC10 to CMPC13	Input	Analog input pin for CMPC1
	CMPC20 to CMPC23	Input	Analog input pin for CMPC2
	CMPC30 to CMPC33	Input	Analog input pin for CMPC3
Analog power supply	AVCC0	—	Analog power supply and reference power supply pin for 12-bit A/D converter unit 0. Connect the AVCC0 pin to AVCC1, AVCC2, or VREF when 12-bit A/D converter unit 0 is not used.
	AVSS0	—	Analog ground and reference ground pin for 12-bit A/D converter unit 0. Connect the AVSS0 pin to AVSS1 or AVSS2 when 12-bit A/D converter unit 0 is not used.
	AVCC1	—	Analog power supply and reference power supply pin for 12-bit A/D converter unit 1. Connect the AVCC1 pin to AVCC0, AVCC2, or VREF when 12-bit A/D converter unit 1 is not used.
	AVSS1	—	Analog ground and reference ground pin for 12-bit A/D converter unit 1. Connect the AVSS1 pin to AVSS0 or AVSS2 when 12-bit A/D converter unit 1 is not used.
	AVCC2	—	Analog power supply and reference power supply pin for 12-bit A/D converter unit 2. Connect the AVCC2 pin to AVCC0, AVCC1, or VREF when 12-bit A/D converter unit 2 is not used.
	AVSS2	—	Analog ground and reference ground pin for 12-bit A/D converter unit 2. Analog ground pin for comparator C and 8-bit D/A converter. Connect the AVSS2 pin to AVSS0 or AVSS1 when 12-bit A/D converter unit 2, comparator C and 8-bit D/A converter are not used.
	VREF	—	Analog power supply pin for comparator C and 8-bit D/A converter. For the 64-pin LFQFP package, the VREF pin is internally connected to AVCC2 and is shared. Connect the VREF pin to AVCC0, AVCC1, or AVCC2 when comparator C and 8-bit D/A converter are not used.

Table 1.6 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version A) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, CAC)	Communications (SCI, RSPI, RIIC)	Others
1		PE5			IRQ0
2		P02	MTIOC9D	CTS1#, RTS1#, SS1#	IRQ5, ADST0
3	VSS				
4		P00			IRQ2, ADST1
5	VCL				
6	MD				FINED
7		P01	POE12#		IRQ4, ADST2
8		PE4	MTCLKC, POE10#		IRQ1
9		PE3	MTCLKD, POE11#		IRQ2
10	RES#				
11	XTAL	P37			
12	VSS				
13	EXTAL	P36			
14	VCC				
15		PE2	POE10#		NMI
16		PE1	MTIOC9D, TMO5	CTS5#, RTS5#, SS5#, SSLA3	
17		PE0	MTIOC9B, TMCI1, TMCI5	SSLA2	
18		PD7	MTIOC9A, TMRI1, TMRI5	SSLA1	
19		PD6	MTIOC9C, TMO1	CTS1#, RTS1#, SS1#, SSLA0	IRQ5, ADST0
20		PD5	TMRI0, TMRI6	RXD1, SMISO1, SSCL1	IRQ3
21		PD4	TMCI0, TMCI6	SCK1	IRQ2
22		PD3	TMO0	TXD1, SMOSI1, SSDA1	
23		PD2	TMCI1, TMO4	SCK5, MOSIA	
24		PD1	TMO2	MISOA	
25		PD0	TMO6	RSPCKA	
26		PB7		SCK5	
27		PB6		RXD5, SMISO5, SSCL5	IRQ5
28		PB5		TXD5, SMOSI5, SSDA5	
29	VCC				
30		PB4	POE8#	CTS5#, RTS5#, SS5#	IRQ3
31	VSS				
32		PB3	MTIOC0A, CACREF	SCK6, RSPCKA	
33		PB2	MTIOC0B, TMRI0, ADSM0	TXD6, SMOSI6, SSDA6, SDA0	
34		PB1	MTIOC0C, TMCI0, ADSM1	RXD6, SMISO6, SSCL6, SCL0	
35		PB0	MTIOC0D, TMO0	TXD6, SMOSI6, SSDA6, MOSIA	ADTRG2#
36		PA5	MTIOC1A, TMCI3	RXD6, SMISO6, SSCL6, MISOA	IRQ1, ADTRG1#
37		PA4	MTIOC1B, TMCI7	SCK6, RSPCKA	ADTRG0#
38		PA3	MTIOC2A, TMRI7	SSLA0	
39		PA2	MTIOC2B, TMO7	CTS6#, RTS6#, SS6#, SSLA1	
40		PA1	MTIOC6A, TMO4	SSLA2	ADTRG0#
41		PA0	MTIOC6C, TMO2	SSLA3	
42	VCC				
43		P96	POE4#		IRQ4
44	VSS				
45		P95	MTIOC6B		
46		P94	MTIOC7A		
47		P93	MTIOC7B		
48		P92	MTIOC6D		
49		P91	MTIOC7C		
50		P90	MTIOC7D		
51		P76	MTIOC4D		
52		P75	MTIOC4C		
53		P74	MTIOC3D		
54		P73	MTIOC4B		

Table 4.1 List of I/O Registers (Address Order) (10/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 73BDh	ICU	Interrupt Source Priority Register 189	IPR189	8	8	2 ICLK
0008 73C0h	ICU	Interrupt Source Priority Register 192	IPR192	8	8	2 ICLK
0008 73C3h	ICU	Interrupt Source Priority Register 195	IPR195	8	8	2 ICLK
0008 73CAh	ICU	Interrupt Source Priority Register 202*2	IPR202	8	8	2 ICLK
0008 73CBh	ICU	Interrupt Source Priority Register 203*2	IPR203	8	8	2 ICLK
0008 73CCh	ICU	Interrupt Source Priority Register 204*2	IPR204	8	8	2 ICLK
0008 73CDh	ICU	Interrupt Source Priority Register 205*2	IPR205	8	8	2 ICLK
0008 73CEh	ICU	Interrupt Source Priority Register 206*2	IPR206	8	8	2 ICLK
0008 73CFh	ICU	Interrupt Source Priority Register 207*2	IPR207	8	8	2 ICLK
0008 73D0h	ICU	Interrupt Source Priority Register 208*2	IPR208	8	8	2 ICLK
0008 73D1h	ICU	Interrupt Source Priority Register 209*2	IPR209	8	8	2 ICLK
0008 73D2h	ICU	Interrupt Source Priority Register 210*2	IPR210	8	8	2 ICLK
0008 73D3h	ICU	Interrupt Source Priority Register 211*2	IPR211	8	8	2 ICLK
0008 73D4h	ICU	Interrupt Source Priority Register 212*2	IPR212	8	8	2 ICLK
0008 73D5h	ICU	Interrupt Source Priority Register 213*2	IPR213	8	8	2 ICLK
0008 73D6h	ICU	Interrupt Source Priority Register 214*2	IPR214	8	8	2 ICLK
0008 73D7h	ICU	Interrupt Source Priority Register 215*2	IPR215	8	8	2 ICLK
0008 73D8h	ICU	Interrupt Source Priority Register 216*2	IPR216	8	8	2 ICLK
0008 73D9h	ICU	Interrupt Source Priority Register 217*2	IPR217	8	8	2 ICLK
0008 73DAh	ICU	Interrupt Source Priority Register 218	IPR218	8	8	2 ICLK
0008 73DEh	ICU	Interrupt Source Priority Register 222	IPR222	8	8	2 ICLK
0008 73E2h	ICU	Interrupt Source Priority Register 226	IPR226	8	8	2 ICLK
0008 73EEh	ICU	Interrupt Source Priority Register 238*2	IPR238	8	8	2 ICLK
0008 73EFh	ICU	Interrupt Source Priority Register 239*2	IPR239	8	8	2 ICLK
0008 73F0h	ICU	Interrupt Source Priority Register 240*2	IPR240	8	8	2 ICLK
0008 73F1h	ICU	Interrupt Source Priority Register 241*2	IPR241	8	8	2 ICLK
0008 73F2h	ICU	Interrupt Source Priority Register 242*2	IPR242	8	8	2 ICLK
0008 73F3h	ICU	Interrupt Source Priority Register 243*2	IPR243	8	8	2 ICLK
0008 73F4h	ICU	Interrupt Source Priority Register 244*2	IPR244	8	8	2 ICLK
0008 73F6h	ICU	Interrupt Source Priority Register 246	IPR246	8	8	2 ICLK
0008 73F7h	ICU	Interrupt Source Priority Register 247	IPR247	8	8	2 ICLK
0008 73F8h	ICU	Interrupt Source Priority Register 248	IPR248	8	8	2 ICLK
0008 73F9h	ICU	Interrupt Source Priority Register 249	IPR249	8	8	2 ICLK
0008 7500h	ICU	IRQ Control Register 0	IRQCR0	8	8	2 ICLK
0008 7501h	ICU	IRQ Control Register 1	IRQCR1	8	8	2 ICLK
0008 7502h	ICU	IRQ Control Register 2	IRQCR2	8	8	2 ICLK
0008 7503h	ICU	IRQ Control Register 3	IRQCR3	8	8	2 ICLK
0008 7504h	ICU	IRQ Control Register 4	IRQCR4	8	8	2 ICLK
0008 7505h	ICU	IRQ Control Register 5	IRQCR5	8	8	2 ICLK
0008 7506h	ICU	IRQ Control Register 6	IRQCR6	8	8	2 ICLK
0008 7507h	ICU	IRQ Control Register 7	IRQCR7	8	8	2 ICLK
0008 7510h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK
0008 7514h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2 or 3 PCLKB
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB
0008 8004h	CMT0	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (11/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 8006h	CMT0	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB
0008 800Ah	CMT1	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB
0008 800Ch	CMT1	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2 or 3 PCLKB
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB
0008 8014h	CMT2	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB
0008 8016h	CMT2	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB
0008 801Ah	CMT3	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB
0008 801Ch	CMT3	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2 or 3 PCLKB
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2 or 3 PCLKB
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2 or 3 PCLKB
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2 or 3 PCLKB
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSTPR	8	8	2 or 3 PCLKB
0008 80C0h	DA	D/A Data Register 0	DADR0	16	16	2 or 3 PCLKB
0008 80C2h	DA	D/A Data Register 1*2	DADR1	16	16	2 or 3 PCLKB
0008 80C4h	DA	D/A Control Register	DACR	8	8	2 or 3 PCLKB
0008 80C5h	DA	DADRm Format Select Register	DADPR	8	8	2 or 3 PCLKB
0008 80C6h	DA	D/A A/D Synchronous Start Control Register*2	DAADSCR	8	8	2 or 3 PCLKB
0008 8200h	TMR0	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8201h	TMR1	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8202h	TMR0	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8203h	TMR1	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8204h	TMR0	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8205h	TMR1	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB
0008 8206h	TMR0	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8207h	TMR1	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB
0008 8208h	TMR0	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8209h	TMR1	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB
0008 820Ah	TMR0	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 820Bh	TMR1	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB
0008 8210h	TMR2	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8211h	TMR3	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8212h	TMR2	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8213h	TMR3	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8214h	TMR2	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8215h	TMR3	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB
0008 8216h	TMR2	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8217h	TMR3	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB
0008 8218h	TMR2	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8219h	TMR3	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB
0008 821Ah	TMR2	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB
0008 8220h	TMR4	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8221h	TMR5	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8222h	TMR4	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8223h	TMR5	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8224h	TMR4	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8225h	TMR5	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB
0008 8226h	TMR4	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (19/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 C168h	MPC	P50 Pin Function Control Register	P50PFS	8	8	2 or 3 PCLKB
0008 C169h	MPC	P51 Pin Function Control Register	P51PFS	8	8	2 or 3 PCLKB
0008 C16Ah	MPC	P52 Pin Function Control Register	P52PFS	8	8	2 or 3 PCLKB
0008 C16Bh	MPC	P53 Pin Function Control Register	P53PFS	8	8	2 or 3 PCLKB
0008 C16Ch	MPC	P54 Pin Function Control Register	P54PFS	8	8	2 or 3 PCLKB
0008 C16Dh	MPC	P55 Pin Function Control Register	P55PFS	8	8	2 or 3 PCLKB
0008 C170h	MPC	P60 Pin Function Control Register	P60PFS	8	8	2 or 3 PCLKB
0008 C171h	MPC	P61 Pin Function Control Register	P61PFS	8	8	2 or 3 PCLKB
0008 C172h	MPC	P62 Pin Function Control Register	P62PFS	8	8	2 or 3 PCLKB
0008 C173h	MPC	P63 Pin Function Control Register	P63PFS	8	8	2 or 3 PCLKB
0008 C174h	MPC	P64 Pin Function Control Register	P64PFS	8	8	2 or 3 PCLKB
0008 C175h	MPC	P65 Pin Function Control Register	P65PFS	8	8	2 or 3 PCLKB
0008 C178h	MPC	P70 Pin Function Control Register	P70PFS	8	8	2 or 3 PCLKB
0008 C179h	MPC	P71 Pin Function Control Register	P71PFS	8	8	2 or 3 PCLKB
0008 C17Ah	MPC	P72 Pin Function Control Register	P72PFS	8	8	2 or 3 PCLKB
0008 C17Bh	MPC	P73 Pin Function Control Register	P73PFS	8	8	2 or 3 PCLKB
0008 C17Ch	MPC	P74 Pin Function Control Register	P74PFS	8	8	2 or 3 PCLKB
0008 C17Dh	MPC	P75 Pin Function Control Register	P75PFS	8	8	2 or 3 PCLKB
0008 C17Eh	MPC	P76 Pin Function Control Register	P76PFS	8	8	2 or 3 PCLKB
0008 C180h	MPC	P80 Pin Function Control Register	P80PFS	8	8	2 or 3 PCLKB
0008 C181h	MPC	P81 Pin Function Control Register	P81PFS	8	8	2 or 3 PCLKB
0008 C182h	MPC	P82 Pin Function Control Register	P82PFS	8	8	2 or 3 PCLKB
0008 C188h	MPC	P90 Pin Function Control Register	P90PFS	8	8	2 or 3 PCLKB
0008 C189h	MPC	P91 Pin Function Control Register	P91PFS	8	8	2 or 3 PCLKB
0008 C18Ah	MPC	P92 Pin Function Control Register	P92PFS	8	8	2 or 3 PCLKB
0008 C18Bh	MPC	P93 Pin Function Control Register	P93PFS	8	8	2 or 3 PCLKB
0008 C18Ch	MPC	P94 Pin Function Control Register	P94PFS	8	8	2 or 3 PCLKB
0008 C18Dh	MPC	P95 Pin Function Control Register	P95PFS	8	8	2 or 3 PCLKB
0008 C18Eh	MPC	P96 Pin Function Control Register	P96PFS	8	8	2 or 3 PCLKB
0008 C190h	MPC	PA0 Pin Function Control Register	PA0PFS	8	8	2 or 3 PCLKB
0008 C191h	MPC	PA1 Pin Function Control Register	PA1PFS	8	8	2 or 3 PCLKB
0008 C192h	MPC	PA2 Pin Function Control Register	PA2PFS	8	8	2 or 3 PCLKB
0008 C193h	MPC	PA3 Pin Function Control Register	PA3PFS	8	8	2 or 3 PCLKB
0008 C194h	MPC	PA4 Pin Function Control Register	PA4PFS	8	8	2 or 3 PCLKB
0008 C195h	MPC	PA5 Pin Function Control Register	PA5PFS	8	8	2 or 3 PCLKB
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2 or 3 PCLKB
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2 or 3 PCLKB
0008 C19Ah	MPC	PB2 Pin Function Control Register	PB2PFS	8	8	2 or 3 PCLKB
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2 or 3 PCLKB
0008 C19Ch	MPC	PB4 Pin Function Control Register	PB4PFS	8	8	2 or 3 PCLKB
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2 or 3 PCLKB
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2 or 3 PCLKB
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2 or 3 PCLKB
0008 C1A8h	MPC	PD0 Pin Function Control Register	PD0PFS	8	8	2 or 3 PCLKB
0008 C1A9h	MPC	PD1 Pin Function Control Register	PD1PFS	8	8	2 or 3 PCLKB
0008 C1AAh	MPC	PD2 Pin Function Control Register	PD2PFS	8	8	2 or 3 PCLKB
0008 C1ABh	MPC	PD3 Pin Function Control Register	PD3PFS	8	8	2 or 3 PCLKB
0008 C1ACh	MPC	PD4 Pin Function Control Register	PD4PFS	8	8	2 or 3 PCLKB
0008 C1ADh	MPC	PD5 Pin Function Control Register	PD5PFS	8	8	2 or 3 PCLKB
0008 C1AEh	MPC	PD6 Pin Function Control Register	PD6PFS	8	8	2 or 3 PCLKB
0008 C1AFh	MPC	PD7 Pin Function Control Register	PD7PFS	8	8	2 or 3 PCLKB
0008 C1B0h	MPC	PE0 Pin Function Control Register	PE0PFS	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (25/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000A 842Ch	RSCAN	Receive Buffer Register 8DL*2	RMDF28	16	16	2 or 3 PCLKB
000A 842Eh	RSCAN	Receive Rule Entry Register 11CH*2	GAFLPH11	16	16	2 or 3 PCLKB
000A 842Eh	RSCAN	Receive Buffer Register 8DH*2	RMDF38	16	16	2 or 3 PCLKB
000A 8430h	RSCAN	Receive Rule Entry Register 12AL*2	GAFLIDL12	16	16	2 or 3 PCLKB
000A 8430h	RSCAN	Receive Buffer Register 9AL*2	RMIDL9	16	16	2 or 3 PCLKB
000A 8432h	RSCAN	Receive Rule Entry Register 12AH*2	GAFLIDH12	16	16	2 or 3 PCLKB
000A 8432h	RSCAN	Receive Buffer Register 9AH*2	RMIDH9	16	16	2 or 3 PCLKB
000A 8434h	RSCAN	Receive Rule Entry Register 12BL*2	GAFLML12	16	16	2 or 3 PCLKB
000A 8434h	RSCAN	Receive Buffer Register 9BL*2	RMTS9	16	16	2 or 3 PCLKB
000A 8436h	RSCAN	Receive Rule Entry Register 12BH*2	GAFLMH12	16	16	2 or 3 PCLKB
000A 8436h	RSCAN	Receive Buffer Register 9BH*2	RMPTR9	16	16	2 or 3 PCLKB
000A 8438h	RSCAN	Receive Rule Entry Register 12CL*2	GAFLPL12	16	16	2 or 3 PCLKB
000A 8438h	RSCAN	Receive Buffer Register 9CL*2	RMDF09	16	16	2 or 3 PCLKB
000A 843Ah	RSCAN	Receive Rule Entry Register 12CH*2	GAFLPH12	16	16	2 or 3 PCLKB
000A 843Ah	RSCAN	Receive Buffer Register 9CH*2	RMDF19	16	16	2 or 3 PCLKB
000A 843Ch	RSCAN	Receive Rule Entry Register 13AL*2	GAFLIDL13	16	16	2 or 3 PCLKB
000A 843Ch	RSCAN	Receive Buffer Register 9DL*2	RMDF29	16	16	2 or 3 PCLKB
000A 843Eh	RSCAN	Receive Rule Entry Register 13AH*2	GAFLIDH13	16	16	2 or 3 PCLKB
000A 843Eh	RSCAN	Receive Buffer Register 9DH*2	RMDF39	16	16	2 or 3 PCLKB
000A 8440h	RSCAN	Receive Rule Entry Register 13BL*2	GAFLML13	16	16	2 or 3 PCLKB
000A 8440h	RSCAN	Receive Buffer Register 10AL*2	RMIDL10	16	16	2 or 3 PCLKB
000A 8442h	RSCAN	Receive Rule Entry Register 13BH*2	GAFLMH13	16	16	2 or 3 PCLKB
000A 8442h	RSCAN	Receive Buffer Register 10AH*2	RMIDH10	16	16	2 or 3 PCLKB
000A 8444h	RSCAN	Receive Rule Entry Register 13CL*2	GAFLPL13	16	16	2 or 3 PCLKB
000A 8444h	RSCAN	Receive Buffer Register 10BL*2	RMTS10	16	16	2 or 3 PCLKB
000A 8446h	RSCAN	Receive Rule Entry Register 13CH*2	GAFLPH13	16	16	2 or 3 PCLKB
000A 8446h	RSCAN	Receive Buffer Register 10BH*2	RMPTR10	16	16	2 or 3 PCLKB
000A 8448h	RSCAN	Receive Rule Entry Register 14AL*2	GAFLIDL14	16	16	2 or 3 PCLKB
000A 8448h	RSCAN	Receive Buffer Register 10CL*2	RMDF010	16	16	2 or 3 PCLKB
000A 844Ah	RSCAN	Receive Rule Entry Register 14AH*2	GAFLIDH14	16	16	2 or 3 PCLKB
000A 844Ah	RSCAN	Receive Buffer Register 10CH*2	RMDF110	16	16	2 or 3 PCLKB
000A 844Ch	RSCAN	Receive Rule Entry Register 14BL*2	GAFLML14	16	16	2 or 3 PCLKB
000A 844Ch	RSCAN	Receive Buffer Register 10DL*2	RMDF210	16	16	2 or 3 PCLKB
000A 844Eh	RSCAN	Receive Rule Entry Register 14BH*2	GAFLMH14	16	16	2 or 3 PCLKB
000A 844Eh	RSCAN	Receive Buffer Register 10DH*2	RMDF310	16	16	2 or 3 PCLKB
000A 8450h	RSCAN	Receive Rule Entry Register 14CL*2	GAFLPL14	16	16	2 or 3 PCLKB
000A 8450h	RSCAN	Receive Buffer Register 11AL*2	RMIDL11	16	16	2 or 3 PCLKB
000A 8452h	RSCAN	Receive Rule Entry Register 14CH*2	GAFLPH14	16	16	2 or 3 PCLKB
000A 8452h	RSCAN	Receive Buffer Register 11AH*2	RMIDH11	16	16	2 or 3 PCLKB
000A 8454h	RSCAN	Receive Rule Entry Register 15AL*2	GAFLIDL15	16	16	2 or 3 PCLKB
000A 8454h	RSCAN	Receive Buffer Register 11BL*2	RMTS11	16	16	2 or 3 PCLKB
000A 8456h	RSCAN	Receive Rule Entry Register 15AH*2	GAFLIDH15	16	16	2 or 3 PCLKB
000A 8456h	RSCAN	Receive Buffer Register 11BH*2	RMPTR11	16	16	2 or 3 PCLKB
000A 8458h	RSCAN	Receive Rule Entry Register 15BL*2	GAFLML15	16	16	2 or 3 PCLKB
000A 8458h	RSCAN	Receive Buffer Register 11CL*2	RMDF011	16	16	2 or 3 PCLKB
000A 845Ah	RSCAN	Receive Rule Entry Register 15BH*2	GAFLMH15	16	16	2 or 3 PCLKB
000A 845Ah	RSCAN	Receive Buffer Register 11CH*2	RMDF111	16	16	2 or 3 PCLKB
000A 845Ch	RSCAN	Receive Rule Entry Register 15CL*2	GAFLPL15	16	16	2 or 3 PCLKB
000A 845Ch	RSCAN	Receive Buffer Register 11DL*2	RMDF211	16	16	2 or 3 PCLKB
000A 845Eh	RSCAN	Receive Rule Entry Register 15CH*2	GAFLPH15	16	16	2 or 3 PCLKB
000A 845Eh	RSCAN	Receive Buffer Register 11DH*2	RMDF311	16	16	2 or 3 PCLKB
000A 8460h	RSCAN	Receive Buffer Register 12AL*2	RMIDL12	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (32/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000C 1A4Dh	MTU7	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA
000C 1A50h	MTU6	Timer Synchronous Clear Register	TSYCR	8	8	4 or 5 PCLKA
000C 1A60h	MTU	Timer Waveform Control Register B	TWCRB	8	8	4 or 5 PCLKA
000C 1A70h	MTU	Timer Mode Register 2B	TMDR2B	8	8	4 or 5 PCLKA
000C 1A72h	MTU6	Timer General Register E	TGRE	16	16	4 or 5 PCLKA
000C 1A74h	MTU7	Timer General Register E	TGRE	16	16	4 or 5 PCLKA
000C 1A76h	MTU7	Timer General Register F	TGRF	16	16	4 or 5 PCLKA
000C 1A80h	MTU	Timer Start Register B	TSTRB	8	8, 16	4 or 5 PCLKA
000C 1A81h	MTU	Timer Synchronous Register B	TSYRB	8	8	4 or 5 PCLKA
000C 1A84h	MTU	Timer Read/Write Enable Register B	TRWERB	8	8	4 or 5 PCLKA
000C 1A93h	MTU6	Noise Filter Control Register 6	NFCR6	8	8	4 or 5 PCLKA
000C 1A94h	MTU7	Noise Filter Control Register 7	NFCR7	8	8	4 or 5 PCLKA
000C 1A95h	MTU5	Noise Filter Control Register 5	NFCR5	8	8	4 or 5 PCLKA
000C 1C80h	MTU5	Timer Counter U	TCNTU	16	16, 32	4 or 5 PCLKA
000C 1C82h	MTU5	Timer General Register U	TGRU	16	16	4 or 5 PCLKA
000C 1C84h	MTU5	Timer Control Register U	TCRU	8	8	4 or 5 PCLKA
000C 1C85h	MTU5	Timer Control Register 2U	TCR2U	8	8	4 or 5 PCLKA
000C 1C86h	MTU5	Timer I/O Control Register U	TIORU	8	8	4 or 5 PCLKA
000C 1C90h	MTU5	Timer Counter V	TCNTV	16	16, 32	4 or 5 PCLKA
000C 1C92h	MTU5	Timer General Register V	TGRV	16	16	4 or 5 PCLKA
000C 1C94h	MTU5	Timer Control Register V	TCRV	8	8	4 or 5 PCLKA
000C 1C95h	MTU5	Timer Control Register 2V	TCR2V	8	8	4 or 5 PCLKA
000C 1C96h	MTU5	Timer I/O Control Register V	TIORV	8	8	4 or 5 PCLKA
000C 1CA0h	MTU5	Timer Counter W	TCNTW	16	16, 32	4 or 5 PCLKA
000C 1CA2h	MTU5	Timer General Register W	TGRW	16	16	4 or 5 PCLKA
000C 1CA4h	MTU5	Timer Control Register W	TCRW	8	8	4 or 5 PCLKA
000C 1CA5h	MTU5	Timer Control Register 2W	TCR2W	8	8	4 or 5 PCLKA
000C 1CA6h	MTU5	Timer I/O Control Register W	TIORW	8	8	4 or 5 PCLKA
000C 1CB2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	4 or 5 PCLKA
000C 1CB4h	MTU5	Timer Start Register	TSTR	8	8	4 or 5 PCLKA
000C 1CB6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	4 or 5 PCLKA
000C 1D30h	MTU	A/D Conversion Start Request Select Register 0	TADSTRGR0	8	8	4 or 5 PCLKA
000C 1D32h	MTU	A/D Conversion Start Request Select Register 1	TADSTRGR1	8	8	4 or 5 PCLKA
000C 2000h	GPT	General PWM Timer Software Start Register*2	GTSTR	16	8, 16, 32	4 or 5 PCLKA
000C 2002h	GPT	Noise Filter Control Register*2	NFCR	16	16, 32	4 or 5 PCLKA
000C 2004h	GPT	General PWM Timer Hardware Source Start/Stop Control Register 0*2	GTHSCR	16	8, 16, 32	4 or 5 PCLKA
000C 2006h	GPT	General PWM Timer Hardware Source Clear Control Register*2	GTHCCR	16	8, 16, 32	4 or 5 PCLKA
000C 2008h	GPT	General PWM Timer Hardware Start Source Select Register*2	GTHSSR	16	8, 16, 32	4 or 5 PCLKA
000C 200Ah	GPT	General PWM Timer Hardware Stop/Clear Source Select Register*2	GTHPSR	16	8, 16, 32	4 or 5 PCLKA
000C 200Ch	GPT	General PWM Timer Write-Protection Register*2	GTWP	16	8, 16, 32	4 or 5 PCLKA
000C 200Eh	GPT	General PWM Timer Sync Register*2	GTSYNC	16	8, 16, 32	4 or 5 PCLKA
000C 2010h	GPT	General PWM Timer External Trigger Input Interrupt Register*2	GTETINT	16	8, 16, 32	4 or 5 PCLKA
000C 2014h	GPT	General PWM Timer Buffer Operation Disable Register*2	GTBDR	16	8, 16, 32	4 or 5 PCLKA
000C 2018h	GPT	General PWM Timer Start Write-Protection Register*2	GTSWP	16	8, 16, 32	4 or 5 PCLKA
000C 201Ch	GPT	General PWM Timer Clearing Write-Protection Register*2	GTCWP	16	8, 16, 32	4 or 5 PCLKA
000C 2020h	GPT	General PWM Timer Common Register Write-Protection Register*2	GTCMNWP	16	8, 16, 32	4 or 5 PCLKA
000C 2024h	GPT	General PWM Timer Mode Register*2	GTMDR	16	8, 16, 32	4 or 5 PCLKA
000C 2028h	GPT	General PWM Timer External Clock Noise Filter Control Register*2	GTECNFCR	32	8, 16, 32	4 or 5 PCLKA

Table 5.10 DC Characteristics (8)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

The ripple voltage must meet the allowable ripple frequency $f_{r\,(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (2.7 V). When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_{r\,(VCC)}$	—	—	10	kHz	Figure 5.5 $V_{r\,(VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 5.5 $V_{r\,(VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 5.5 $V_{r\,(VCC)} \leq VCC \times 0.06$
Allowable voltage change rising/falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

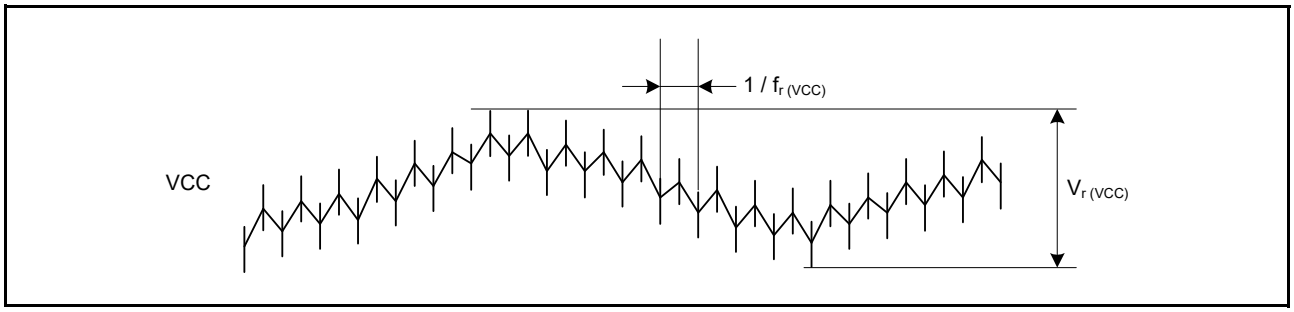


Figure 5.5 Ripple Waveform

Table 5.11 DC Characteristics (9)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Permissible error of VCL pin external capacitance	C_{VCL}	3.3	4.7	6.1	µF	

Note: The recommended capacitance is 4.7 µF. Variations in connected capacitors should be within the above range.

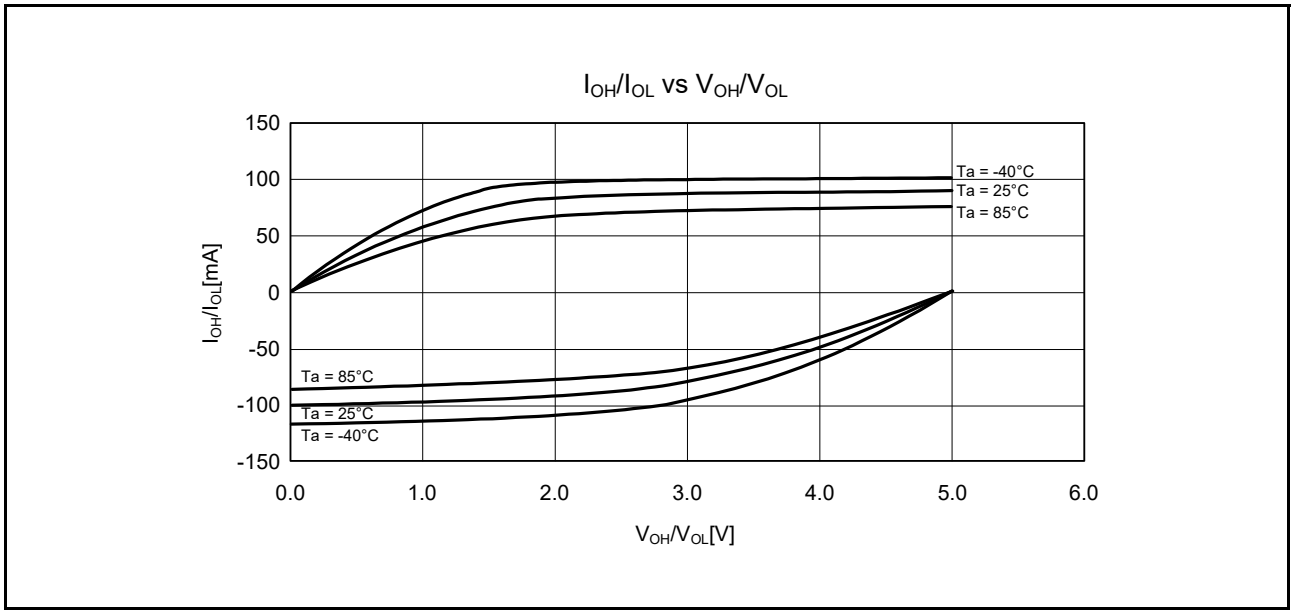


Figure 5.12 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.0 V when Normal Output is Selected (Reference Data)

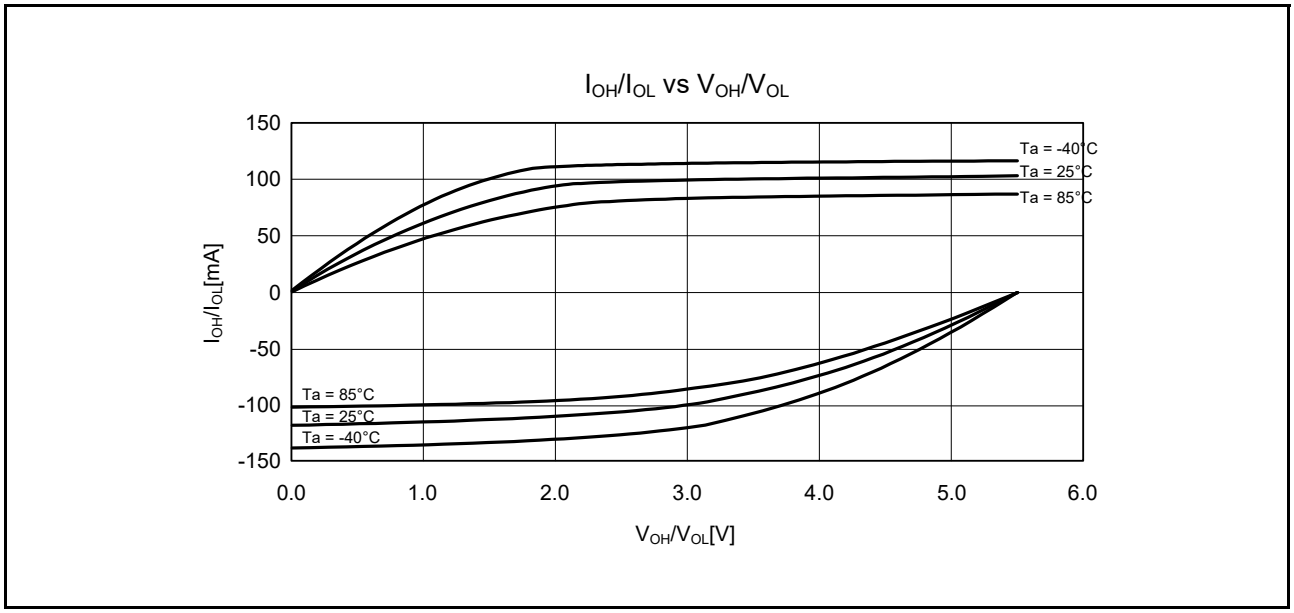


Figure 5.13 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.5 V when Normal Output is Selected (Reference Data)

Table 5.16 Clock Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{Xcyc}	50	—	—	ns	Figure 5.22
EXTAL external clock input high pulse width	t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width	t_{XL}	20	—	—	ns	
EXTAL external clock rise time	t_{Xr}	—	—	5	ns	
EXTAL external clock fall time	t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1	t_{XWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency	f_{MAIN}	1	—	20	MHz	
Main clock oscillation stabilization time (crystal)*2	$t_{MAINOSC}$	—	3	—	ms	Figure 5.23
Main clock oscillation stabilization time (ceramic resonator)*2	$t_{MAINOSC}$	—	50	—	μs	
LOCO clock oscillation frequency	f_{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	0.5	μs	Figure 5.24
HOCO clock oscillation frequency	f_{HOCO} (32MHz)	31.52	32	32.48	MHz	T_a = –40 to –20°C
		31.68	32	32.32	MHz	T_a = –20 to +75°C
		31.52	32	32.48	MHz	T_a = +75 to +85°C
	f_{HOCO} (64MHz)	63.04	64	64.96	MHz	T_a = –40 to –20°C
		63.36	64	64.64	MHz	T_a = –20 to +75°C
		63.04	64	64.96	MHz	T_a = +75 to +85°C
HOCO clock oscillation stabilization time	t_{HOCO} (32MHz)	—	—	37.1	μs	Figure 5.26
	t_{HOCO} (64MHz)	—	—	80.6	μs	Figure 5.26
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time	t_{ILOCO}	—	—	50	μs	Figure 5.27
PLL circuit oscillation frequency	f_{PLL}	40	—	80	MHz	
PLL clock oscillation stabilization time	t_{PLL}	—	—	50	μs	Figure 5.28
PLL free-running oscillation frequency	f_{PLLFR}	—	8	—	MHz	

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.

Note 2. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that is has become 1, and then start using the main clock.

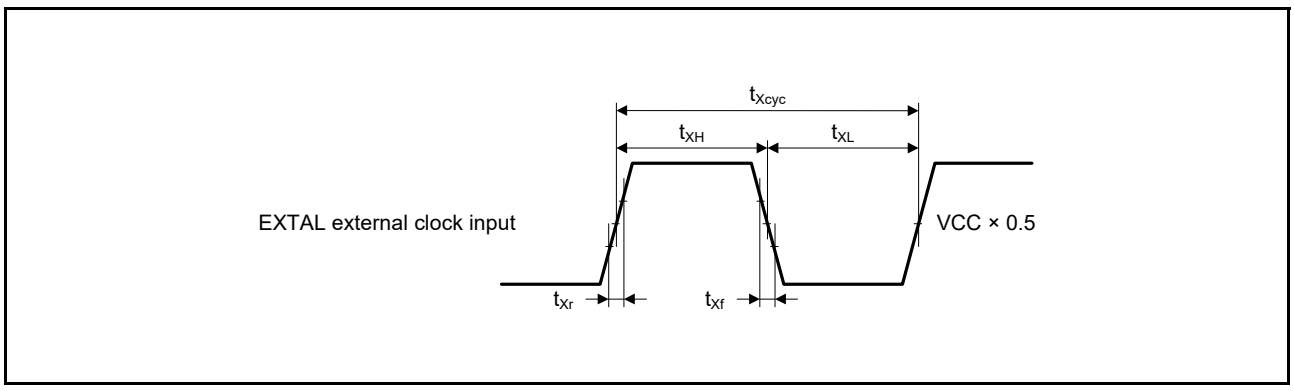


Figure 5.22 EXTAL External Clock Input Timing

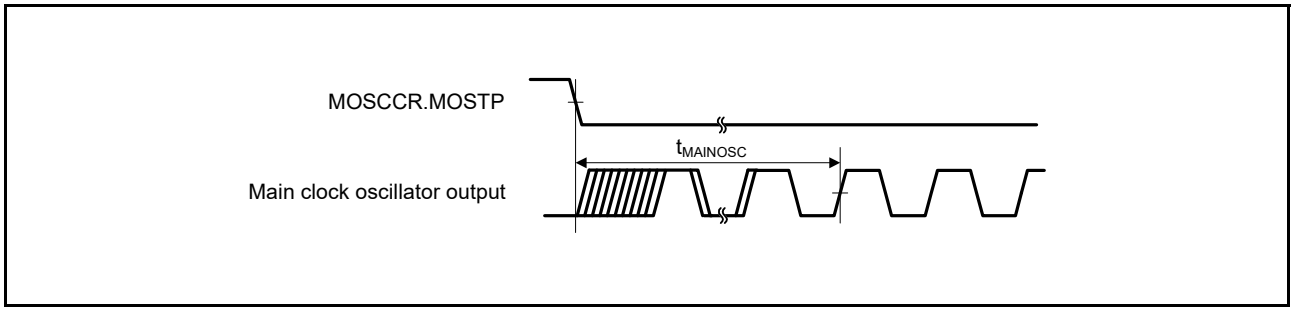


Figure 5.23 Main Clock Oscillation Start Timing

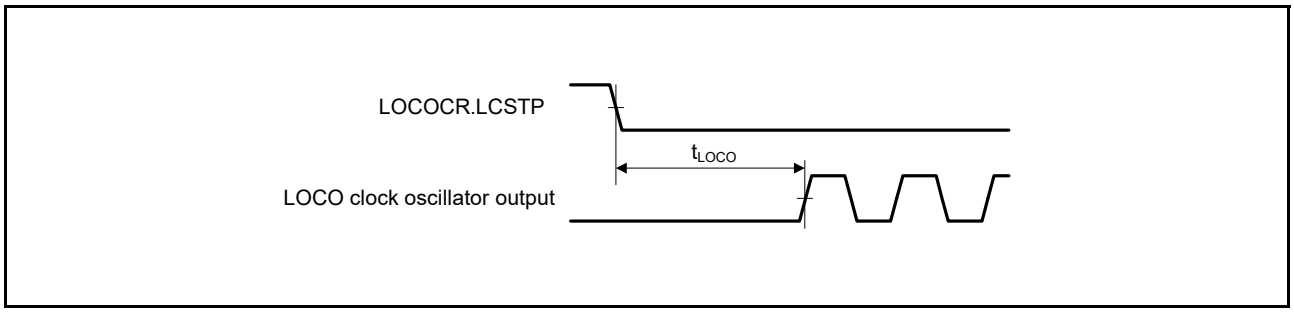


Figure 5.24 LOCO Clock Oscillation Start Timing

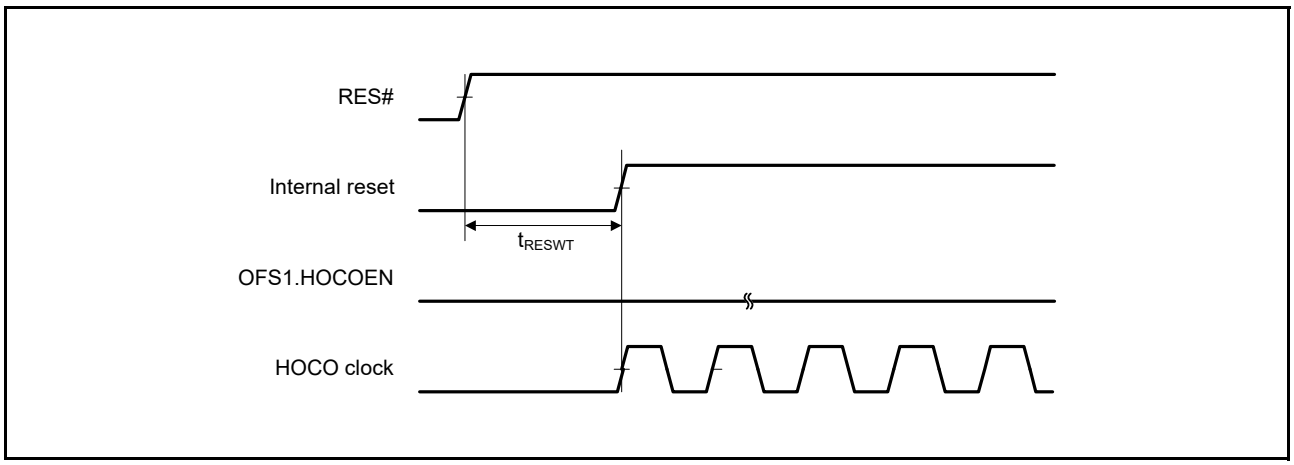


Figure 5.25 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0)

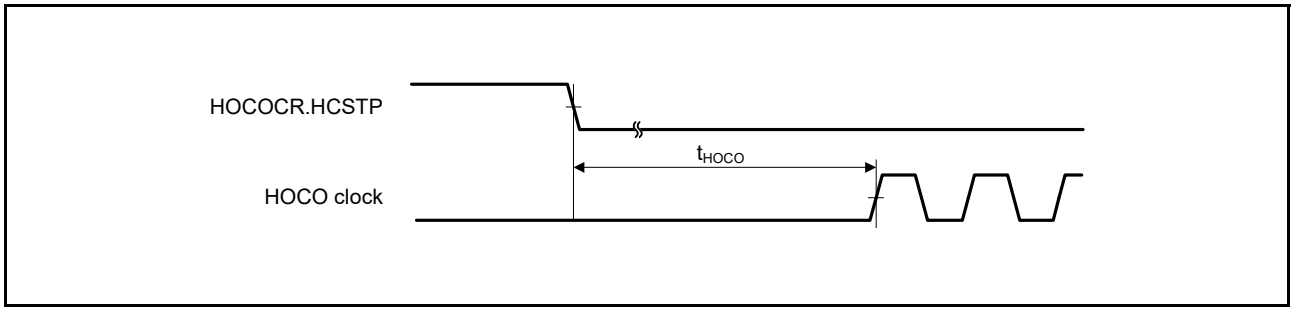


Figure 5.26 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit)

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.18 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	High-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 5.32
			Main clock oscillator and PLL circuit operating*3	t_{SBYPC}	—	2	3	ms	
		External clock input to main clock oscillator	Main clock oscillator operating*4	t_{SBYEX}	—	35	50	µs	
			Main clock oscillator and PLL circuit operating*5	t_{SBYPE}	—	70	95	µs	
		HOCO clock operation	HOCO clock oscillator operation 1*6	t_{SBYHO}	—	40	55	µs	
			HOCO clock oscillator operation 2*7		—	75	90	µs	
			HOCO clock oscillator, PLL circuit operation*8	t_{SBYPH}	—	110	130	µs	
		LOCO clock oscillator operating*9		t_{SBYLO}	—	40	55	µs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.

Note 2. When the frequency of crystal is 20 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 3. When the frequency of PLL is 80 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
When the frequencies of ICLK and PCLKA are set to 80 MHz, PCLKB and PCLKD are set to 40 MHz, and FCLK is set to 20 MHz.

Note 4. When the frequency of the external clock is 20 MHz.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 5. When the frequency of PLL is 80 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.
When the frequencies of ICLK and PCLKA are set to 80 MHz, PCLKB and PCLKD are set to 40 MHz, and FCLK is set to 20 MHz.

Note 6. When the frequency of the high-speed on-chip oscillator is 32 MHz. When the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 05h. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 7. When the frequency of the high-speed on-chip oscillator is 64 MHz. Set the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 06h. When the frequencies of ICLK and PCLKA are set to 64 MHz, and the frequencies of PCLKB, PCLKD, and FCLK are set to 32 MHz.

Note 8. When the frequency of the high-speed on-chip oscillator is 32 MHz, and the frequency of PLL is 80 MHz. When the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 05h. When the frequencies of ICLK and PCLKA are set to 80 MHz, the frequencies of PCLKB and PCLKD are set to 40 MHz, and the frequency of FCLK is set to 20MHz.

Note 9. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

5.3.5 Timing of On-Chip Peripheral Modules

Table 5.23 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item				Symbol	Min.	Max.	Unit *1	Test Conditions
I/O ports	Input data pulse width			t_{PRW}	1.5	—	t_{Pcyc}	Figure 5.36
MTU3	Input capture input pulse width		Single-edge setting	t_{TICW}	3	—	t_{PAcyc}	Figure 5.37
			Both-edge setting		5	—		
	Timer clock pulse width		Single-edge setting	t_{TCKWH}, t_{TCKWL}	3	—	t_{PAcyc}	Figure 5.38
			Both-edge setting		5	—		
			Phase counting mode		5	—		
POE3	POE# input pulse width			t_{POEW}	1.5	—	t_{Pcyc}	Figure 5.39
GPT	Input capture input pulse width		Single-edge setting	t_{GTICW}	1.5	—	t_{PAcyc}	Figure 5.40
			Both-edge setting		2.5	—		
	External trigger input pulse width		Single-edge setting	t_{GTETW}	1.5	—	t_{PAcyc}	Figure 5.41
			Both-edge setting		2.5	—		
	Timer clock pulse width			t_{GTCKWH}	1.5	—	t_{PAcyc}	Figure 5.42
				t_{GTCKWL}				
TMR	Timer clock pulse width		Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{Pcyc}	Figure 5.43
			Both-edge setting		2.5	—		
SCI	Input clock cycle		Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 5.44
			Clock synchronous		6	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle		Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	Figure 5.45
			Clock synchronous		4	—		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time			t_{SCKr}	—	20	ns	
	Output clock fall time			t_{SCKf}	—	20	ns	
	Transmit data delay time (master)	Clock synchronous		t_{TXD}	—	40	ns	
	Transmit data delay time (slave)	Clock synchronous	VCC = 4.0 V or above		—	40	ns	
			VCC = 2.7 V or above		—	65	ns	
	Receive data setup time (master)	Clock synchronous	VCC = 4.0 V or above	t_{RXS}	40	—	ns	
			VCC = 2.7 V or above		65	—	ns	
	Receive data setup time (slave)	Clock synchronous			40	—	ns	
	Receive data hold time	Clock synchronous		t_{RXH}	40	—	ns	
A/D converter	Trigger input pulse width			t_{TRGW}	1.5	—	t_{Pcyc}	Figure 5.46
CAC	CACREF input pulse width		$t_{Pcyc} \le t_{cac}$ *2	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	ns	
			$t_{Pcyc} > t_{cac}$ *2		5 t_{cac} + 6.5 t_{Pcyc}			

Note 1. t_{Pcyc}: PCLK cycle, t_{PAcyc}: PCLKA cycle
Note 2. t_{cac}: CAC count clock source cycle

Table 5.26 Timing of On-Chip Peripheral Modules (4)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Standard mode, SMBus)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 5.52
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t_{STAS}	1000	—	ns	
	STOP condition setup time	t_{STOS}	1000	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast mode)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 5.52
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	300	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t_{STAS}	300	—	ns	
	STOP condition setup time	t_{STOS}	300	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. t_{IICcyc}: RIIC internal reference count clock (IICφ) cycle

Note 2. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

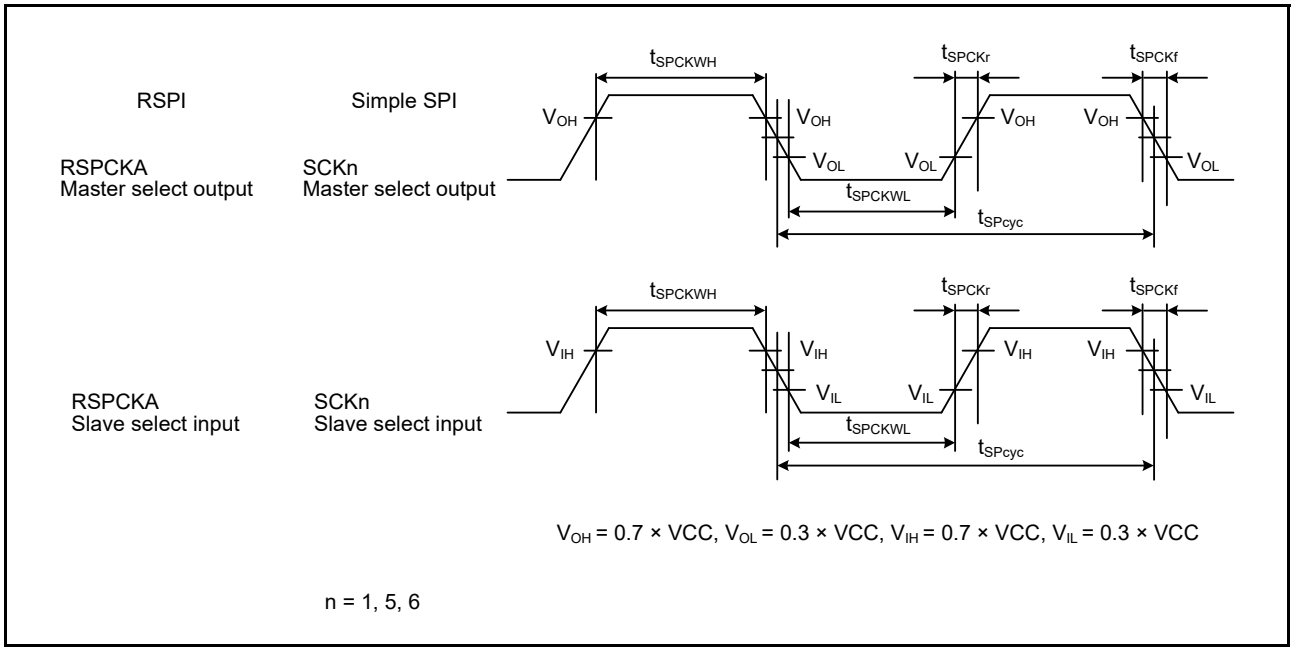


Figure 5.47 RSPI Clock Timing and Simple SPI Clock Timing

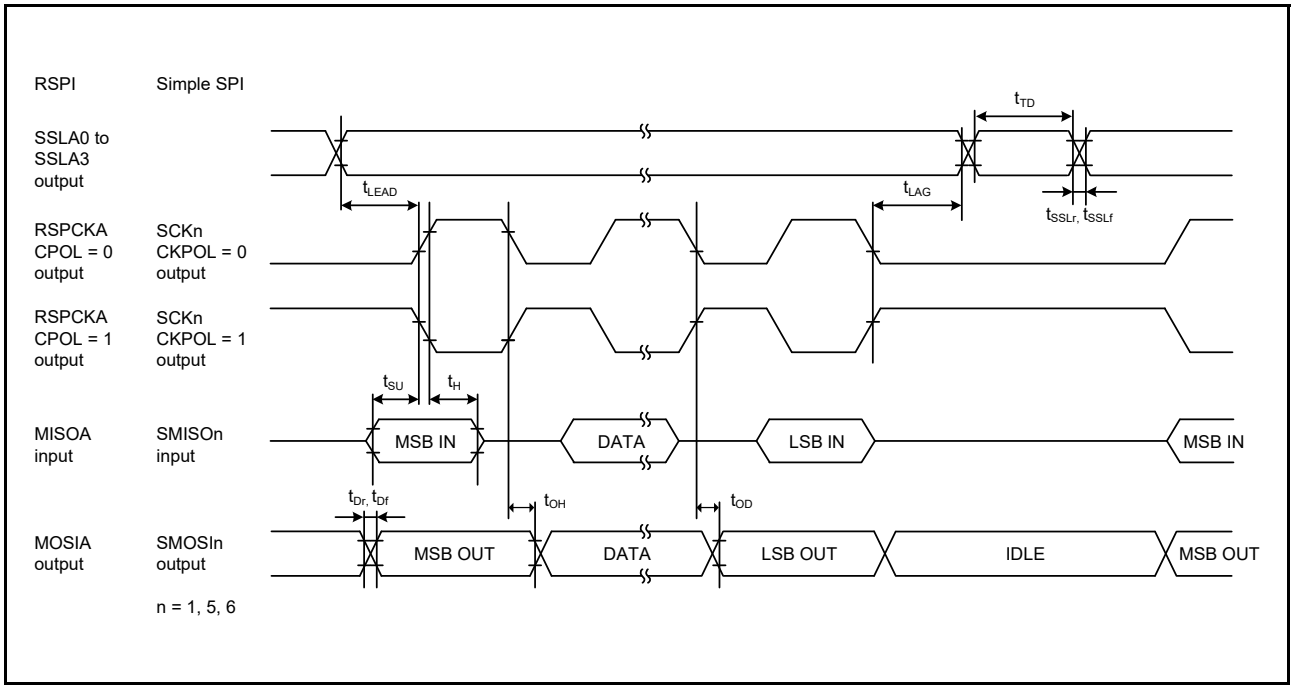


Figure 5.48 RSPI Timing (Master, CPHA = 0) and Simple SPI Clock Timing (Master, CKPH = 1)

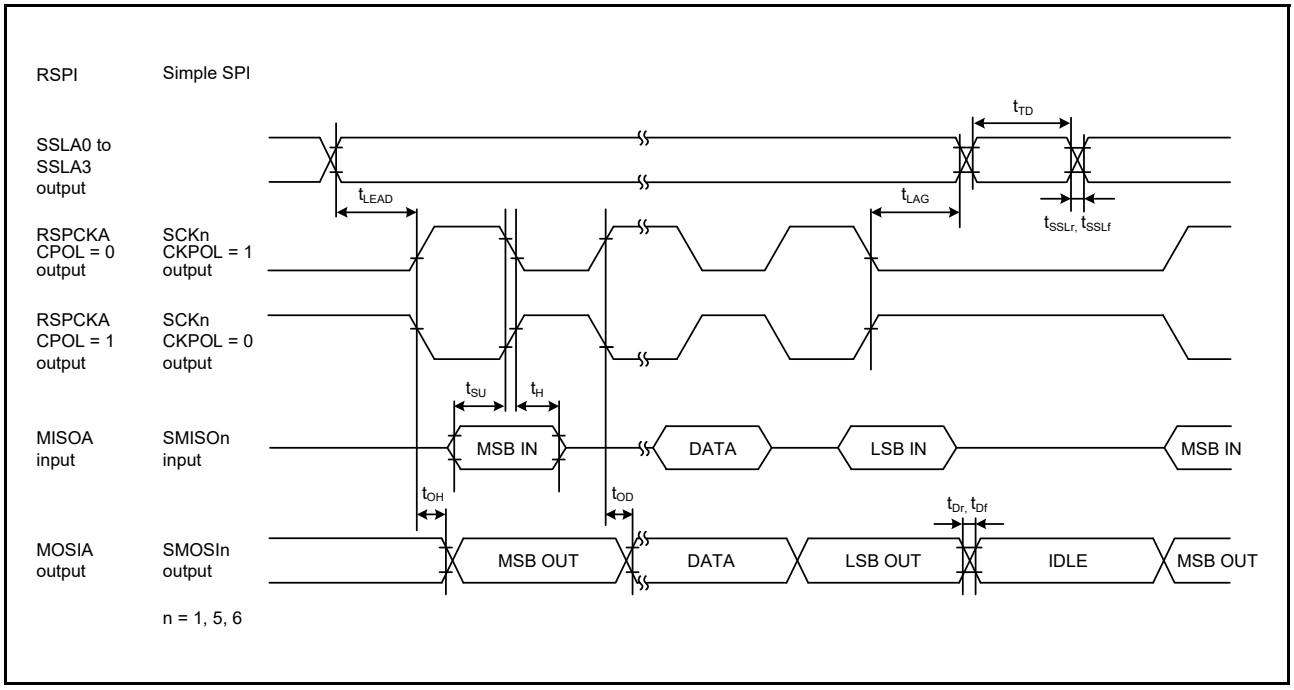


Figure 5.49 RSPI Timing (Master, CPHA = 1) and Simple SPI Clock Timing (Master, CKPH = 0)

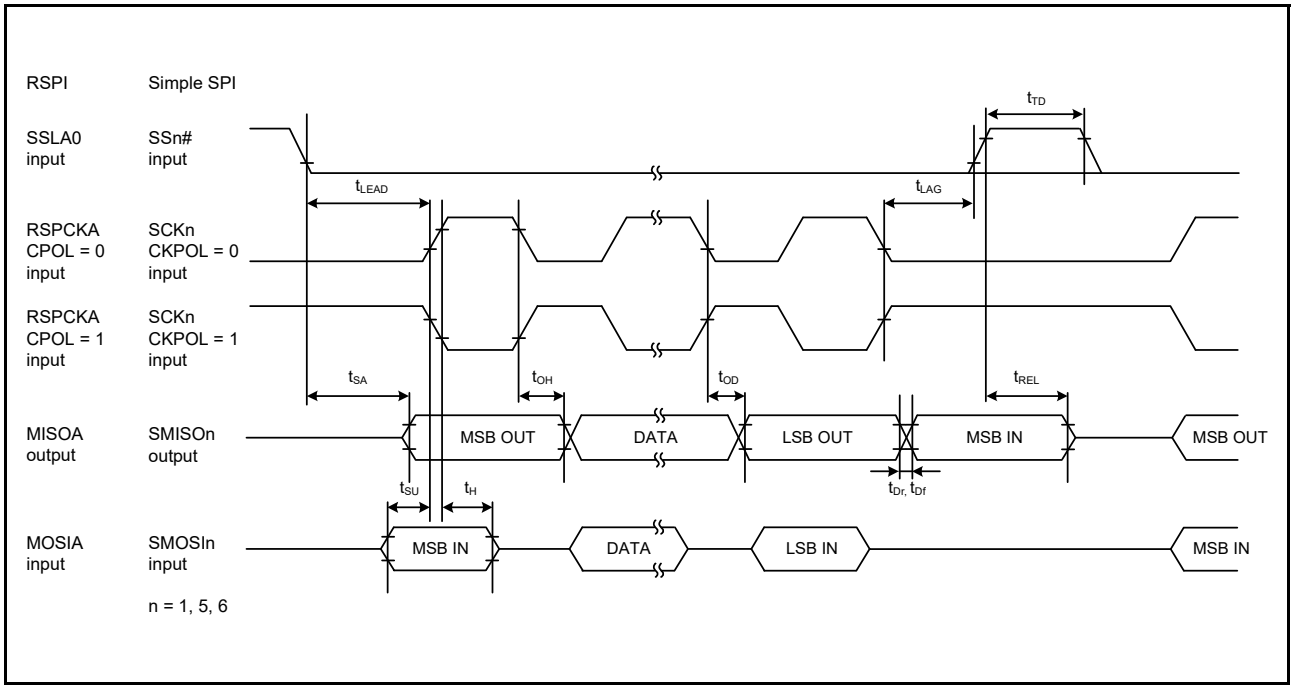


Figure 5.50 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1)

5.4 A/D Conversion Characteristics

Table 5.28 A/D Conversion Characteristics (1)

Conditions: VCC = 4.5 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	40	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 40 MHz)	Permissible signal source impedance (Max.) = 1.0 kΩ Sample-and-hold circuit not in use	1.00	—	—	µs	High-precision channel ADSSTRn.SST[7:0] bits = 08h
		1.25	—	—	µs	Normal-precision channel ADSSTRn.SST[7:0] bits = 12h
	Permissible signal source impedance (Max.) = 1.0 kΩ Sample-and-hold circuit in use	1.65	—	—	µs	High-precision channel ADSSTRn.SST[7:0] bits = 08h ADSHCR.SSTSH[7:0] bits = 0Dh AN100 to 102 = 0.25 V to AVCC1 – 0.25 V
Analog input capacitance		—	—	12	pF	
Offset error		—	±2.0	±6.5	LSB	
Full-scale error		—	±2.0	±6.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy	Sample-and-hold circuit in use	—	±2.5	±8.0	LSB	AN100 to 102 = 0.25V to AVCC1 – 0.25
	Sample-and-hold circuit not in use	—	±3.0	±8.0	LSB	
DNL differential nonlinearity error		—	±0.5	±1.5	LSB	
INL integral nonlinearity error		—	±1.5	±4.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

5.6 Comparator Characteristics

Table 5.33 Comparator Characteristics

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Offset voltage	V_{cioff}	—	—	40	mV	
Reference input voltage range	V_{cref}	0	—	VREF	V	
Response time	t_{cr}	—	—	200	ns	VOD = 100 mV CMPCTL.CDFS = 0
	t_{cf}	—	—	200	ns	
Stabilization wait time for input selection	t_{cwait}	300	—	—	ns	
Operation stabilization wait time	t_{cmp}		—	1	µs	

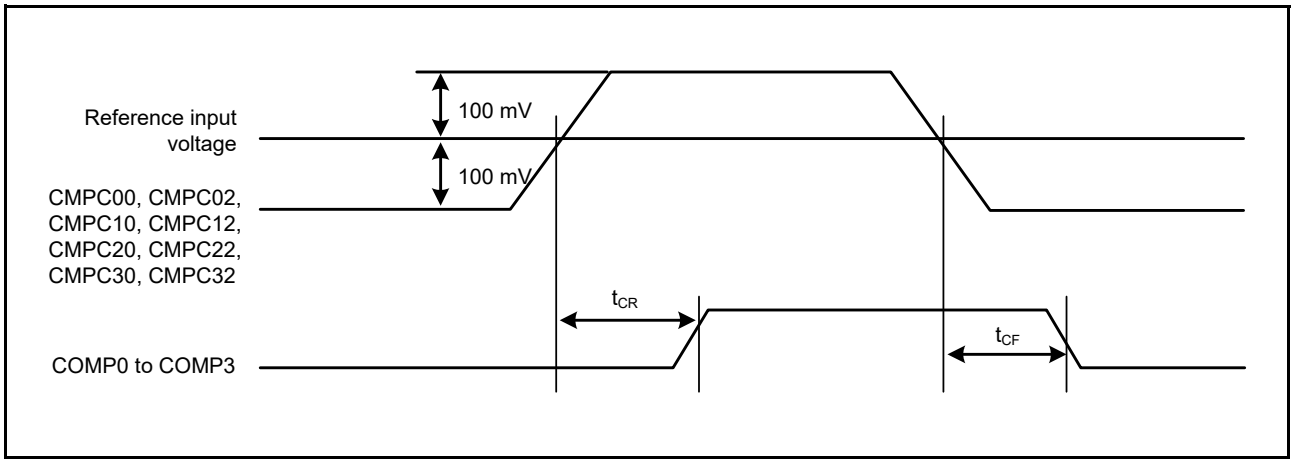


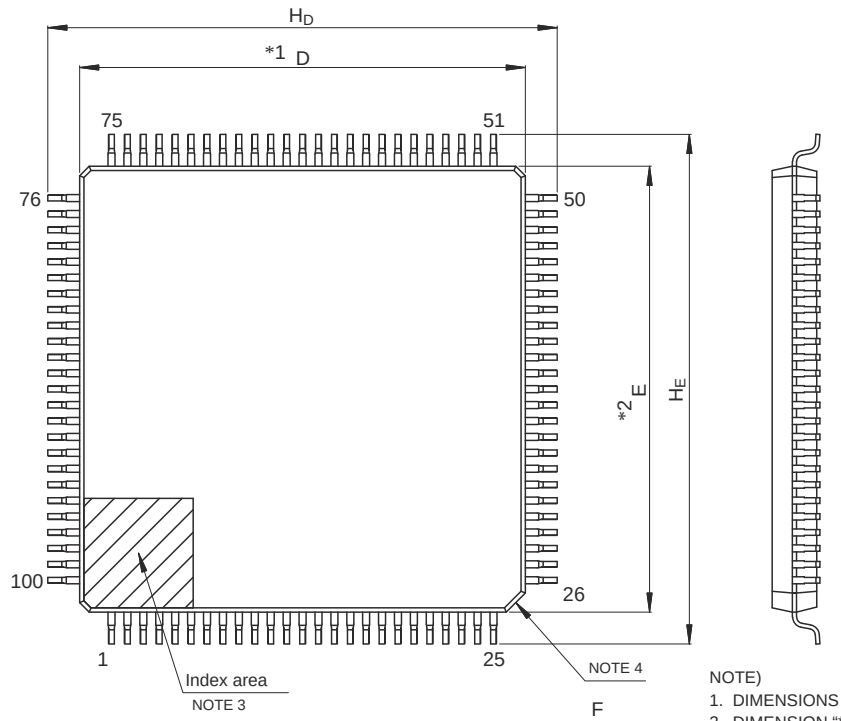
Figure 5.54 Comparator Response Time

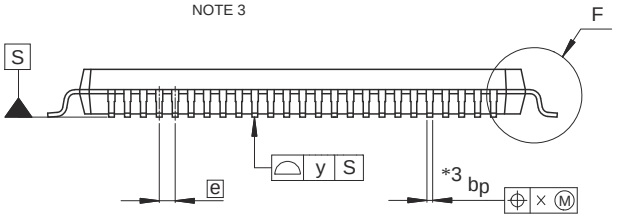
Appendix 1. Package Dimensions

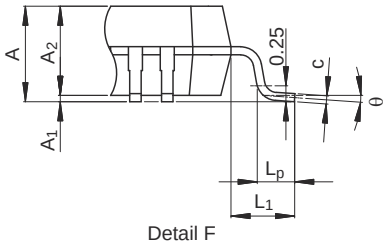
Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm







NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure A 100-Pin LFQFP (PLQP0100KB-B)