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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 17x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f524taadff-31

Table 1.1 Outline of Specifications (4/4)

Classification	Module/Function	Description
12-bit A/D converter (S12ADF)		• 12 bits (5 channels × 2 units/12 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 1.0 µs per channel when the ADCLK is operating at 40 MHz • Operating modes Scan mode (single scan mode, continuous scan mode, and 3 group scan mode) Group A priority control (only for 3 group scan mode) • Sampling variable Sampling time can be set up for each channel • Self-diagnostic function • Double trigger mode (A/D conversion data duplicated) • Assist on analog input disconnection detection • A/D conversion start conditions A software trigger, a trigger from a timer (MTU3, GPT, TMR), or an external trigger signal • Sample-and-hold function Sample-and-hold circuit included (3 channels for unit 1) • Amplification of input signals by a programmable gain amplifier (1 channel for unit 0, 3 channels for unit 1) Amplification rate: 2.0 times, 2.5 times, 3.077 times, 3.636 times, 4.0 times, 4.444 times (total of 6 steps)
Comparator C (CMPC)		• 4 channels • Function to compare the reference voltage and the analog input voltage • Reference voltage: Select from among two voltages • Analog input voltage is selectable from 4 inputs
8-bit D/A converter (DA, DAa)		• DA 1 channel 8-bit resolution Output voltage: 0 V to VREF Dedicated for generating comparator C reference voltage • DAa 2 channels 8-bit resolution Output voltage: 0 V to VREF Can be output externally and used as comparator C reference voltage
Safety	Memory protection unit (MPU)	• Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh. • Minimum protection unit: 16 bytes • Reading from, writing to, and enabling the execution access can be specified for each area. • An address exception occurs when the detected access is not in the permitted area.
	Register write protection function	• Protects important registers from being overwritten for in case a program runs out of control.
	CRC calculator (CRC)	• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
	Main clock oscillation stop function	• Main clock oscillation stop detection: Available
	Clock frequency accuracy measurement circuit (CAC)	• Monitors the clock output from the main clock oscillator, high-speed on-chip oscillator, low-speed on-chip oscillator, the PLL frequency synthesizer, IWDT-dedicated on-chip oscillator, and PCLKB.
	Data operation circuit (DOC)	The function to compare, add, or subtract 16-bit data
Power supply voltages/Operating frequencies		VCC = 2.7 to 5.5 V: 80 MHz
Packages		100-pin LFQFP 0.5 mm pitch 80-pin LQFP 0.65 mm pitch 80-pin LFQFP 0.5 mm pitch 64-pin LFQFP 0.5 mm pitch
On-chip debugging system		E1 emulator (FINE interface)

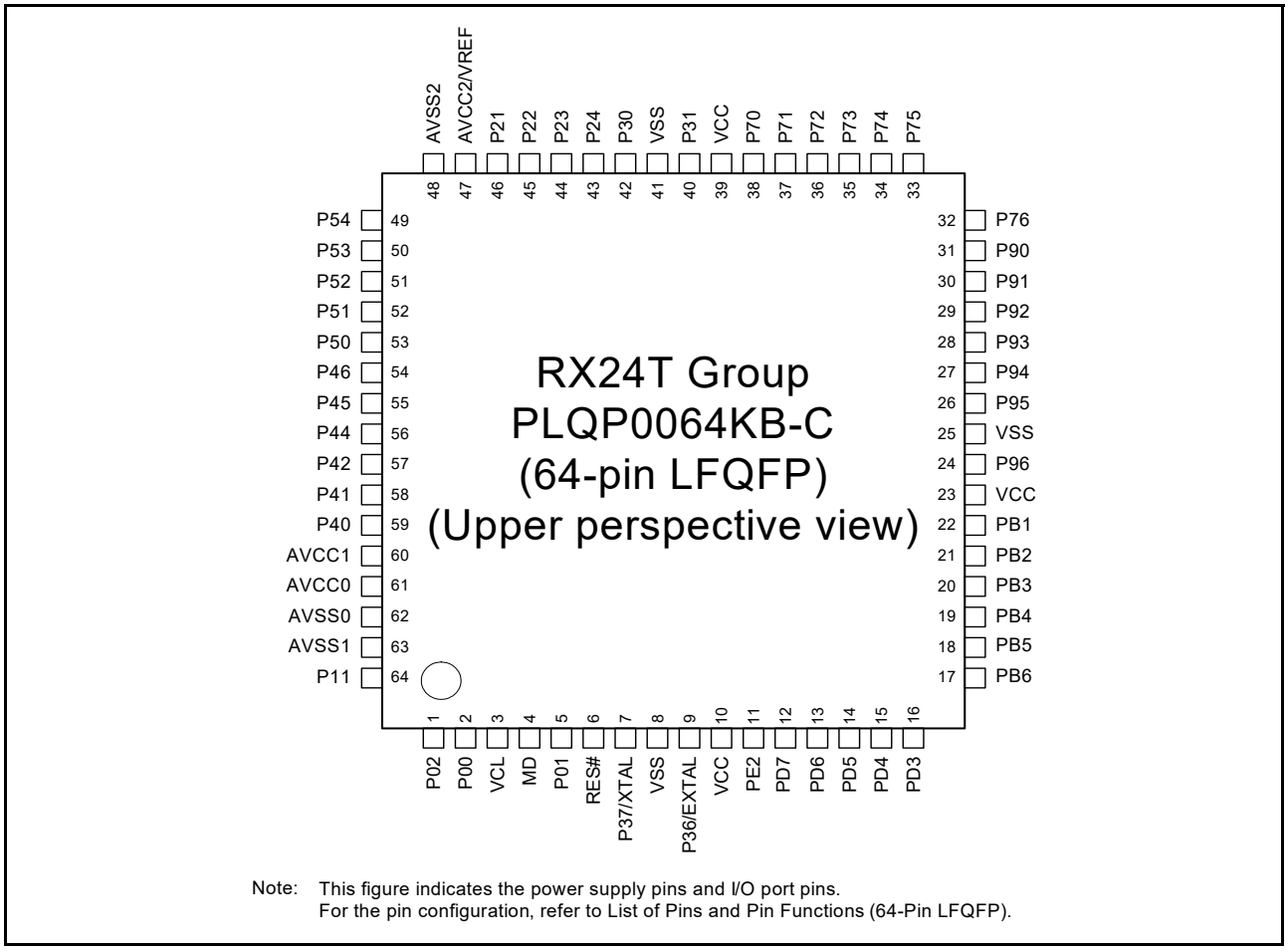
1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products

Group	Part No.	Part No. (for Orders)	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (max.)	Chip Version
RX24T	R5F524TEADFP	R5F524TEADFP#31	PLQP0100KB-B	512 Kbytes	32 Kbytes	8 Kbytes	80 MHz	B
	R5F524TCADFP	R5F524TCADFP#31	PLQP0100KB-B	384 Kbytes				
	R5F524TBADFP	R5F524TBADFP#31	PLQP0100KB-B	256 Kbytes				
	R5F524TAADFP	R5F524TAADFP#31	PLQP0100KB-B	256 Kbytes	16 Kbytes	8 Kbytes	80 MHz	A
	R5F524TAADFF	R5F524TAADFF#31	PLQP0080JA-A					
	R5F524TAADFN	R5F524TAADFN#31	PLQP0080KB-B					
	R5F524TAADFM	R5F524TAADFM#31	PLQP0064KB-C					
	R5F524T8ADFP	R5F524T8ADFP#31	PLQP0100KB-B	128 Kbytes				
	R5F524T8ADFF	R5F524T8ADFF#31	PLQP0080JA-A					
	R5F524T8ADFN	R5F524T8ADFN#31	PLQP0080KB-B					
	R5F524T8ADFM	R5F524T8ADFM#31	PLQP0064KB-C					

Note: The part numbers for orders above are used for products in mass production or under development when this manual is issued. Refer to the Renesas Electronics Corporation website for the latest part numbers.



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, refer to List of Pins and Pin Functions (64-Pin LFQFP).

Figure 1.6 Pin Assignments of the 64-Pin LFQFP

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version B) (2/3)

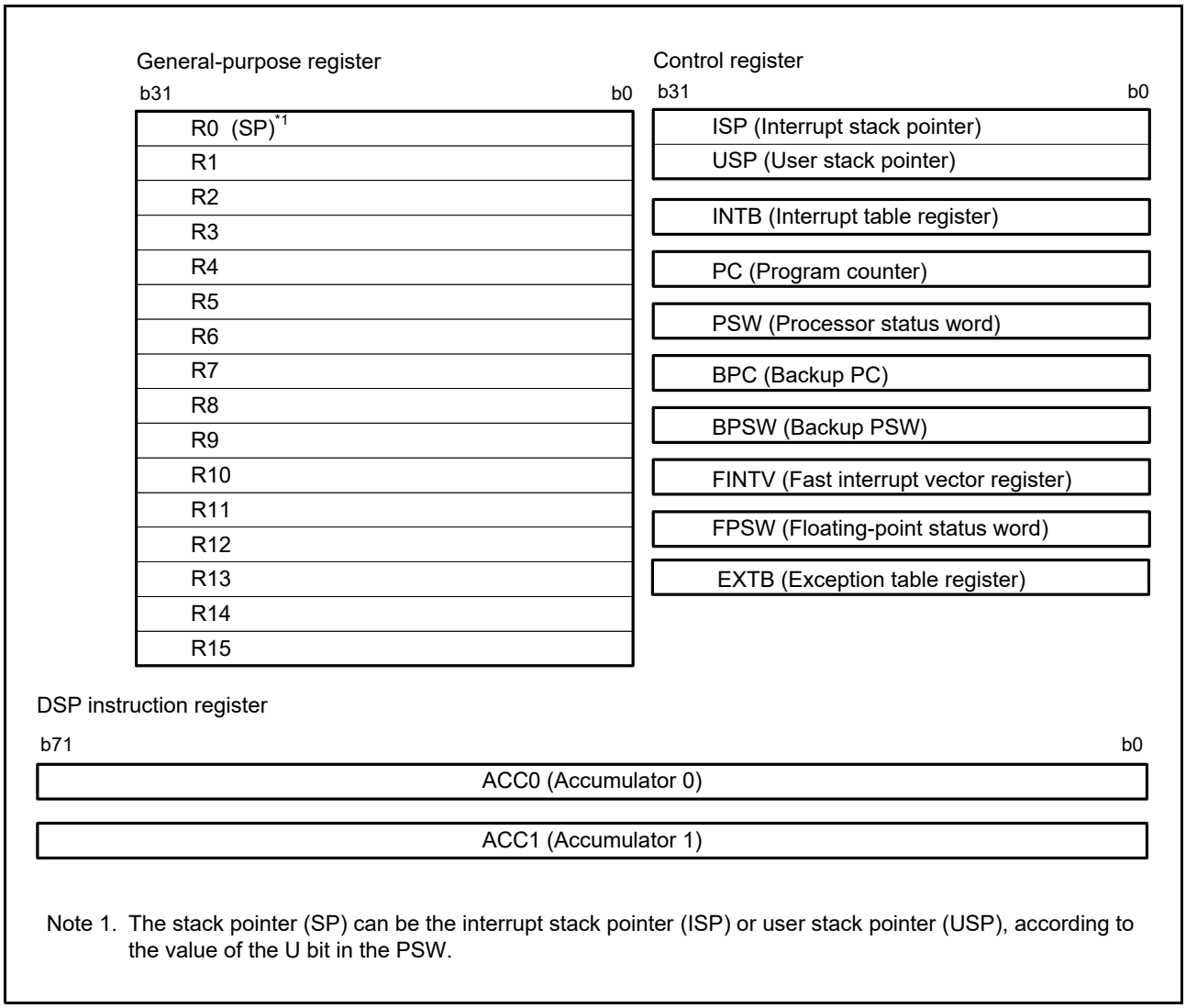
Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
52		P75	MTIOC4C, MTIOC4C#, GTIOC1B, GTIOC1B#		
53		P74	MTIOC3D, MTIOC3D#, GTIOC0B, GTIOC0B#		
54		P73	MTIOC4B, MTIOC4B#, GTIOC2A, GTIOC2A#		
55		P72	MTIOC4A, MTIOC4A#, GTIOC1A, GTIOC1A#		
56		P71	MTIOC3B, MTIOC3B#, GTIOC0A, GTIOC0A#		
57		P70	POE0#		IRQ5
58		P33	MTIOC3A, MTIOC3A#, MTCLKA, MTCLKA#, TMO0	SSLA3	
59		P32	MTIOC3C, MTIOC3C#, MTCLKB, MTCLKB#, TMO6	SSLA2	
60	VCC				
61		P31	MTIOC0A, MTIOC0A#, MTCLKC, MTCLKC#, TMRI6	SSLA1	IRQ6
62	VSS				
63		P30	MTIOC0B, MTIOC0B#, MTCLKD, MTCLKD#, TMCI6	SSLA0	IRQ7, COMP3
64		P24	MTIC5U, MTIC5U#, TMCI2, TMO6	RSPCKA	COMP0, DA0
65		P23	MTIC5V, MTIC5V#, TMO2, CACREF	MOSIA	COMP1, DA1
66		P22	MTIC5W, MTIC5W#, TMRI2, TMO4	MISOA	ADTRG2#, COMP2
67		P21	MTCLKA, MTCLKA#, MTIOC9A, MTIOC9A#, TMCI4		IRQ6, ADTRG1#, AN116
68		P20	MTCLKB, MTCLKB#, MTIOC9C, MTIOC9C#, TMRI4		IRQ7, ADTRG0#, AN016
69		P65			AN205
70		P64			AN204
71	AVCC2				
72	VREF				
73	AVSS2				
74		P63			AN203, IRQ7
75		P62			AN202, IRQ6
76		P61			AN201, IRQ5
77		P60			AN200, IRQ4
78		P55			AN211, IRQ3
79		P54			AN210, IRQ2
80		P53			AN209, IRQ1
81		P52			AN208, IRQ0
82		P51			AN207
83		P50			AN206
84		P47			AN103
85		P46			AN102, CMPC12, CMPC13, CMPC30, CMPC31
86		P45			AN101, CMPC02, CMPC03, CMPC20, CMPC21
87		P44			AN100, CMPC10, CMPC11, CMPC32, CMPC33
88		P43			AN003
89		P42			AN002
90		P41			AN001
91		P40			AN000, CMPC00, CMPC01, CMPC22, CMPC23
92	AVCC1				
93	AVCC0				

Table 1.6 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version A) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, CAC)	Communications (SCI, RSPI, RIIC)	Others
55		P72	MTIOC4A		
56		P71	MTIOC3B		
57		P70	POE0#		IRQ5
58		P33	MTIOC3A, MTCLKA, TMO0	SSLA3	
59		P32	MTIOC3C, MTCLKB, TMO6	SSLA2	
60	VCC				
61		P31	MTIOC0A, MTCLKC, TMRI6	SSLA1	IRQ6
62	VSS				
63		P30	MTIOC0B, MTCLKD, TMCI6	SSLA0	IRQ7, COMP3
64		P24	MTIC5U, TMCI2, TMO6	RSPCKA	COMP0
65		P23	MTIC5V, TMO2, CACREF	MOSIA	COMP1
66		P22	MTIC5W, TMRI2, TMO4	MISOA	ADTRG2#, COMP2
67		P21	MTCLKA, MTIOC9A, TMCI4		IRQ6, ADTRG1#, AN116, CVREFC1
68		P20	MTCLKB, MTIOC9C, TMRI4		IRQ7, ADTRG0#, AN016, CVREFC0
69		P65			AN205
70		P64			AN204
71	AVCC2				
72	VREF				
73	AVSS2				
74		P63			AN203, IRQ7
75		P62			AN202, IRQ6
76		P61			AN201, IRQ5
77		P60			AN200, IRQ4
78		P55			AN211, IRQ3
79		P54			AN210, IRQ2
80		P53			AN209, IRQ1
81		P52			AN208, IRQ0
82		P51			AN207
83		P50			AN206
84		P47			AN103
85		P46			AN102, CMPC12, CMPC13, CMPC30, CMPC31
86		P45			AN101, CMPC02, CMPC03, CMPC20, CMPC21
87		P44			AN100, CMPC10, CMPC11, CMPC32, CMPC33
88		P43			AN003
89		P42			AN002
90		P41			AN001
91		P40			AN000, CMPC00, CMPC01, CMPC22, CMPC23
92	AVCC1				
93	AVCC0				
94	AVSS0				
95	AVSS1				
96		P82	MTIC5U, TMO4	SCK6	
97		P81	MTIC5V, TMCI4	TXD6, SMOSI6, SSDA6	
98		P80	MTIC5W, TMRI4	RXD6, SMISO6, SSCL6	
99		P11	MTIOC3A, MTCLKC, TMO3		IRQ1
100		P10	MTIOC9B, MTCLKD, TMRI3, POE12#	CTS6#, RTS6#, SS6#	IRQ0

2. CPU

Figure 2.1 shows register set of the CPU.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW.

Figure 2.1 Register Set of the CPU

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps.

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For numbers of clock cycles for access to I/O registers, see Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral bus 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 are accessed, the number of divided clock synchronization cycles is added.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the bus access from the different bus master (DTC).

(4) Restrictions in Relation to RMPA and String-Manipulation Instructions

The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

(5) Notes on Sleep Mode and Mode Transitions

During sleep mode or mode transitions, do not write to the system control related registers (indicated by ‘SYSTEM’ in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK
0008 0031h	SYSTEM	Memory Wait Cycle Setting Register	MEMWAIT	8	8	3 ICLK
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK
0008 0036h	SYSTEM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3 ICLK
0008 0037h	SYSTEM	High-Speed On-Chip Oscillator Control Register 2	HOCOCR2	8	8	3 ICLK
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK
0008 00A5h	SYSTEM	High-Speed On-Chip Oscillator Wait Control Register	HOCOWTCR	8	8	3 ICLK
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK
0008 1000h	FLASH	ROM Cache Enable Register	ROMCE	16	16	3 ICLK
0008 1004h	FLASH	ROM Cache Invalidate Register	ROMCIV	16	16	3 ICLK
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2 ICLK
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2 ICLK
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK

Table 4.1 List of I/O Registers (Address Order) (2/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32	1 ICLK
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32	1 ICLK
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32	1 ICLK
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32	1 ICLK
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32	1 ICLK
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32	1 ICLK
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32	1 ICLK
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32	1 ICLK
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32	1 ICLK
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32	1 ICLK
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32	1 ICLK
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32	1 ICLK
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32	1 ICLK
0008 6520h	MPU	Region Search Address Register	MPSA	32	32	1 ICLK
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16	1 ICLK
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16	1 ICLK
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32	1 ICLK
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32	1 ICLK
0008 7010h	ICU	Interrupt Request Register 016	IR016	8	8	2 ICLK
0008 7017h	ICU	Interrupt Request Register 023	IR023	8	8	2 ICLK
0008 701Bh	ICU	Interrupt Request Register 027	IR027	8	8	2 ICLK
0008 701Ch	ICU	Interrupt Request Register 028	IR028	8	8	2 ICLK
0008 701Dh	ICU	Interrupt Request Register 029	IR029	8	8	2 ICLK
0008 701Eh	ICU	Interrupt Request Register 030	IR030	8	8	2 ICLK
0008 701Fh	ICU	Interrupt Request Register 031	IR031	8	8	2 ICLK
0008 7020h	ICU	Interrupt Request Register 032	IR032	8	8	2 ICLK
0008 7021h	ICU	Interrupt Request Register 033	IR033	8	8	2 ICLK
0008 7022h	ICU	Interrupt Request Register 034	IR034	8	8	2 ICLK
0008 7028h	ICU	Interrupt Request Register 040*2	IR040	8	8	2 ICLK
0008 7029h	ICU	Interrupt Request Register 041*2	IR041	8	8	2 ICLK
0008 702Ch	ICU	Interrupt Request Register 044	IR044	8	8	2 ICLK
0008 702Dh	ICU	Interrupt Request Register 045	IR045	8	8	2 ICLK
0008 702Eh	ICU	Interrupt Request Register 046	IR046	8	8	2 ICLK
0008 702Fh	ICU	Interrupt Request Register 047	IR047	8	8	2 ICLK
0008 7030h	ICU	Interrupt Request Register 048*2	IR048	8	8	2 ICLK
0008 7031h	ICU	Interrupt Request Register 049*2	IR049	8	8	2 ICLK
0008 7032h	ICU	Interrupt Request Register 050*2	IR050	8	8	2 ICLK
0008 7033h	ICU	Interrupt Request Register 051*2	IR051	8	8	2 ICLK
0008 7034h	ICU	Interrupt Request Register 052*2	IR052	8	8	2 ICLK
0008 7035h	ICU	Interrupt Request Register 053*2	IR053	8	8	2 ICLK
0008 7036h	ICU	Interrupt Request Register 054*2	IR054	8	8	2 ICLK
0008 7037h	ICU	Interrupt Request Register 055*2	IR055	8	8	2 ICLK
0008 7038h	ICU	Interrupt Request Register 056*2	IR056	8	8	2 ICLK
0008 7039h	ICU	Interrupt Request Register 057	IR057	8	8	2 ICLK
0008 703Bh	ICU	Interrupt Request Register 059*2	IR059	8	8	2 ICLK
0008 703Ch	ICU	Interrupt Request Register 060*2	IR060	8	8	2 ICLK
0008 703Dh	ICU	Interrupt Request Register 061*2	IR061	8	8	2 ICLK
0008 703Eh	ICU	Interrupt Request Register 062*2	IR062	8	8	2 ICLK
0008 703Fh	ICU	Interrupt Request Register 063*2	IR063	8	8	2 ICLK
0008 7040h	ICU	Interrupt Request Register 064	IR064	8	8	2 ICLK
0008 7041h	ICU	Interrupt Request Register 065	IR065	8	8	2 ICLK
0008 7042h	ICU	Interrupt Request Register 066	IR066	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (7/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 71A1h	ICU	DTC Transfer Request Enable Register 161	DTCER161	8	8	2 ICLK
0008 71A2h	ICU	DTC Transfer Request Enable Register 162	DTCER162	8	8	2 ICLK
0008 71ADh	ICU	DTC Transfer Request Enable Register 173	DTCER173	8	8	2 ICLK
0008 71AEh	ICU	DTC Transfer Request Enable Register 174	DTCER174	8	8	2 ICLK
0008 71AFh	ICU	DTC Transfer Request Enable Register 175	DTCER175	8	8	2 ICLK
0008 71B1h	ICU	DTC Transfer Request Enable Register 177	DTCER177	8	8	2 ICLK
0008 71B2h	ICU	DTC Transfer Request Enable Register 178	DTCER178	8	8	2 ICLK
0008 71B4h	ICU	DTC Transfer Request Enable Register 180	DTCER180	8	8	2 ICLK
0008 71B5h	ICU	DTC Transfer Request Enable Register 181	DTCER181	8	8	2 ICLK
0008 71B7h	ICU	DTC Transfer Request Enable Register 183	DTCER183	8	8	2 ICLK
0008 71B8h	ICU	DTC Transfer Request Enable Register 184	DTCER184	8	8	2 ICLK
0008 71BAh	ICU	DTC Transfer Request Enable Register 186	DTCER186	8	8	2 ICLK
0008 71BBh	ICU	DTC Transfer Request Enable Register 187	DTCER187	8	8	2 ICLK
0008 71BDh	ICU	DTC Transfer Request Enable Register 189	DTCER189	8	8	2 ICLK
0008 71BEh	ICU	DTC Transfer Request Enable Register 190	DTCER190	8	8	2 ICLK
0008 71C0h	ICU	DTC Transfer Request Enable Register 192	DTCER192	8	8	2 ICLK
0008 71C1h	ICU	DTC Transfer Request Enable Register 193	DTCER193	8	8	2 ICLK
0008 71C3h	ICU	DTC Transfer Request Enable Register 195	DTCER195	8	8	2 ICLK
0008 71C4h	ICU	DTC Transfer Request Enable Register 196	DTCER196	8	8	2 ICLK
0008 71CBh	ICU	DTC Transfer Request Enable Register 203*2	DTCER203	8	8	2 ICLK
0008 71CCh	ICU	DTC Transfer Request Enable Register 204*2	DTCER204	8	8	2 ICLK
0008 71CDh	ICU	DTC Transfer Request Enable Register 205*2	DTCER205	8	8	2 ICLK
0008 71CEh	ICU	DTC Transfer Request Enable Register 206*2	DTCER206	8	8	2 ICLK
0008 71CFh	ICU	DTC Transfer Request Enable Register 207*2	DTCER207	8	8	2 ICLK
0008 71D0h	ICU	DTC Transfer Request Enable Register 208*2	DTCER208	8	8	2 ICLK
0008 71D1h	ICU	DTC Transfer Request Enable Register 209*2	DTCER209	8	8	2 ICLK
0008 71D2h	ICU	DTC Transfer Request Enable Register 210*2	DTCER210	8	8	2 ICLK
0008 71D4h	ICU	DTC Transfer Request Enable Register 212*2	DTCER212	8	8	2 ICLK
0008 71D5h	ICU	DTC Transfer Request Enable Register 213*2	DTCER213	8	8	2 ICLK
0008 71D6h	ICU	DTC Transfer Request Enable Register 214*2	DTCER214	8	8	2 ICLK
0008 71D7h	ICU	DTC Transfer Request Enable Register 215*2	DTCER215	8	8	2 ICLK
0008 71D8h	ICU	DTC Transfer Request Enable Register 216*2	DTCER216	8	8	2 ICLK
0008 71D9h	ICU	DTC Transfer Request Enable Register 217*2	DTCER217	8	8	2 ICLK
0008 71DBh	ICU	DTC Transfer Request Enable Register 219	DTCER219	8	8	2 ICLK
0008 71DCh	ICU	DTC Transfer Request Enable Register 220	DTCER220	8	8	2 ICLK
0008 71DFh	ICU	DTC Transfer Request Enable Register 223	DTCER223	8	8	2 ICLK
0008 71E0h	ICU	DTC Transfer Request Enable Register 224	DTCER224	8	8	2 ICLK
0008 71E3h	ICU	DTC Transfer Request Enable Register 227	DTCER227	8	8	2 ICLK
0008 71E4h	ICU	DTC Transfer Request Enable Register 228	DTCER228	8	8	2 ICLK
0008 71EEh	ICU	DTC Transfer Request Enable Register 238*2	DTCER238	8	8	2 ICLK
0008 71EFh	ICU	DTC Transfer Request Enable Register 239*2	DTCER239	8	8	2 ICLK
0008 71F1h	ICU	DTC Transfer Request Enable Register 241*2	DTCER241	8	8	2 ICLK
0008 71F2h	ICU	DTC Transfer Request Enable Register 242*2	DTCER242	8	8	2 ICLK
0008 71F3h	ICU	DTC Transfer Request Enable Register 243*2	DTCER243	8	8	2 ICLK
0008 71F4h	ICU	DTC Transfer Request Enable Register 244*2	DTCER244	8	8	2 ICLK
0008 71F7h	ICU	DTC Transfer Request Enable Register 247	DTCER247	8	8	2 ICLK
0008 71F8h	ICU	DTC Transfer Request Enable Register 248	DTCER248	8	8	2 ICLK
0008 7202h	ICU	Interrupt Request Enable Register 02	IER02	8	8	2 ICLK
0008 7203h	ICU	Interrupt Request Enable Register 03	IER03	8	8	2 ICLK
0008 7204h	ICU	Interrupt Request Enable Register 04	IER04	8	8	2 ICLK
0008 7205h	ICU	Interrupt Request Enable Register 05	IER05	8	8	2 ICLK
0008 7206h	ICU	Interrupt Request Enable Register 06*2	IER06	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (26/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
000A 8462h	RSCAN	Receive Buffer Register 12AH*2	RMIDH12	16	16	2 or 3 PCLKB
000A 8464h	RSCAN	Receive Buffer Register 12BL*2	RMTS12	16	16	2 or 3 PCLKB
000A 8466h	RSCAN	Receive Buffer Register 12BH*2	RMPTR12	16	16	2 or 3 PCLKB
000A 8468h	RSCAN	Receive Buffer Register 12CL*2	RMDF012	16	16	2 or 3 PCLKB
000A 846Ah	RSCAN	Receive Buffer Register 12CH*2	RMDF112	16	16	2 or 3 PCLKB
000A 846Ch	RSCAN	Receive Buffer Register 12DL*2	RMDF212	16	16	2 or 3 PCLKB
000A 846Eh	RSCAN	Receive Buffer Register 12DH*2	RMDF312	16	16	2 or 3 PCLKB
000A 8470h	RSCAN	Receive Buffer Register 13AL*2	RMIDL13	16	16	2 or 3 PCLKB
000A 8472h	RSCAN	Receive Buffer Register 13AH*2	RMIDH13	16	16	2 or 3 PCLKB
000A 8474h	RSCAN	Receive Buffer Register 13BL*2	RMTS13	16	16	2 or 3 PCLKB
000A 8476h	RSCAN	Receive Buffer Register 13BH*2	RMPTR13	16	16	2 or 3 PCLKB
000A 8478h	RSCAN	Receive Buffer Register 13CL*2	RMDF013	16	16	2 or 3 PCLKB
000A 847Ah	RSCAN	Receive Buffer Register 13CH*2	RMDF113	16	16	2 or 3 PCLKB
000A 847Ch	RSCAN	Receive Buffer Register 13DL*2	RMDF213	16	16	2 or 3 PCLKB
000A 847Eh	RSCAN	Receive Buffer Register 13DH*2	RMDF313	16	16	2 or 3 PCLKB
000A 8480h	RSCAN	Receive Buffer Register 14AL*2	RMIDL14	16	16	2 or 3 PCLKB
000A 8482h	RSCAN	Receive Buffer Register 14AH*2	RMIDH14	16	16	2 or 3 PCLKB
000A 8484h	RSCAN	Receive Buffer Register 14BL*2	RMTS14	16	16	2 or 3 PCLKB
000A 8486h	RSCAN	Receive Buffer Register 14BH*2	RMPTR14	16	16	2 or 3 PCLKB
000A 8488h	RSCAN	Receive Buffer Register 14CL*2	RMDF014	16	16	2 or 3 PCLKB
000A 848Ah	RSCAN	Receive Buffer Register 14CH*2	RMDF114	16	16	2 or 3 PCLKB
000A 848Ch	RSCAN	Receive Buffer Register 14DL*2	RMDF214	16	16	2 or 3 PCLKB
000A 848Eh	RSCAN	Receive Buffer Register 14DH*2	RMDF314	16	16	2 or 3 PCLKB
000A 8490h	RSCAN	Receive Buffer Register 15AL*2	RMIDL15	16	16	2 or 3 PCLKB
000A 8492h	RSCAN	Receive Buffer Register 15AH*2	RMIDH15	16	16	2 or 3 PCLKB
000A 8494h	RSCAN	Receive Buffer Register 15BL*2	RMTS15	16	16	2 or 3 PCLKB
000A 8496h	RSCAN	Receive Buffer Register 15BH*2	RMPTR15	16	16	2 or 3 PCLKB
000A 8498h	RSCAN	Receive Buffer Register 15CL*2	RMDF015	16	16	2 or 3 PCLKB
000A 849Ah	RSCAN	Receive Buffer Register 15CH*2	RMDF115	16	16	2 or 3 PCLKB
000A 849Ch	RSCAN	Receive Buffer Register 15DL*2	RMDF215	16	16	2 or 3 PCLKB
000A 849Eh	RSCAN	Receive Buffer Register 15DH*2	RMDF315	16	16	2 or 3 PCLKB
000A 8580h to 000A 859Fh	RSCAN	RAM Test Register 0 to 15*2	RPGACC0 to 15	16	16	2 or 3 PCLKB
000A 85A0h	RSCAN	Receive FIFO Access Register 0AL*2	RFIDL0	16	16	2 or 3 PCLKB
000A 85A0h	RSCAN	RAM Test Register 16*2	RPGACC16	16	16	2 or 3 PCLKB
000A 85A2h	RSCAN	Receive FIFO Access Register 0AH*2	RFIDH0	16	16	2 or 3 PCLKB
000A 85A2h	RSCAN	RAM Test Register 17*2	RPGACC17	16	16	2 or 3 PCLKB
000A 85A4h	RSCAN	Receive FIFO Access Register 0BL*2	RFTS0	16	16	2 or 3 PCLKB
000A 85A4h	RSCAN	RAM Test Register 18*2	RPGACC18	16	16	2 or 3 PCLKB
000A 85A6h	RSCAN	Receive FIFO Access Register 0BH*2	RFPTR0	16	16	2 or 3 PCLKB
000A 85A6h	RSCAN	RAM Test Register 19*2	RPGACC19	16	16	2 or 3 PCLKB
000A 85A8h	RSCAN	Receive FIFO Access Register 0CL*2	RFDF00	16	16	2 or 3 PCLKB
000A 85A8h	RSCAN	RAM Test Register 20*2	RPGACC20	16	16	2 or 3 PCLKB
000A 85AAh	RSCAN	Receive FIFO Access Register 0CH*2	RFDF10	16	16	2 or 3 PCLKB
000A 85AAh	RSCAN	RAM Test Register 21*2	RPGACC21	16	16	2 or 3 PCLKB
000A 85ACh	RSCAN	Receive FIFO Access Register 0DL*2	RFDF20	16	16	2 or 3 PCLKB
000A 85ACh	RSCAN	RAM Test Register 22*2	RPGACC22	16	16	2 or 3 PCLKB
000A 85AEh	RSCAN	Receive FIFO Access Register 0DH*2	RFDF30	16	16	2 or 3 PCLKB
000A 85AEh	RSCAN	RAM Test Register 23*2	RPGACC23	16	16	2 or 3 PCLKB
000A 85B0h	RSCAN	Receive FIFO Access Register 1AL*2	RFIDL1	16	16	2 or 3 PCLKB
000A 85B0h	RSCAN	RAM Test Register 24*2	RPGACC24	16	16	2 or 3 PCLKB
000A 85B2h	RSCAN	Receive FIFO Access Register 1AH*2	RFIDH1	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (27/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000A 85B2h	RSCAN	RAM Test Register 25*2	RPGACC25	16	16	2 or 3 PCLKB
000A 85B4h	RSCAN	Receive FIFO Access Register 1BL*2	RFTS1	16	16	2 or 3 PCLKB
000A 85B4h	RSCAN	RAM Test Register 26*2	RPGACC26	16	16	2 or 3 PCLKB
000A 85B6h	RSCAN	Receive FIFO Access Register 1BH*2	RFPTR1	16	16	2 or 3 PCLKB
000A 85B6h	RSCAN	RAM Test Register 27*2	RPGACC27	16	16	2 or 3 PCLKB
000A 85B8h	RSCAN	Receive FIFO Access Register 1CL*2	RFDF01	16	16	2 or 3 PCLKB
000A 85B8h	RSCAN	RAM Test Register 28*2	RPGACC28	16	16	2 or 3 PCLKB
000A 85BAh	RSCAN	Receive FIFO Access Register 1CH*2	RFDF11	16	16	2 or 3 PCLKB
000A 85BAh	RSCAN	RAM Test Register 29*2	RPGACC29	16	16	2 or 3 PCLKB
000A 85BCh	RSCAN	Receive FIFO Access Register 1DL*2	RFDF21	16	16	2 or 3 PCLKB
000A 85BCh	RSCAN	RAM Test Register 30*2	RPGACC30	16	16	2 or 3 PCLKB
000A 85BEh	RSCAN	Receive FIFO Access Register 1DH*2	RFDF31	16	16	2 or 3 PCLKB
000A 85BEh	RSCAN	RAM Test Register 31*2	RPGACC31	16	16	2 or 3 PCLKB
000A 85C0h to 000A 85DEh	RSCAN	RAM Test Register 32 to 47*2	RPGACC32 to 47	16	16	2 or 3 PCLKB
000A 85E0h	RSCAN0	Transmit/Receive FIFO Access Register 0AL*2	CFIDL0	16	16	2 or 3 PCLKB
000A 85E0h	RSCAN	RAM Test Register 48*2	RPGACC48	16	16	2 or 3 PCLKB
000A 85E2h	RSCAN0	Transmit/Receive FIFO Access Register 0AH*2	CFIDH0	16	16	2 or 3 PCLKB
000A 85E2h	RSCAN	RAM Test Register 49*2	RPGACC49	16	16	2 or 3 PCLKB
000A 85E4h	RSCAN0	Transmit/Receive FIFO Access Register 0BL*2	CFTS0	16	16	2 or 3 PCLKB
000A 85E4h	RSCAN	RAM Test Register 50*2	RPGACC50	16	16	2 or 3 PCLKB
000A 85E6h	RSCAN0	Transmit/Receive FIFO Access Register 0BH*2	CFPTR0	16	16	2 or 3 PCLKB
000A 85E6h	RSCAN	RAM Test Register 51*2	RPGACC51	16	16	2 or 3 PCLKB
000A 85E8h	RSCAN0	Transmit/Receive FIFO Access Register 0CL*2	CFDF00	16	16	2 or 3 PCLKB
000A 85E8h	RSCAN	RAM Test Register 52*2	RPGACC52	16	16	2 or 3 PCLKB
000A 85EAh	RSCAN0	Transmit/Receive FIFO Access Register 0CH*2	CFDF10	16	16	2 or 3 PCLKB
000A 85EAh	RSCAN	RAM Test Register 53*2	RPGACC53	16	16	2 or 3 PCLKB
000A 85ECh	RSCAN0	Transmit/Receive FIFO Access Register 0DL*2	CFDF20	16	16	2 or 3 PCLKB
000A 85ECh	RSCAN	RAM Test Register 54*2	RPGACC54	16	16	2 or 3 PCLKB
000A 85EEh	RSCAN0	Transmit/Receive FIFO Access Register 0DH*2	CFDF30	16	16	2 or 3 PCLKB
000A 85EEh	RSCAN	RAM Test Register 55*2	RPGACC55	16	16	2 or 3 PCLKB
000A 85F0h to 000A 85FEh	RSCAN	RAM Test Register 56 to 63*2	RPGACC56 to 63	16	16	2 or 3 PCLKB
000A 8600h	RSCAN0	Transmit Buffer Register 0AL*2	TMIDL0	16	16	2 or 3 PCLKB
000A 8600h	RSCAN	RAM Test Register 64*2	RPGACC64	16	16	2 or 3 PCLKB
000A 8602h	RSCAN0	Transmit Buffer Register 0AH*2	TMIDH0	16	16	2 or 3 PCLKB
000A 8602h	RSCAN	RAM Test Register 65*2	RPGACC65	16	16	2 or 3 PCLKB
000A 8604h	RSCAN	RAM Test Register 66*2	RPGACC66	16	16	2 or 3 PCLKB
000A 8606h	RSCAN0	Transmit Buffer Register 0BH*2	TMPTR0	16	16	2 or 3 PCLKB
000A 8606h	RSCAN	RAM Test Register 67*2	RPGACC67	16	16	2 or 3 PCLKB
000A 8608h	RSCAN0	Transmit Buffer Register 0CL*2	TMDF00	16	16	2 or 3 PCLKB
000A 8608h	RSCAN	RAM Test Register 68*2	RPGACC68	16	16	2 or 3 PCLKB
000A 860Ah	RSCAN0	Transmit Buffer Register 0CH*2	TMDF10	16	16	2 or 3 PCLKB
000A 860Ah	RSCAN	RAM Test Register 69*2	RPGACC69	16	16	2 or 3 PCLKB
000A 860Ch	RSCAN0	Transmit Buffer Register 0DL*2	TMDF20	16	16	2 or 3 PCLKB
000A 860Ch	RSCAN	RAM Test Register 70*2	RPGACC70	16	16	2 or 3 PCLKB
000A 860Eh	RSCAN0	Transmit Buffer Register 0DH*2	TMDF30	16	16	2 or 3 PCLKB
000A 860Eh	RSCAN	RAM Test Register 71*2	RPGACC71	16	16	2 or 3 PCLKB
000A 8610h	RSCAN0	Transmit Buffer Register 1AL*2	TMIDL1	16	16	2 or 3 PCLKB
000A 8610h	RSCAN	RAM Test Register 72*2	RPGACC72	16	16	2 or 3 PCLKB
000A 8612h	RSCAN0	Transmit Buffer Register 1AH*2	TMIDH1	16	16	2 or 3 PCLKB
000A 8612h	RSCAN	RAM Test Register 73*2	RPGACC73	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (36/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000C 2330h	GPT01	Longword A/D Converter Start Request Timing Double Buffer Register A*2	GTADTDBRALW	32	32	4 or 5 PCLKA
000C 2334h	GPT01	Longword A/D Converter Start Request Timing Register B*2	GTADTRBLW	32	32	4 or 5 PCLKA
000C 2338h	GPT01	Longword A/D Converter Start Request Timing Buffer Register B*2	GTADTBRBLW	32	32	4 or 5 PCLKA
000C 233Ch	GPT01	Longword A/D Converter Start Request Timing Double Buffer Register B*2	GTADTDBRBLW	32	32	4 or 5 PCLKA
000C 2340h	GPT01	General PWM Timer Longword Dead Time Value Register U*2	GTDVULW	32	32	4 or 5 PCLKA
000C 2344h	GPT01	General PWM Timer Longword Dead Time Value Register D*2	GTDVDLW	32	32	4 or 5 PCLKA
000C 2348h	GPT01	General PWM Timer Longword Dead Time Buffer Register U*2	GTDBULW	32	32	4 or 5 PCLKA
000C 234Ch	GPT01	General PWM Timer Longword Dead Time Buffer Register D*2	GTDBDLW	32	32	4 or 5 PCLKA
000C 2380h	GPT23	General PWM Timer Longword Counter*2	GTCNTLW	32	32	4 or 5 PCLKA
000C 2384h	GPT23	General PWM Timer Longword Compare Capture Register A*2	GTCCRALW	32	32	4 or 5 PCLKA
000C 2388h	GPT23	General PWM Timer Longword Compare Capture Register B*2	GTCCRBLW	32	32	4 or 5 PCLKA
000C 238Ch	GPT23	General PWM Timer Longword Compare Capture Register C*2	GTCCRCLW	32	32	4 or 5 PCLKA
000C 2390h	GPT23	General PWM Timer Longword Compare Capture Register D*2	GTCCRDLW	32	32	4 or 5 PCLKA
000C 2394h	GPT23	General PWM Timer Longword Compare Capture Register E*2	GTCCRELW	32	32	4 or 5 PCLKA
000C 2398h	GPT23	General PWM Timer Longword Compare Capture Register F*2	GTCCRFLW	32	32	4 or 5 PCLKA
000C 239Ch	GPT23	General PWM Timer Longword Period Setting Register*2	GTPRLW	32	32	4 or 5 PCLKA
000C 23A0h	GPT23	General PWM Timer Longword Period Setting Buffer Register*2	GTPBRLW	32	32	4 or 5 PCLKA
000C 23A4h	GPT23	General PWM Timer Longword Period Setting Double Buffer Register*2	GTPDBRLW	32	32	4 or 5 PCLKA
000C 23A8h	GPT23	Longword A/D Converter Start Request Timing Register A*2	GTADTRALW	32	32	4 or 5 PCLKA
000C 23ACh	GPT23	Longword A/D Converter Start Request Timing Buffer Register A*2	GTADTBRALW	32	32	4 or 5 PCLKA
000C 23B0h	GPT23	Longword A/D Converter Start Request Timing Double Buffer Register A*2	GTADTDBRALW	32	32	4 or 5 PCLKA
000C 23B4h	GPT23	Longword A/D Converter Start Request Timing Register B*2	GTADTRBLW	32	32	4 or 5 PCLKA
000C 23B8h	GPT23	Longword A/D Converter Start Request Timing Buffer Register B*2	GTADTBRBLW	32	32	4 or 5 PCLKA
000C 23BCh	GPT23	Longword A/D Converter Start Request Timing Double Buffer Register B*2	GTADTDBRBLW	32	32	4 or 5 PCLKA
000C 23C0h	GPT23	General PWM Timer Longword Dead Time Value Register U*2	GTDVULW	32	32	4 or 5 PCLKA
000C 23C4h	GPT23	General PWM Timer Longword Dead Time Value Register D*2	GTDVDLW	32	32	4 or 5 PCLKA
000C 23C8h	GPT23	General PWM Timer Longword Dead Time Buffer Register U*2	GTDBULW	32	32	4 or 5 PCLKA
000C 23CCh	GPT23	General PWM Timer Longword Dead Time Buffer Register D*2	GTDBDLW	32	32	4 or 5 PCLKA
007F C090h	FLASH	E2 DataFlash Control Register	DFLCTL	8	8	2 or 3 FCLK
007F C100h	FLASH	Flash P/E Mode Control Register	FPMCR	8	8	2 or 3 FCLK
007F C104h	FLASH	Flash Area Select Register	FASR	8	8	2 or 3 FCLK
007F C108h	FLASH	Flash Processing Start Address Register L	FSARL	16	16	2 or 3 FCLK
007F C110h	FLASH	Flash Processing Start Address Register H	FSARH	16	16	2 or 3 FCLK
007F C114h	FLASH	Flash Control Register	FCR	8	8	2 or 3 FCLK
007F C118h	FLASH	Flash Processing End Address Register L	FEARL	16	16	2 or 3 FCLK
007F C120h	FLASH	Flash Processing End Address Register H	FEARH	16	16	2 or 3 FCLK
007F C124h	FLASH	Flash Reset Register	FRESETR	8	8	2 or 3 FCLK
007F C12Ch	FLASH	Flash Status Register 1	FSTATR1	8	8	2 or 3 FCLK
007F C130h	FLASH	Flash Write Buffer 0 Register	FWB0	16	16	2 or 3 FCLK
007F C138h	FLASH	Flash Write Buffer 1 Register	FWB1	16	16	2 or 3 FCLK
007F C140h	FLASH	Flash Write Buffer 2 Register	FWB2	16	16	2 or 3 FCLK

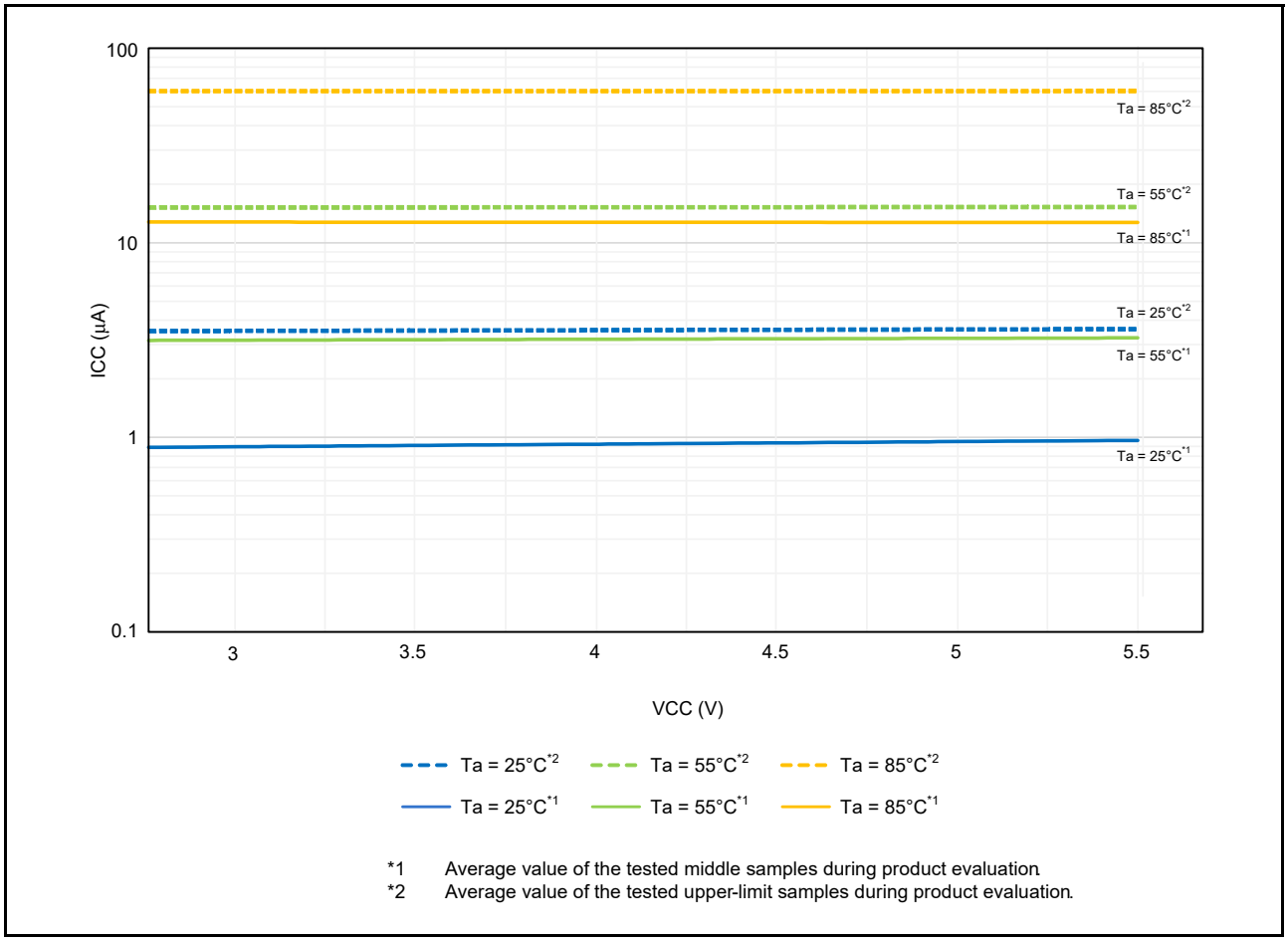


Figure 5.2 Voltage Dependency in Software Standby Mode (Chip Version B) (Reference Data)

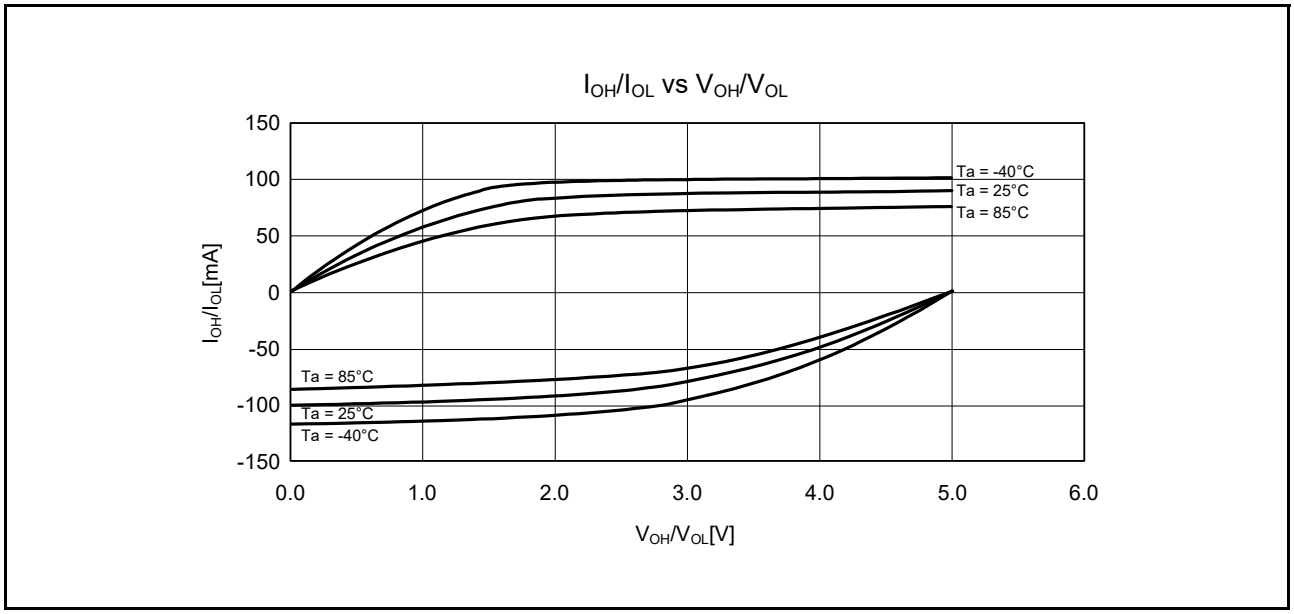


Figure 5.12 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.0 V when Normal Output is Selected (Reference Data)

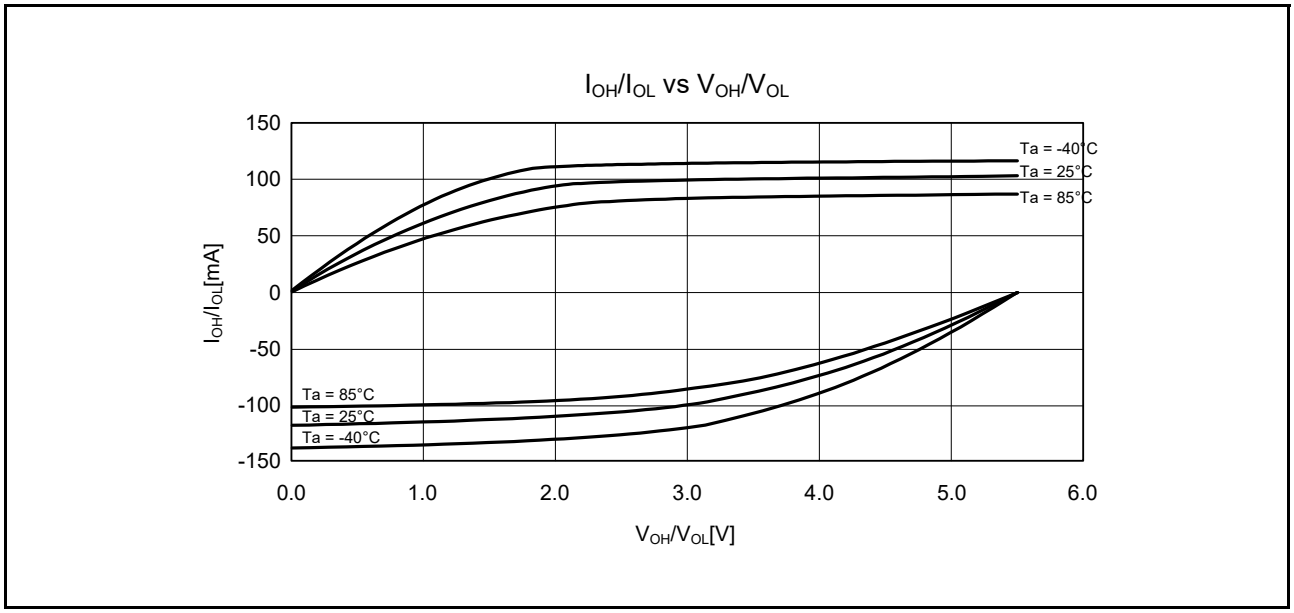


Figure 5.13 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.5 V when Normal Output is Selected (Reference Data)

5.3 AC Characteristics

5.3.1 Clock Timing

Table 5.14 Operating Frequency Value (High-Speed Operating Mode)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	min.	typ.	max.	Unit
Operating frequency	System clock (ICLK)	f_{max}	—	—	80	MHz
	FlashIF clock (FCLK)*1, *2		—	—	32	
	Peripheral module clock (PCLKA)		—	—	80	
	Peripheral module clock (PCLKB)		—	—	40	
	Peripheral module clock (PCLKD)		—	—	40	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.

Table 5.15 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	min.	typ.	max.	Unit
Operating frequency	System clock (ICLK)	f_{max}	—	—	12	MHz
	FlashIF clock (FCLK)*1, *2		—	—	12	
	Peripheral module clock (PCLKA)		—	—	12	
	Peripheral module clock (PCLKB)		—	—	12	
	Peripheral module clock (PCLKD)		—	—	12	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.

Table 5.19 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Middle-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 5.32
			Main clock oscillator and PLL circuit operating*3	t_{SBYPC}	—	2	3	ms	
		External clock input to main clock oscillator	Main clock oscillator operating*4	t_{SBYEX}	—	3	4	µs	
			Main clock oscillator and PLL circuit operating*5	t_{SBYPE}	—	65	85	µs	
		HOCO clock oscillator operating	HOCO clock oscillator operating 1 *6	t_{SBYHO}	—	40	50	µs	
			HOCO clock oscillator operating 2 *7		—	75	85	µs	
			HOCO clock oscillator and PLL circuit operating*8	t_{SBYPH}	—	110	125	µs	
		LOCO clock oscillator operating*9		t_{SBYLO}	—	5	7	µs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.

Note 2. When the frequency of the crystal is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 3. When the frequency of PLL is 48 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 12 MHz.

Note 4. When the frequency of the external clock is 12 MHz.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 5. When the frequency of PLL is 48 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 12 MHz.

Note 6. When the frequency of the high-speed on-chip oscillator is 32 MHz. When the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 05h. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 8 MHz.

Note 7. When the frequency of the high-speed on-chip oscillator is 64 MHz. Set the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 06h. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 8 MHz.

Note 8. When the frequency of the high-speed on-chip oscillator is 32 MHz, and the frequency of PLL is 80 MHz. When the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 05h. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 10 MHz.

Note 9. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Table 5.25 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C, C = 30pF

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.47
	SCK clock cycle input (slave)			6	—	t_{Pcyc}	
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (master)	VCC = 4.0 V or above	t_{SU}	40	—	ns	Figure 5.48, Figure 5.49
		VCC = 2.7 V or above		65	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SS input setup time		t_{LEAD}	3	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	3	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	VCC = 4.0 V or above		—	40		
		VCC = 2.7 V or above		—	65		
	Data output hold time	Master	t_{OH}	–10	—	ns	
		Slave		–10	—		
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SS input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{Pcyc}	Figure 5.50, Figure 5.51
	Slave output release time		t_{REL}	—	6	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

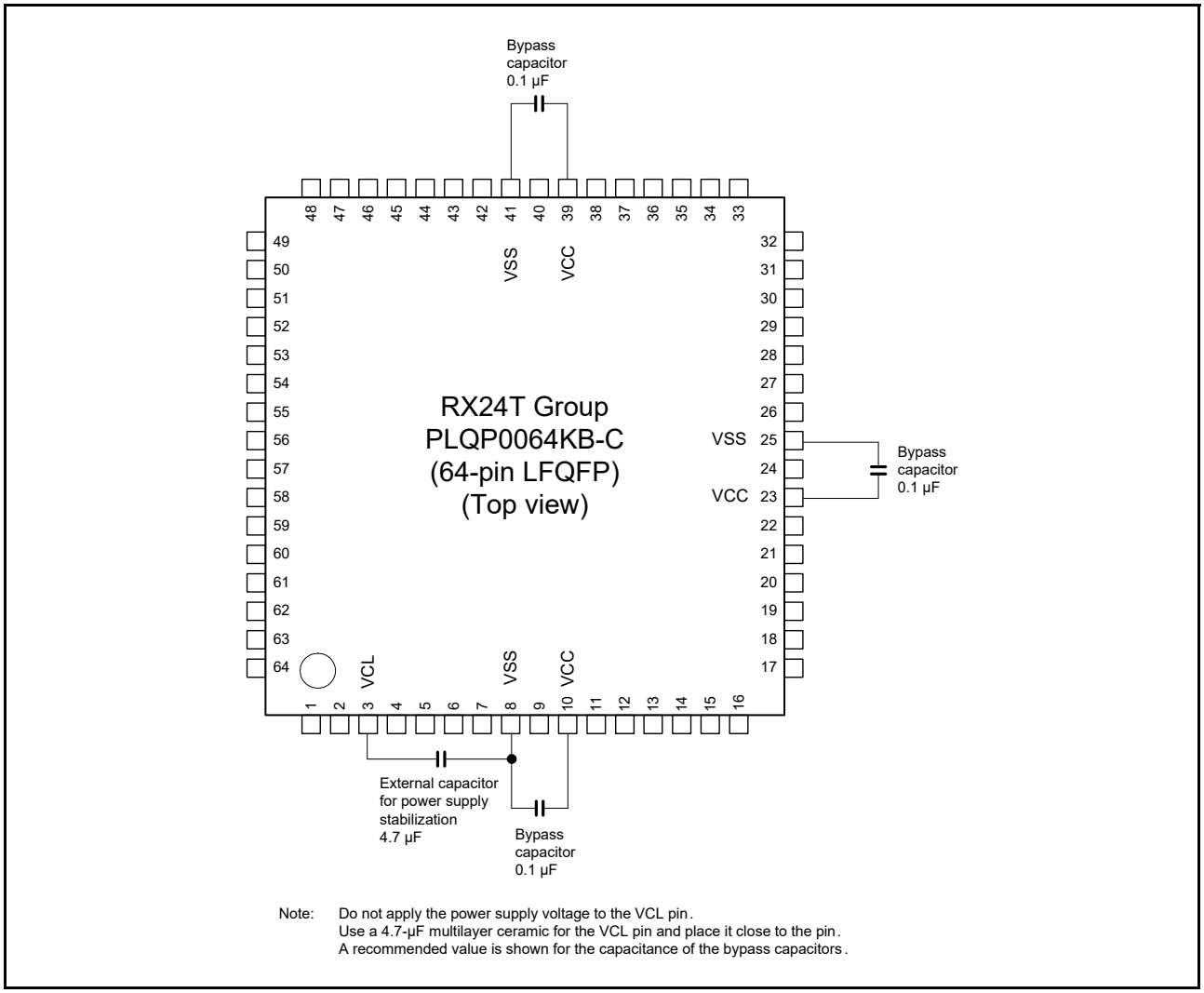


Figure 5.63 Connecting Capacitors (64 Pins)