Renesas Electronics America Inc - R5F524TAADFN#30 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 17x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f524taadfn-30

Table 1.1 Outline of Specifications (4/4)

Classification	Module/Function	Description
12-bit A/D converter (S12ADF)		• 12 bits (5 channels × 2 units/12 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 1.0 µs per channel when the ADCLK is operating at 40 MHz • Operating modes Scan mode (single scan mode, continuous scan mode, and 3 group scan mode) Group A priority control (only for 3 group scan mode) • Sampling variable Sampling time can be set up for each channel • Self-diagnostic function • Double trigger mode (A/D conversion data duplicated) • Assist on analog input disconnection detection • A/D conversion start conditions A software trigger, a trigger from a timer (MTU3, GPT, TMR), or an external trigger signal • Sample-and-hold function Sample-and-hold circuit included (3 channels for unit 1) • Amplification of input signals by a programmable gain amplifier (1 channel for unit 0, 3 channels for unit 1) Amplification rate: 2.0 times, 2.5 times, 3.077 times, 3.636 times, 4.0 times, 4.444 times (total of 6 steps)
Comparator C (CMPC)		• 4 channels • Function to compare the reference voltage and the analog input voltage • Reference voltage: Select from among two voltages • Analog input voltage is selectable from 4 inputs
8-bit D/A converter (DA, DAa)		• DA 1 channel 8-bit resolution Output voltage: 0 V to VREF Dedicated for generating comparator C reference voltage • DAa 2 channels 8-bit resolution Output voltage: 0 V to VREF Can be output externally and used as comparator C reference voltage
Safety	Memory protection unit (MPU)	• Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh. • Minimum protection unit: 16 bytes • Reading from, writing to, and enabling the execution access can be specified for each area. • An address exception occurs when the detected access is not in the permitted area.
	Register write protection function	• Protects important registers from being overwritten for in case a program runs out of control.
	CRC calculator (CRC)	• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
	Main clock oscillation stop function	• Main clock oscillation stop detection: Available
	Clock frequency accuracy measurement circuit (CAC)	• Monitors the clock output from the main clock oscillator, high-speed on-chip oscillator, low-speed on-chip oscillator, the PLL frequency synthesizer, IWDT-dedicated on-chip oscillator, and PCLKB.
	Data operation circuit (DOC)	The function to compare, add, or subtract 16-bit data
Power supply voltages/Operating frequencies		VCC = 2.7 to 5.5 V: 80 MHz
Packages		100-pin LFQFP 0.5 mm pitch 80-pin LQFP 0.65 mm pitch 80-pin LFQFP 0.5 mm pitch 64-pin LFQFP 0.5 mm pitch
On-chip debugging system		E1 emulator (FINE interface)

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP/LFQFP) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, CAC)	Communications (SCI, RSPI, RIIC)	Others
1		P02	MTIOC9D	CTS1#, RTS1#, SS1#	IRQ5, ADST0
2	VSS				
3		P00			IRQ2, ADST1
4	VCL				
5	MD				FINED
6		P01	POE12#		IRQ4, ADST2
7		PE4	MTCLKC, POE10#		IRQ1
8		PE3	MTCLKD, POE11#		IRQ2
9	RES#				
10	XTAL	P37			
11	VSS				
12	EXTAL	P36			
13	VCC				
14		PE2	POE10#		NMI
15		PD7	MTIOC9A, TMRI1, TMRI5	SSLA1	
16		PD6	MTIOC9C, TMO1	CTS1#, RTS1#, SS1#, SSLA0	IRQ5, ADST0
17		PD5	TMRI0, TMRI6	RXD1, SMISO1, SSCL1	IRQ3
18		PD4	TMCI0, TMCI6	SCK1	IRQ2
19		PD3	TMO0	TXD1, SMOSI1, SSDA1	
20		PD2	TMCI1, TMO4	SCK5, MOSIA	
21		PB6		RXD5, SMISO5, SSCL5	IRQ5
22		PB5		TXD5, SMOSI5, SSDA5	
23	VCC				
24		PB4	POE8#	CTS5#, RTS5#, SS5#	IRQ3
25	VSS				
26		PB3	MTIOC0A, CACREF	SCK6, RSPCKA	
27		PB2	MTIOC0B, TMRI0, ADSM0	TXD6, SMOSI6, SSDA6, SDA0	
28		PB1	MTIOC0C, TMCI0, ADSM1	RXD6, SMISO6, SSCL6, SCL0	
29		PB0	MTIOC0D, TMO0	TXD6, SMOSI6, SSDA6, MOSIA	ADTRG2#
30		PA5	MTIOC1A, TMCI3	RXD6, SMISO6, SSCL6, MISOA	IRQ1, ADTRG1#
31		PA3	MTIOC2A, TMRI7	SSLA0	
32	VCC				
33		P96	POE4#		IRQ4
34	VSS				
35		P95	MTIOC6B		
36		P94	MTIOC7A		
37		P93	MTIOC7B		
38		P92	MTIOC6D		
39		P91	MTIOC7C		
40		P90	MTIOC7D		
41		P76	MTIOC4D		
42		P75	MTIOC4C		
43		P74	MTIOC3D		
44		P73	MTIOC4B		
45		P72	MTIOC4A		
46		P71	MTIOC3B		
47		P70	POE0#		IRQ5
48	VCC				

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP/LFQFP) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, CAC)	Communications (SCI, RSPI, RIIC)	Others
49		P31	MTIOC0A, MTCLKC, TMRI6	SSLA1	IRQ6
50	VSS				
51		P30	MTIOC0B, MTCLKD, TMCI6	SSLA0	IRQ7, COMP3
52		P24	MTIC5U, TMCI2, TMO6	RSPCKA	COMP0
53		P23	MTIC5V, TMO2, CACREF	MOSIA	COMP1
54		P22	MTIC5W, TMRI2, TMO4	MISOA	ADTRG2#, COMP2
55		P21	MTCLKA, MTIOC9A, TMCI4		IRQ6, ADTRG1#, AN116, CVREFC1
56		P20	MTCLKB, MTIOC9C, TMRI4		IRQ7, ADTRG0#, AN016, CVREFC0
57	AVCC2				
58	VREF				
59	AVSS2				
60		P62			AN202, IRQ6
61		P55			AN211, IRQ3
62		P54			AN210, IRQ2
63		P53			AN209, IRQ1
64		P52			AN208, IRQ0
65		P51			AN207
66		P50			AN206
67		P47			AN103
68		P46			AN102, CMPC12, CMPC13, CMPC30, CMPC31
69		P45			AN101, CMPC02, CMPC03, CMPC20, CMPC21
70		P44			AN100, CMPC10, CMPC11, CMPC32, CMPC33
71		P43			AN003
72		P42			AN002
73		P41			AN001
74		P40			AN000, CMPC00, CMPC01, CMPC22, CMPC23
75	AVCC1				
76	AVCC0				
77	AVSS0				
78	AVSS1				
79		P11	MTIOC3A, MTCLKC, TMO3		IRQ1
80		P10	MTIOC9B, MTCLKD, TMRI3, POE12#	CTS6#, RTS6#, SS6#	IRQ0

Table 1.8 List of Pins and Pin Functions (64-Pin LFQFP) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, CAC)	Communications (SCI, RSPI, RIIC)	Others
1		P02	MTIOC9D	CTS1#, RTS1#, SS1#	IRQ5, ADST0
2		P00			IRQ2, ADST1
3	VCL				
4	MD				FINED
5		P01	POE12#		IRQ4, ADST2
6	RES#				
7	XTAL	P37			
8	VSS				
9	EXTAL	P36			
10	VCC				
11		PE2	POE10#		NMI
12		PD7	MTIOC9A, TMRI1, TMRI5	SSLA1	
13		PD6	MTIOC9C, TMO1	CTS1#, RTS1#, SS1#	
14		PD5	TMRI0, TMRI6	RXD1, SMISO1, SSCL1	
15		PD4	TMCI0, TMCI6	SCK1	IRQ2
16		PD3	TMO0	TXD1, SMOSI1, SSDA1	
17		PB6		RXD5, SMISO5, SSCL5	IRQ5
18		PB5		TXD5, SMOSI5, SSDA5	
19		PB4	POE8#	CTS5#, RTS5#, SS5#	IRQ3
20		PB3	MTIOC0A, CACREF	SCK6, RSPCKA	
21		PB2	MTIOC0B, TMRI0, ADSM0	TXD6, SMOSI6, SSDA6, SDA0	
22		PB1	MTIOC0C, TMCI0, ADSM1	RXD6, SMISO6, SSCL6, SCL0	
23	VCC				
24		P96	POE4#		IRQ4
25	VSS				
26		P95	MTIOC6B		
27		P94	MTIOC7A		
28		P93	MTIOC7B		
29		P92	MTIOC6D		
30		P91	MTIOC7C		
31		P90	MTIOC7D		
32		P76	MTIOC4D		
33		P75	MTIOC4C		
34		P74	MTIOC3D		
35		P73	MTIOC4B		
36		P72	MTIOC4A		
37		P71	MTIOC3B		
38		P70	POE0#		IRQ5
39	VCC				
40		P31	MTIOC0A, MTCLKC, TMRI6	SSLA1	IRQ6
41	VSS				
42		P30	MTIOC0B, MTCLKD, TMCI6	SSLA0	IRQ7, COMP3
43		P24	MTIC5U, TMCI2, TMO6	RSPCKA	COMP0
44		P23	MTIC5V, TMO2, CACREF	MOSIA	COMP1
45		P22	MTIC5W, TMRI2, TMO4	MISOA	ADTRG2#, COMP2
46		P21	MTCLKA, MTIOC9A, TMCI4		IRQ6, ADTRG1#, AN116, CVREFC1
47	AVCC2/VREF				
48	AVSS2				
49		P54			AN210, IRQ2
50		P53			AN209, IRQ1
51		P52			AN208, IRQ0
52		P51			AN207
53		P50			AN206

Table 4.1 List of I/O Registers (Address Order) (5/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 70D0h	ICU	Interrupt Request Register 208*2	IR208	8	8	2 ICLK
0008 70D1h	ICU	Interrupt Request Register 209*2	IR209	8	8	2 ICLK
0008 70D2h	ICU	Interrupt Request Register 210*2	IR210	8	8	2 ICLK
0008 70D3h	ICU	Interrupt Request Register 211*2	IR211	8	8	2 ICLK
0008 70D4h	ICU	Interrupt Request Register 212*2	IR212	8	8	2 ICLK
0008 70D5h	ICU	Interrupt Request Register 213*2	IR213	8	8	2 ICLK
0008 70D6h	ICU	Interrupt Request Register 214*2	IR214	8	8	2 ICLK
0008 70D7h	ICU	Interrupt Request Register 215*2	IR215	8	8	2 ICLK
0008 70D8h	ICU	Interrupt Request Register 216*2	IR216	8	8	2 ICLK
0008 70D9h	ICU	Interrupt Request Register 217*2	IR217	8	8	2 ICLK
0008 70DAh	ICU	Interrupt Request Register 218	IR218	8	8	2 ICLK
0008 70DBh	ICU	Interrupt Request Register 219	IR219	8	8	2 ICLK
0008 70DCh	ICU	Interrupt Request Register 220	IR220	8	8	2 ICLK
0008 70DDh	ICU	Interrupt Request Register 221	IR221	8	8	2 ICLK
0008 70DEh	ICU	Interrupt Request Register 222	IR222	8	8	2 ICLK
0008 70DFh	ICU	Interrupt Request Register 223	IR223	8	8	2 ICLK
0008 70E0h	ICU	Interrupt Request Register 224	IR224	8	8	2 ICLK
0008 70E1h	ICU	Interrupt Request Register 225	IR225	8	8	2 ICLK
0008 70E2h	ICU	Interrupt Request Register 226	IR226	8	8	2 ICLK
0008 70E3h	ICU	Interrupt Request Register 227	IR227	8	8	2 ICLK
0008 70E4h	ICU	Interrupt Request Register 228	IR228	8	8	2 ICLK
0008 70E5h	ICU	Interrupt Request Register 229	IR229	8	8	2 ICLK
0008 70EEh	ICU	Interrupt Request Register 238*2	IR238	8	8	2 ICLK
0008 70EFh	ICU	Interrupt Request Register 239*2	IR239	8	8	2 ICLK
0008 70F0h	ICU	Interrupt Request Register 240*2	IR240	8	8	2 ICLK
0008 70F1h	ICU	Interrupt Request Register 241*2	IR241	8	8	2 ICLK
0008 70F2h	ICU	Interrupt Request Register 242*2	IR242	8	8	2 ICLK
0008 70F3h	ICU	Interrupt Request Register 243*2	IR243	8	8	2 ICLK
0008 70F4h	ICU	Interrupt Request Register 244*2	IR244	8	8	2 ICLK
0008 70F6h	ICU	Interrupt Request Register 246	IR246	8	8	2 ICLK
0008 70F7h	ICU	Interrupt Request Register 247	IR247	8	8	2 ICLK
0008 70F8h	ICU	Interrupt Request Register 248	IR248	8	8	2 ICLK
0008 70F9h	ICU	Interrupt Request Register 249	IR249	8	8	2 ICLK
0008 711Bh	ICU	DTC Transfer Request Enable Register 027	DTCER027	8	8	2 ICLK
0008 711Ch	ICU	DTC Transfer Request Enable Register 028	DTCER028	8	8	2 ICLK
0008 711Dh	ICU	DTC Transfer Request Enable Register 029	DTCER029	8	8	2 ICLK
0008 711Eh	ICU	DTC Transfer Request Enable Register 030	DTCER030	8	8	2 ICLK
0008 711Fh	ICU	DTC Transfer Request Enable Register 031	DTCER031	8	8	2 ICLK
0008 712Dh	ICU	DTC Transfer Request Enable Register 045	DTCER045	8	8	2 ICLK
0008 712Eh	ICU	DTC Transfer Request Enable Register 046	DTCER046	8	8	2 ICLK
0008 7130h	ICU	DTC Transfer Request Enable Register 048*2	DTCER048	8	8	2 ICLK
0008 7131h	ICU	DTC Transfer Request Enable Register 049*2	DTCER049	8	8	2 ICLK
0008 7132h	ICU	DTC Transfer Request Enable Register 050*2	DTCER050	8	8	2 ICLK
0008 7133h	ICU	DTC Transfer Request Enable Register 051*2	DTCER051	8	8	2 ICLK
0008 7135h	ICU	DTC Transfer Request Enable Register 053*2	DTCER053	8	8	2 ICLK
0008 7136h	ICU	DTC Transfer Request Enable Register 054*2	DTCER054	8	8	2 ICLK
0008 7137h	ICU	DTC Transfer Request Enable Register 055*2	DTCER055	8	8	2 ICLK
0008 7138h	ICU	DTC Transfer Request Enable Register 056*2	DTCER056	8	8	2 ICLK
0008 713Bh	ICU	DTC Transfer Request Enable Register 059*2	DTCER059	8	8	2 ICLK
0008 7140h	ICU	DTC Transfer Request Enable Register 064	DTCER064	8	8	2 ICLK
0008 7141h	ICU	DTC Transfer Request Enable Register 065	DTCER065	8	8	2 ICLK
0008 7142h	ICU	DTC Transfer Request Enable Register 066	DTCER066	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (11/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 8006h	CMT0	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB
0008 800Ah	CMT1	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB
0008 800Ch	CMT1	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2 or 3 PCLKB
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB
0008 8014h	CMT2	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB
0008 8016h	CMT2	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB
0008 801Ah	CMT3	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB
0008 801Ch	CMT3	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2 or 3 PCLKB
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2 or 3 PCLKB
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2 or 3 PCLKB
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2 or 3 PCLKB
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSTPR	8	8	2 or 3 PCLKB
0008 80C0h	DA	D/A Data Register 0	DADR0	16	16	2 or 3 PCLKB
0008 80C2h	DA	D/A Data Register 1*2	DADR1	16	16	2 or 3 PCLKB
0008 80C4h	DA	D/A Control Register	DACR	8	8	2 or 3 PCLKB
0008 80C5h	DA	DADRm Format Select Register	DADPR	8	8	2 or 3 PCLKB
0008 80C6h	DA	D/A A/D Synchronous Start Control Register*2	DAADSCR	8	8	2 or 3 PCLKB
0008 8200h	TMR0	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8201h	TMR1	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8202h	TMR0	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8203h	TMR1	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8204h	TMR0	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8205h	TMR1	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB
0008 8206h	TMR0	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8207h	TMR1	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB
0008 8208h	TMR0	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8209h	TMR1	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB
0008 820Ah	TMR0	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 820Bh	TMR1	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB
0008 8210h	TMR2	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8211h	TMR3	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8212h	TMR2	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8213h	TMR3	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8214h	TMR2	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8215h	TMR3	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB
0008 8216h	TMR2	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8217h	TMR3	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB
0008 8218h	TMR2	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8219h	TMR3	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB
0008 821Ah	TMR2	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB
0008 8220h	TMR4	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8221h	TMR5	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8222h	TMR4	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8223h	TMR5	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8224h	TMR4	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8225h	TMR5	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB
0008 8226h	TMR4	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (14/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 9214h	S12AD1	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB
0008 9216h	S12AD1	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB
0008 9218h	S12AD1	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB
0008 921Eh	S12AD1	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB
0008 9220h	S12AD1	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB
0008 9222h	S12AD1	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB
0008 9224h	S12AD1	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB
0008 9226h	S12AD1	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB
0008 9240h	S12AD1	A/D Data Register 16	ADDR16	16	16	2 or 3 PCLKB
0008 9266h	S12AD1	A/D Sample-and-hold Circuit Control Register	ADSHCR	16	16	2 or 3 PCLKB
0008 927Ah	S12AD1	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB
0008 9280h	S12AD1	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB
0008 9284h	S12AD1	A/D Data Duplication Register A	ADDBLDRA	16	16	2 or 3 PCLKB
0008 9286h	S12AD1	A/D Data Duplication Register B	ADDBLDRB	16	16	2 or 3 PCLKB
0008 92D4h	S12AD1	A/D Channel Select Register C0	ADANSC0	16	16	2 or 3 PCLKB
0008 92D6h	S12AD1	A/D Channel Select Register C1	ADANSC1	16	16	2 or 3 PCLKB
0008 92D9h	S12AD1	A/D Group C Trigger Select Register	ADGCTRGR	8	8	2 or 3 PCLKB
0008 92DDh	S12AD1	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB
0008 92E0h	S12AD1	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB
0008 92E1h	S12AD1	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB
0008 92E2h	S12AD1	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB
0008 92E3h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB
0008 93A0h	S12AD1	A/D Programmable Gain Amplifier Control Register	ADPGACR	16	16	2 or 3 PCLKB
0008 93A2h	S12AD1	A/D Programmable Gain Amplifier Gain Setting Register 0	ADPGAGS0	16	16	2 or 3 PCLKB
0008 9400h	S12AD2	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB
0008 9404h	S12AD2	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB
0008 9408h	S12AD2	A/D-Converted Value Addition/Average Function Channel Select Register 0	ADADS0	16	16	2 or 3 PCLKB
0008 940Ch	S12AD2	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB
0008 940Eh	S12AD2	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB
0008 9410h	S12AD2	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB
0008 9412h	S12AD2	A/D Conversion Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB
0008 9414h	S12AD2	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB
0008 9418h	S12AD2	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB
0008 941Ch	S12AD2	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB
0008 941Eh	S12AD2	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB
0008 9420h	S12AD2	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB
0008 9422h	S12AD2	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB
0008 9424h	S12AD2	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB
0008 9426h	S12AD2	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB
0008 9428h	S12AD2	A/D Data Register 4	ADDR4	16	16	2 or 3 PCLKB
0008 942Ah	S12AD2	A/D Data Register 5	ADDR5	16	16	2 or 3 PCLKB
0008 942Ch	S12AD2	A/D Data Register 6	ADDR6	16	16	2 or 3 PCLKB
0008 942Eh	S12AD2	A/D Data Register 7	ADDR7	16	16	2 or 3 PCLKB
0008 9430h	S12AD2	A/D Data Register 8	ADDR8	16	16	2 or 3 PCLKB
0008 9432h	S12AD2	A/D Data Register 9	ADDR9	16	16	2 or 3 PCLKB
0008 9434h	S12AD2	A/D Data Register 10	ADDR10	16	16	2 or 3 PCLKB
0008 9436h	S12AD2	A/D Data Register 11	ADDR11	16	16	2 or 3 PCLKB
0008 947Ah	S12AD2	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB
0008 9480h	S12AD2	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB
0008 9484h	S12AD2	A/D Data Duplication Register A	ADDBLDRA	16	16	2 or 3 PCLKB
0008 9486h	S12AD2	A/D Data Duplication Register B	ADDBLDRB	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (23/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000A 83C4h	RSCAN	Receive Buffer Register 2BL*2	RMTS2	16	16	2 or 3 PCLKB
000A 83C6h	RSCAN	Receive Rule Entry Register 3AH*2	GAFLIDH3	16	16	2 or 3 PCLKB
000A 83C6h	RSCAN	Receive Buffer Register 2BH*2	RMPTR2	16	16	2 or 3 PCLKB
000A 83C8h	RSCAN	Receive Rule Entry Register 3BL*2	GAFLML3	16	16	2 or 3 PCLKB
000A 83C8h	RSCAN	Receive Buffer Register 2CL*2	RMDF02	16	16	2 or 3 PCLKB
000A 83CAh	RSCAN	Receive Rule Entry Register 3BH*2	GAFLMH3	16	16	2 or 3 PCLKB
000A 83CAh	RSCAN	Receive Buffer Register 2CH*2	RMDF12	16	16	2 or 3 PCLKB
000A 83CCh	RSCAN	Receive Rule Entry Register 3CL*2	GAFLPL3	16	16	2 or 3 PCLKB
000A 83CCh	RSCAN	Receive Buffer Register 2DL*2	RMDF22	16	16	2 or 3 PCLKB
000A 83CEh	RSCAN	Receive Rule Entry Register 3CH*2	GAFLPH3	16	16	2 or 3 PCLKB
000A 83CEh	RSCAN	Receive Buffer Register 2DH*2	RMDF32	16	16	2 or 3 PCLKB
000A 83D0h	RSCAN	Receive Rule Entry Register 4AL*2	GAFLIDL4	16	16	2 or 3 PCLKB
000A 83D0h	RSCAN	Receive Buffer Register 3AL*2	RMIDL3	16	16	2 or 3 PCLKB
000A 83D2h	RSCAN	Receive Rule Entry Register 4AH*2	GAFLIDH4	16	16	2 or 3 PCLKB
000A 83D2h	RSCAN	Receive Buffer Register 3AH*2	RMIDH3	16	16	2 or 3 PCLKB
000A 83D4h	RSCAN	Receive Rule Entry Register 4BL*2	GAFLML4	16	16	2 or 3 PCLKB
000A 83D4h	RSCAN	Receive Buffer Register 3BL*2	RMTS3	16	16	2 or 3 PCLKB
000A 83D6h	RSCAN	Receive Rule Entry Register 4BH*2	GAFLMH4	16	16	2 or 3 PCLKB
000A 83D6h	RSCAN	Receive Buffer Register 3BH*2	RMPTR3	16	16	2 or 3 PCLKB
000A 83D8h	RSCAN	Receive Rule Entry Register 4CL*2	GAFLPL4	16	16	2 or 3 PCLKB
000A 83D8h	RSCAN	Receive Buffer Register 3CL*2	RMDF03	16	16	2 or 3 PCLKB
000A 83DAh	RSCAN	Receive Rule Entry Register 4CH*2	GAFLPH4	16	16	2 or 3 PCLKB
000A 83DAh	RSCAN	Receive Buffer Register 3CH*2	RMDF13	16	16	2 or 3 PCLKB
000A 83DCh	RSCAN	Receive Rule Entry Register 5AL*2	GAFLIDL5	16	16	2 or 3 PCLKB
000A 83DCh	RSCAN	Receive Buffer Register 3DL*2	RMDF23	16	16	2 or 3 PCLKB
000A 83DEh	RSCAN	Receive Rule Entry Register 5AH*2	GAFLIDH5	16	16	2 or 3 PCLKB
000A 83DEh	RSCAN	Receive Buffer Register 3DH*2	RMDF33	16	16	2 or 3 PCLKB
000A 83E0h	RSCAN	Receive Rule Entry Register 5BL*2	GAFLML5	16	16	2 or 3 PCLKB
000A 83E0h	RSCAN	Receive Buffer Register 4AL*2	RMIDL4	16	16	2 or 3 PCLKB
000A 83E2h	RSCAN	Receive Rule Entry Register 5BH*2	GAFLMH5	16	16	2 or 3 PCLKB
000A 83E2h	RSCAN	Receive Buffer Register 4AH*2	RMIDH4	16	16	2 or 3 PCLKB
000A 83E4h	RSCAN	Receive Rule Entry Register 5CL*2	GAFLPL5	16	16	2 or 3 PCLKB
000A 83E4h	RSCAN	Receive Buffer Register 4BL*2	RMTS4	16	16	2 or 3 PCLKB
000A 83E6h	RSCAN	Receive Rule Entry Register 5CH*2	GAFLPH5	16	16	2 or 3 PCLKB
000A 83E6h	RSCAN	Receive Buffer Register 4BH*2	RMPTR4	16	16	2 or 3 PCLKB
000A 83E8h	RSCAN	Receive Rule Entry Register 6AL*2	GAFLIDL6	16	16	2 or 3 PCLKB
000A 83E8h	RSCAN	Receive Buffer Register 4CL*2	RMDF04	16	16	2 or 3 PCLKB
000A 83EAh	RSCAN	Receive Rule Entry Register 6AH*2	GAFLIDH6	16	16	2 or 3 PCLKB
000A 83EAh	RSCAN	Receive Buffer Register 4CH*2	RMDF14	16	16	2 or 3 PCLKB
000A 83ECh	RSCAN	Receive Rule Entry Register 6BL*2	GAFLML6	16	16	2 or 3 PCLKB
000A 83ECh	RSCAN	Receive Buffer Register 4DL*2	RMDF24	16	16	2 or 3 PCLKB
000A 83EEh	RSCAN	Receive Rule Entry Register 6BH*2	GAFLMH6	16	16	2 or 3 PCLKB
000A 83EEh	RSCAN	Receive Buffer Register 4DH*2	RMDF34	16	16	2 or 3 PCLKB
000A 83F0h	RSCAN	Receive Rule Entry Register 6CL*2	GAFLPL6	16	16	2 or 3 PCLKB
000A 83F0h	RSCAN	Receive Buffer Register 5AL*2	RMIDL5	16	16	2 or 3 PCLKB
000A 83F2h	RSCAN	Receive Rule Entry Register 6CH*2	GAFLPH6	16	16	2 or 3 PCLKB
000A 83F2h	RSCAN	Receive Buffer Register 5AH*2	RMIDH5	16	16	2 or 3 PCLKB
000A 83F4h	RSCAN	Receive Rule Entry Register 7AL*2	GAFLIDL7	16	16	2 or 3 PCLKB
000A 83F4h	RSCAN	Receive Buffer Register 5BL*2	RMTS5	16	16	2 or 3 PCLKB
000A 83F6h	RSCAN	Receive Rule Entry Register 7AH*2	GAFLIDH7	16	16	2 or 3 PCLKB
000A 83F6h	RSCAN	Receive Buffer Register 5BH*2	RMPTR5	16	16	2 or 3 PCLKB
000A 83F8h	RSCAN	Receive Rule Entry Register 7BL*2	GAFLML7	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (24/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
000A 83F8h	RSCAN	Receive Buffer Register 5CL*2	RMDF05	16	16	2 or 3 PCLKB
000A 83FAh	RSCAN	Receive Rule Entry Register 7BH*2	GAFLMH7	16	16	2 or 3 PCLKB
000A 83FAh	RSCAN	Receive Buffer Register 5CH*2	RMDF15	16	16	2 or 3 PCLKB
000A 83FCh	RSCAN	Receive Rule Entry Register 7CL*2	GAFLPL7	16	16	2 or 3 PCLKB
000A 83FCh	RSCAN	Receive Buffer Register 5DL*2	RMDF25	16	16	2 or 3 PCLKB
000A 83FEh	RSCAN	Receive Rule Entry Register 7CH*2	GAFLPH7	16	16	2 or 3 PCLKB
000A 83FEh	RSCAN	Receive Buffer Register 5DH*2	RMDF35	16	16	2 or 3 PCLKB
000A 8400h	RSCAN	Receive Rule Entry Register 8AL*2	GAFLIDL8	16	16	2 or 3 PCLKB
000A 8400h	RSCAN	Receive Buffer Register 6AL*2	RMIDL6	16	16	2 or 3 PCLKB
000A 8402h	RSCAN	Receive Rule Entry Register 8AH*2	GAFLIDH8	16	16	2 or 3 PCLKB
000A 8402h	RSCAN	Receive Buffer Register 6AH*2	RMIDH6	16	16	2 or 3 PCLKB
000A 8404h	RSCAN	Receive Rule Entry Register 8BL*2	GAFLML8	16	16	2 or 3 PCLKB
000A 8404h	RSCAN	Receive Buffer Register 6BL*2	RMTS6	16	16	2 or 3 PCLKB
000A 8406h	RSCAN	Receive Rule Entry Register 8BH*2	GAFLMH8	16	16	2 or 3 PCLKB
000A 8406h	RSCAN	Receive Buffer Register 6BH*2	RMPTR6	16	16	2 or 3 PCLKB
000A 8408h	RSCAN	Receive Rule Entry Register 8CL*2	GAFLPL8	16	16	2 or 3 PCLKB
000A 8408h	RSCAN	Receive Buffer Register 6CL*2	RMDF06	16	16	2 or 3 PCLKB
000A 840Ah	RSCAN	Receive Rule Entry Register 8CH*2	GAFLPH8	16	16	2 or 3 PCLKB
000A 840Ah	RSCAN	Receive Buffer Register 6CH*2	RMDF16	16	16	2 or 3 PCLKB
000A 840Ch	RSCAN	Receive Rule Entry Register 9AL*2	GAFLIDL9	16	16	2 or 3 PCLKB
000A 840Ch	RSCAN	Receive Buffer Register 6DL*2	RMDF26	16	16	2 or 3 PCLKB
000A 840Eh	RSCAN	Receive Rule Entry Register 9AH*2	GAFLIDH9	16	16	2 or 3 PCLKB
000A 840Eh	RSCAN	Receive Buffer Register 6DH*2	RMDF36	16	16	2 or 3 PCLKB
000A 8410h	RSCAN	Receive Rule Entry Register 9BL*2	GAFLML9	16	16	2 or 3 PCLKB
000A 8410h	RSCAN	Receive Buffer Register 7AL*2	RMIDL7	16	16	2 or 3 PCLKB
000A 8412h	RSCAN	Receive Rule Entry Register 9BH*2	GAFLMH9	16	16	2 or 3 PCLKB
000A 8412h	RSCAN	Receive Buffer Register 7AH*2	RMIDH7	16	16	2 or 3 PCLKB
000A 8414h	RSCAN	Receive Rule Entry Register 9CL*2	GAFLPL9	16	16	2 or 3 PCLKB
000A 8414h	RSCAN	Receive Buffer Register 7BL*2	RMTS7	16	16	2 or 3 PCLKB
000A 8416h	RSCAN	Receive Rule Entry Register 9CH*2	GAFLPH9	16	16	2 or 3 PCLKB
000A 8416h	RSCAN	Receive Buffer Register 7BH*2	RMPTR7	16	16	2 or 3 PCLKB
000A 8418h	RSCAN	Receive Rule Entry Register 10AL*2	GAFLIDL10	16	16	2 or 3 PCLKB
000A 8418h	RSCAN	Receive Buffer Register 7CL*2	RMDF07	16	16	2 or 3 PCLKB
000A 841Ah	RSCAN	Receive Rule Entry Register 10AH*2	GAFLIDH10	16	16	2 or 3 PCLKB
000A 841Ah	RSCAN	Receive Buffer Register 7CH*2	RMDF17	16	16	2 or 3 PCLKB
000A 841Ch	RSCAN	Receive Rule Entry Register 10BL*2	GAFLML10	16	16	2 or 3 PCLKB
000A 841Ch	RSCAN	Receive Buffer Register 7DL*2	RMDF27	16	16	2 or 3 PCLKB
000A 841Eh	RSCAN	Receive Rule Entry Register 10BH*2	GAFLMH10	16	16	2 or 3 PCLKB
000A 841Eh	RSCAN	Receive Buffer Register 7DH*2	RMDF37	16	16	2 or 3 PCLKB
000A 8420h	RSCAN	Receive Rule Entry Register 10CL*2	GAFLPL10	16	16	2 or 3 PCLKB
000A 8420h	RSCAN	Receive Buffer Register 8AL*2	RMIDL8	16	16	2 or 3 PCLKB
000A 8422h	RSCAN	Receive Rule Entry Register 10CH*2	GAFLPH10	16	16	2 or 3 PCLKB
000A 8422h	RSCAN	Receive Buffer Register 8AH*2	RMIDH8	16	16	2 or 3 PCLKB
000A 8424h	RSCAN	Receive Rule Entry Register 11AL*2	GAFLIDL11	16	16	2 or 3 PCLKB
000A 8424h	RSCAN	Receive Buffer Register 8BL*2	RMTS8	16	16	2 or 3 PCLKB
000A 8426h	RSCAN	Receive Rule Entry Register 11AH*2	GAFLIDH11	16	16	2 or 3 PCLKB
000A 8426h	RSCAN	Receive Buffer Register 8BH*2	RMPTR8	16	16	2 or 3 PCLKB
000A 8428h	RSCAN	Receive Rule Entry Register 11BL*2	GAFLML11	16	16	2 or 3 PCLKB
000A 8428h	RSCAN	Receive Buffer Register 8CL*2	RMDF08	16	16	2 or 3 PCLKB
000A 842Ah	RSCAN	Receive Rule Entry Register 11BH*2	GAFLMH11	16	16	2 or 3 PCLKB
000A 842Ah	RSCAN	Receive Buffer Register 8CH*2	RMDF18	16	16	2 or 3 PCLKB
000A 842Ch	RSCAN	Receive Rule Entry Register 11CL*2	GAFLPL11	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (26/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
000A 8462h	RSCAN	Receive Buffer Register 12AH*2	RMIDH12	16	16	2 or 3 PCLKB
000A 8464h	RSCAN	Receive Buffer Register 12BL*2	RMTS12	16	16	2 or 3 PCLKB
000A 8466h	RSCAN	Receive Buffer Register 12BH*2	RMPTR12	16	16	2 or 3 PCLKB
000A 8468h	RSCAN	Receive Buffer Register 12CL*2	RMDF012	16	16	2 or 3 PCLKB
000A 846Ah	RSCAN	Receive Buffer Register 12CH*2	RMDF112	16	16	2 or 3 PCLKB
000A 846Ch	RSCAN	Receive Buffer Register 12DL*2	RMDF212	16	16	2 or 3 PCLKB
000A 846Eh	RSCAN	Receive Buffer Register 12DH*2	RMDF312	16	16	2 or 3 PCLKB
000A 8470h	RSCAN	Receive Buffer Register 13AL*2	RMIDL13	16	16	2 or 3 PCLKB
000A 8472h	RSCAN	Receive Buffer Register 13AH*2	RMIDH13	16	16	2 or 3 PCLKB
000A 8474h	RSCAN	Receive Buffer Register 13BL*2	RMTS13	16	16	2 or 3 PCLKB
000A 8476h	RSCAN	Receive Buffer Register 13BH*2	RMPTR13	16	16	2 or 3 PCLKB
000A 8478h	RSCAN	Receive Buffer Register 13CL*2	RMDF013	16	16	2 or 3 PCLKB
000A 847Ah	RSCAN	Receive Buffer Register 13CH*2	RMDF113	16	16	2 or 3 PCLKB
000A 847Ch	RSCAN	Receive Buffer Register 13DL*2	RMDF213	16	16	2 or 3 PCLKB
000A 847Eh	RSCAN	Receive Buffer Register 13DH*2	RMDF313	16	16	2 or 3 PCLKB
000A 8480h	RSCAN	Receive Buffer Register 14AL*2	RMIDL14	16	16	2 or 3 PCLKB
000A 8482h	RSCAN	Receive Buffer Register 14AH*2	RMIDH14	16	16	2 or 3 PCLKB
000A 8484h	RSCAN	Receive Buffer Register 14BL*2	RMTS14	16	16	2 or 3 PCLKB
000A 8486h	RSCAN	Receive Buffer Register 14BH*2	RMPTR14	16	16	2 or 3 PCLKB
000A 8488h	RSCAN	Receive Buffer Register 14CL*2	RMDF014	16	16	2 or 3 PCLKB
000A 848Ah	RSCAN	Receive Buffer Register 14CH*2	RMDF114	16	16	2 or 3 PCLKB
000A 848Ch	RSCAN	Receive Buffer Register 14DL*2	RMDF214	16	16	2 or 3 PCLKB
000A 848Eh	RSCAN	Receive Buffer Register 14DH*2	RMDF314	16	16	2 or 3 PCLKB
000A 8490h	RSCAN	Receive Buffer Register 15AL*2	RMIDL15	16	16	2 or 3 PCLKB
000A 8492h	RSCAN	Receive Buffer Register 15AH*2	RMIDH15	16	16	2 or 3 PCLKB
000A 8494h	RSCAN	Receive Buffer Register 15BL*2	RMTS15	16	16	2 or 3 PCLKB
000A 8496h	RSCAN	Receive Buffer Register 15BH*2	RMPTR15	16	16	2 or 3 PCLKB
000A 8498h	RSCAN	Receive Buffer Register 15CL*2	RMDF015	16	16	2 or 3 PCLKB
000A 849Ah	RSCAN	Receive Buffer Register 15CH*2	RMDF115	16	16	2 or 3 PCLKB
000A 849Ch	RSCAN	Receive Buffer Register 15DL*2	RMDF215	16	16	2 or 3 PCLKB
000A 849Eh	RSCAN	Receive Buffer Register 15DH*2	RMDF315	16	16	2 or 3 PCLKB
000A 8580h to 000A 859Fh	RSCAN	RAM Test Register 0 to 15*2	RPGACC0 to 15	16	16	2 or 3 PCLKB
000A 85A0h	RSCAN	Receive FIFO Access Register 0AL*2	RFIDL0	16	16	2 or 3 PCLKB
000A 85A0h	RSCAN	RAM Test Register 16*2	RPGACC16	16	16	2 or 3 PCLKB
000A 85A2h	RSCAN	Receive FIFO Access Register 0AH*2	RFIDH0	16	16	2 or 3 PCLKB
000A 85A2h	RSCAN	RAM Test Register 17*2	RPGACC17	16	16	2 or 3 PCLKB
000A 85A4h	RSCAN	Receive FIFO Access Register 0BL*2	RFTS0	16	16	2 or 3 PCLKB
000A 85A4h	RSCAN	RAM Test Register 18*2	RPGACC18	16	16	2 or 3 PCLKB
000A 85A6h	RSCAN	Receive FIFO Access Register 0BH*2	RFPTR0	16	16	2 or 3 PCLKB
000A 85A6h	RSCAN	RAM Test Register 19*2	RPGACC19	16	16	2 or 3 PCLKB
000A 85A8h	RSCAN	Receive FIFO Access Register 0CL*2	RFDF00	16	16	2 or 3 PCLKB
000A 85A8h	RSCAN	RAM Test Register 20*2	RPGACC20	16	16	2 or 3 PCLKB
000A 85AAh	RSCAN	Receive FIFO Access Register 0CH*2	RFDF10	16	16	2 or 3 PCLKB
000A 85AAh	RSCAN	RAM Test Register 21*2	RPGACC21	16	16	2 or 3 PCLKB
000A 85ACh	RSCAN	Receive FIFO Access Register 0DL*2	RFDF20	16	16	2 or 3 PCLKB
000A 85ACh	RSCAN	RAM Test Register 22*2	RPGACC22	16	16	2 or 3 PCLKB
000A 85AEh	RSCAN	Receive FIFO Access Register 0DH*2	RFDF30	16	16	2 or 3 PCLKB
000A 85AEh	RSCAN	RAM Test Register 23*2	RPGACC23	16	16	2 or 3 PCLKB
000A 85B0h	RSCAN	Receive FIFO Access Register 1AL*2	RFIDL1	16	16	2 or 3 PCLKB
000A 85B0h	RSCAN	RAM Test Register 24*2	RPGACC24	16	16	2 or 3 PCLKB
000A 85B2h	RSCAN	Receive FIFO Access Register 1AH*2	RFIDH1	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (33/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
000C 202Ch	GPT	General PWM Timer A/D Conversion Start Request Signal Monitor Register*2	GTADSMR	32	8, 16, 32	4 or 5 PCLKA
000C 2100h	GPT0	General PWM Timer I/O Control Register*2	GTIOR	16	8, 16, 32	4 or 5 PCLKA
000C 2102h	GPT0	General PWM Timer Interrupt Output Setting Register*2	GTINTAD	16	8, 16, 32	4 or 5 PCLKA
000C 2104h	GPT0	General PWM Timer Control Register*2	GTCR	16	8, 16, 32	4 or 5 PCLKA
000C 2106h	GPT0	General PWM Timer Buffer Enable Register*2	GTBER	16	8, 16, 32	4 or 5 PCLKA
000C 2108h	GPT0	General PWM Timer Count Direction Register*2	GTUDC	16	8, 16, 32	4 or 5 PCLKA
000C 210Ah	GPT0	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register*2	GTITC	16	8, 16, 32	4 or 5 PCLKA
000C 210Ch	GPT0	General PWM Timer Status Register*2	GTST	16	8, 16, 32	4 or 5 PCLKA
000C 210Eh	GPT0	General PWM Timer Counter*2	GTCNT	16	16	4 or 5 PCLKA
000C 2110h	GPT0	General PWM Timer Compare Capture Register A*2	GTCCRA	16	16, 32	4 or 5 PCLKA
000C 2112h	GPT0	General PWM Timer Compare Capture Register B*2	GTCCRB	16	16, 32	4 or 5 PCLKA
000C 2114h	GPT0	General PWM Timer Compare Capture Register C*2	GTCCRC	16	16, 32	4 or 5 PCLKA
000C 2116h	GPT0	General PWM Timer Compare Capture Register D*2	GTCCRD	16	16, 32	4 or 5 PCLKA
000C 2118h	GPT0	General PWM Timer Compare Capture Register E*2	GTCCRE	16	16, 32	4 or 5 PCLKA
000C 211Ah	GPT0	General PWM Timer Compare Capture Register F*2	GTCCRF	16	16, 32	4 or 5 PCLKA
000C 211Ch	GPT0	General PWM Timer Period Setting Register*2	GTPR	16	16, 32	4 or 5 PCLKA
000C 211Eh	GPT0	General PWM Timer Period Setting Buffer Register*2	GTPBR	16	16, 32	4 or 5 PCLKA
000C 2120h	GPT0	General PWM Timer Period Setting Double Buffer Register*2	GTPDBR	16	16, 32	4 or 5 PCLKA
000C 2124h	GPT0	A/D Converter Start Request Timing Register A*2	GTADTRA	16	16, 32	4 or 5 PCLKA
000C 2126h	GPT0	A/D Converter Start Request Timing Buffer Register A*2	GTADTBRA	16	16, 32	4 or 5 PCLKA
000C 2128h	GPT0	A/D Converter Start Request Timing Double Buffer Register A*2	GTADTDBRA	16	16, 32	4 or 5 PCLKA
000C 212Ch	GPT0	A/D Converter Start Request Timing Register B*2	GTADTRB	16	16, 32	4 or 5 PCLKA
000C 212Eh	GPT0	A/D Converter Start Request Timing Buffer Register B*2	GTADTBRB	16	16, 32	4 or 5 PCLKA
000C 2130h	GPT0	A/D Converter Start Request Timing Double Buffer Register B*2	GTADTDBRB	16	16, 32	4 or 5 PCLKA
000C 2134h	GPT0	General PWM Timer Output Negate Control Register*2	GTONCR	16	16, 32	4 or 5 PCLKA
000C 2136h	GPT0	General PWM Timer Dead Time Control Register*2	GTDTCR	16	16, 32	4 or 5 PCLKA
000C 2138h	GPT0	General PWM Timer Dead Time Value Register U*2	GTDVU	16	16, 32	4 or 5 PCLKA
000C 213Ah	GPT0	General PWM Timer Dead Time Value Register D*2	GTDVD	16	16, 32	4 or 5 PCLKA
000C 213Ch	GPT0	General PWM Timer Dead Time Buffer Register U*2	GTDBU	16	16, 32	4 or 5 PCLKA
000C 213Eh	GPT0	General PWM Timer Dead Time Buffer Register D*2	GTDBD	16	16, 32	4 or 5 PCLKA
000C 2140h	GPT0	General PWM Timer Output Protection Function Status Register*2	GTSOS	16	16, 32	4 or 5 PCLKA
000C 2142h	GPT0	General PWM Timer Output Protection Function Temporary Release Register*2	GTSOTR	16	16, 32	4 or 5 PCLKA
000C 2180h	GPT1	General PWM Timer I/O Control Register*2	GTIOR	16	8, 16, 32	4 or 5 PCLKA
000C 2182h	GPT1	General PWM Timer Interrupt Output Setting Register*2	GTINTAD	16	8, 16, 32	4 or 5 PCLKA
000C 2184h	GPT1	General PWM Timer Control Register*2	GTCR	16	8, 16, 32	4 or 5 PCLKA
000C 2186h	GPT1	General PWM Timer Buffer Enable Register*2	GTBER	16	8, 16, 32	4 or 5 PCLKA
000C 2188h	GPT1	General PWM Timer Count Direction Register*2	GTUDC	16	8, 16, 32	4 or 5 PCLKA
000C 218Ah	GPT1	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register*2	GTITC	16	8, 16, 32	4 or 5 PCLKA
000C 218Ch	GPT1	General PWM Timer Status Register*2	GTST	16	8, 16, 32	4 or 5 PCLKA
000C 218Eh	GPT1	General PWM Timer Counter*2	GTCNT	16	16	4 or 5 PCLKA
000C 2190h	GPT1	General PWM Timer Compare Capture Register A*2	GTCCRA	16	16, 32	4 or 5 PCLKA
000C 2192h	GPT1	General PWM Timer Compare Capture Register B*2	GTCCRB	16	16, 32	4 or 5 PCLKA
000C 2194h	GPT1	General PWM Timer Compare Capture Register C*2	GTCCRC	16	16, 32	4 or 5 PCLKA
000C 2196h	GPT1	General PWM Timer Compare Capture Register D*2	GTCCRD	16	16, 32	4 or 5 PCLKA
000C 2198h	GPT1	General PWM Timer Compare Capture Register E*2	GTCCRE	16	16, 32	4 or 5 PCLKA
000C 219Ah	GPT1	General PWM Timer Compare Capture Register F*2	GTCCRF	16	16, 32	4 or 5 PCLKA
000C 219Ch	GPT1	General PWM Timer Period Setting Register*2	GTPR	16	16, 32	4 or 5 PCLKA
000C 219Eh	GPT1	General PWM Timer Period Setting Buffer Register*2	GTPBR	16	16, 32	4 or 5 PCLKA

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = AVSS1 = AVSS2 = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC	–0.3 to +6.5	V
Input voltage	Port 4, port 5, port 6	V_{in}	–0.3 to VREF + 0.3	V
	Except for port 4, port 5, port 6 and ports for 5 V tolerant*1		–0.3 to VCC + 0.3	V
	Ports for 5 V tolerant*1		–0.3 to +6.5	V
Analog power supply voltage		AVCC0, AVCC1, AVCC2, VREF	–0.3 to +6.5	V
Analog input voltage	When AN000 to AN003, AN100 to AN103, AN200 to AN211 used	V_{AN}	–0.3 to VREF + 0.3	V
	When AN016, AN116, CVREFC0, CVREFC1 used		–0.3 to VCC + 0.3	
Operating temperature		T_{opr}	–40 to +85	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the AVCC1 and AVSS1 pins, between the AVCC2 and AVSS2 pins, between the VREF and AVSS2 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.
Connect the VCL pin to a VSS pin via a 4.7 µF capacitor. The capacitor must be placed close to the pin.
Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered.
The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.
Even if –0.3 to +6.5 V is input to 5-V tolerant ports, it will not cause problems such as damage to the MCU.
Note 1. Ports B1 and B2 are 5 V tolerant.

Table 5.2 Recommended Operating Voltage Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltages	VCC*1, *2		2.7	—	5.5	V
	VSS		—	0	—	
Analog power supply voltages	AVCC0, AVCC1, AVCC2, VREF*1, *2		VCC	—	5.5	V
	AVSS0, AVSS1, AVSS2		—	0	—	

Note 1. AVCC0/AVCC1/AVCC2/VREF and VCC can be set individually within the operating range.
Note 2. When powering on the VCC and AVCC0/AVCC1/AVCC2/VREF pins, power them on at the same time or the VCC pin first and then the AVCC0/AVCC1/AVCC2/VREF pin.

Item					Symbol	Chip Version A		Chip Version B		Unit	Test Conditions
						Typ. *7	Max.	Typ. *7	Max.		
Supply current *1	High-speed operating mode	Deep sleep mode	No peripheral operation*2	ICLK = 80 MHz	I_{CC}	3.4	—	3.4	—	mA	
				ICLK = 64 MHz		2.9	—	2.9	—		
				ICLK = 32 MHz		2.5	—	2.5	—		
				ICLK = 16 MHz		2.3	—	2.3	—		
				ICLK = 8 MHz		2.2	—	2.2	—		
			All peripheral operation: Normal	ICLK = 80 MHz*3		17.7	—	22.2	—		
				ICLK = 64 MHz*4		14.4	—	17.9	—		
				ICLK = 32 MHz*5		10.9	—	12.9	—		
				ICLK = 16 MHz*5		6.6	—	7.6	—		
				ICLK = 8 MHz*5		4.3	—	4.8	—		
		Increase during BGO operation*6				2.5	—	2.5	—		
	Middle-speed operating modes	Normal operating mode	No peripheral operation*8	ICLK = 12 MHz*10	I_{CC}	5.3	—	5.3	—	mA	
				ICLK = 8 MHz		4.5	—	4.5	—		
				ICLK = 1 MHz		2.5	—	2.5	—		
			All peripheral operation: Normal*9	ICLK = 12 MHz*10		7.8	—	8.7	—		
				ICLK = 8 MHz		6.3	—	6.9	—		
				ICLK = 1 MHz		2.7	—	2.7	—		
			All peripheral operation: Max.*9	ICLK = 12 MHz*10		—	17.0	—	18.0		
		Sleep mode	No peripheral operation*8	ICLK = 12 MHz*10		2.6	—	2.6	—		
				ICLK = 8 MHz		2.7	—	2.7	—		
				ICLK = 1 MHz		2.2	—	2.2	—		
			All peripheral operation: Normal*9	ICLK = 12 MHz*10		6.0	—	6.7	—		
				ICLK = 8 MHz		5.1	—	5.6	—		
				ICLK = 1 MHz		2.5	—	2.5	—		
		Deep sleep mode	No peripheral operation*8	ICLK = 12 MHz*10		1.8	—	1.8	—		
				ICLK = 8 MHz		2.1	—	2.1	—		
				ICLK = 1 MHz		2.1	—	2.1	—		
			All peripheral operation: Normal*9	ICLK = 12 MHz*10		5.0	—	5.7	—		
				ICLK = 8 MHz		4.3	—	4.8	—		
				ICLK = 1 MHz		2.3	—	2.3	—		
		Increase during BGO operation*6				2.5	—	2.5	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Supply of the clock signal to peripheral modules is stopped in this state. The clock source is PLL. FCLK, PCLKA, PCLKB, and PCLKD are set to divided by 64.
Note 3. The clock signal to peripheral modules is supplied in this state. The clock source is PLL. FCLK is set to divided by 4. PCLKA is set to divided by 1. PCLKB and PCLKD are set to divided by 2.
Note 4. The clock signal to peripheral modules is supplied in this state. The clock source is PLL. PCLKA is set to divided by 1. FCLK, PCLKB, and PCLKD are set to divided by 2.
Note 5. The clock signal to peripheral modules is supplied in this state. The clock source is PLL. The frequencies of FCLK, PCLKA, PCLKB, and PCLKD are same as ICLK.
Note 6. This is the increase when data is programmed to or erased from the ROM or E2 DataFlash during program execution.
Note 7. Values when VCC = 5 V.
Note 8. Supply of the clock signal to peripheral modules is stopped in this state. The clock source is PLL. FCLK, PCLKA, PCLKB, and PCLKD are set to divided by 64.
Note 9. Supply of the clock signal to peripheral modules is stopped in this state. The clock source is PLL. The frequencies of FCLK, PCLKA, PCLKB, and PCLKD are same as ICLK.
Note 10. When the frequency of PLL is 48 MHz.

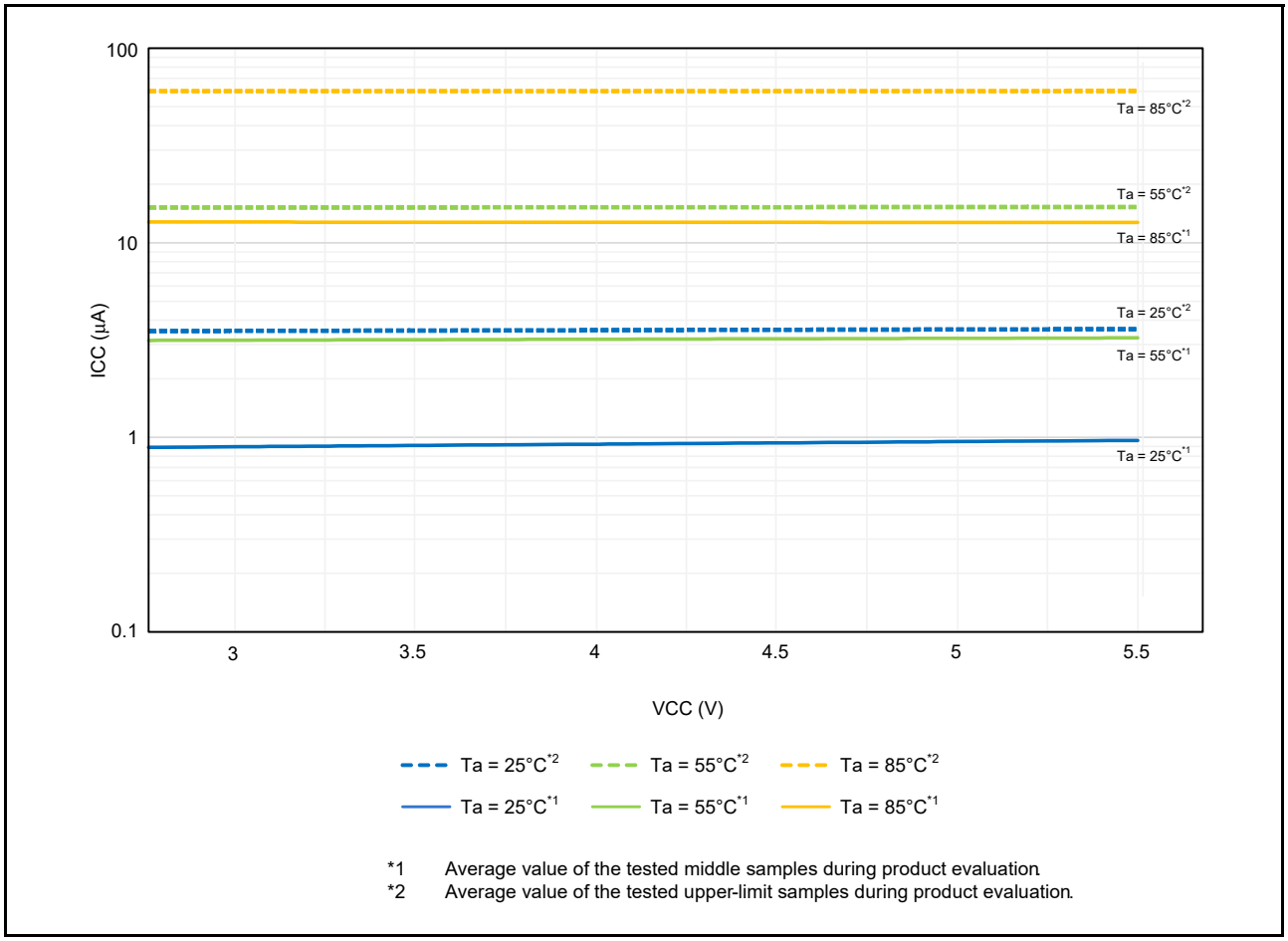


Figure 5.2 Voltage Dependency in Software Standby Mode (Chip Version B) (Reference Data)

Table 5.7 DC Characteristics (5)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total consumption power*1	Pd	—	570	mW	

Note 1. Total power dissipated by the entire chip (including output currents)

Table 5.8 DC Characteristics (6)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

	Item		Symbol	Min.	Typ.*2	Max.	Unit	Test Conditions
Analog power supply current	A/D unit 0	During A/D conversion (programmable gain amplifier in use)	I_{AVCC}	—	1.5	2.5	mA	
		During A/D conversion (programmable gain amplifier not in use)		—	1.0	1.8		
	A/D unit 1	During A/D conversion (sample-and-hold circuits in use, programmable gain amplifier in use)		—	4.6	6.9		
		During A/D conversion (sample-and-hold circuits in use, programmable gain amplifier not in use)		—	3.1	4.8		
		During A/D conversion (sample-and-hold circuits not in use, programmable gain amplifier in use)		—	2.5	3.9		
		During A/D conversion (sample-and-hold circuits not in use, programmable gain amplifier not in use)		—	1.0	1.8		
	A/D unit 2			—	1.0	1.8		
	During D/A conversion (per channel)*1			—	0.7	1.0		
	Waiting for A/D or D/A conversion (all units)			—	—	2.2	µA	
	Waiting for A/D conversion (all units)			—	—	1.2	µA	
Comparator C operating current*3	Comparator enabled		I_{CMP}	—	40.0	60.0	µA	

Note 1. The value of the D/A converter is the value of the power supply current including the reference current.
Note 2. When VCC =AVCC0 = AVCC1 = AVCC2 = VREF = 5 V.
Note 3. Current consumed only by the comparator C module.

Table 5.9 DC Characteristics (7)

Conditions: VCC = 0 V to AVCC0, AVCC0 = AVCC1 = AVCC2 = VREF = 0 V to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power-on VCC rising gradient	At normal startup	SrVCC	0.02	—	20	ms/V	
	Voltage monitoring 0 reset enabled at startup*1, *2		0.02	—	—		

Note 1. When OFS1.LVDAS = 0.
Note 2. Turn on the power supply voltage according to the normal startup rising gradient because the register settings set by OFS1 are not read in boot mode.

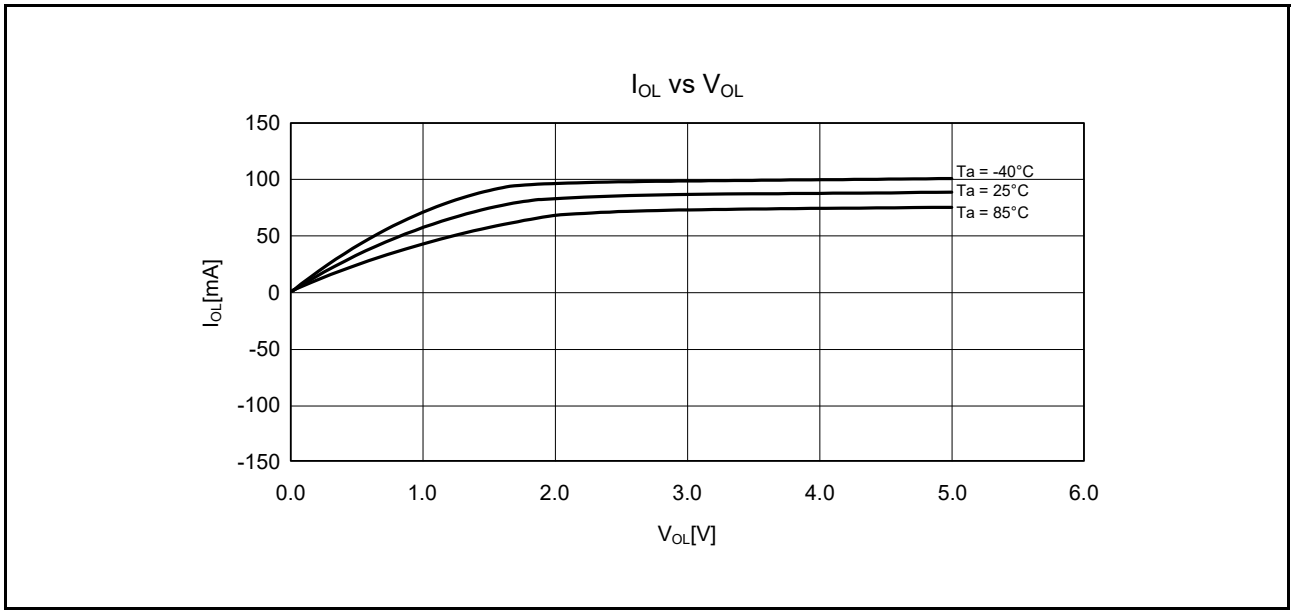


Figure 5.20 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 5.0 V (Reference Data)

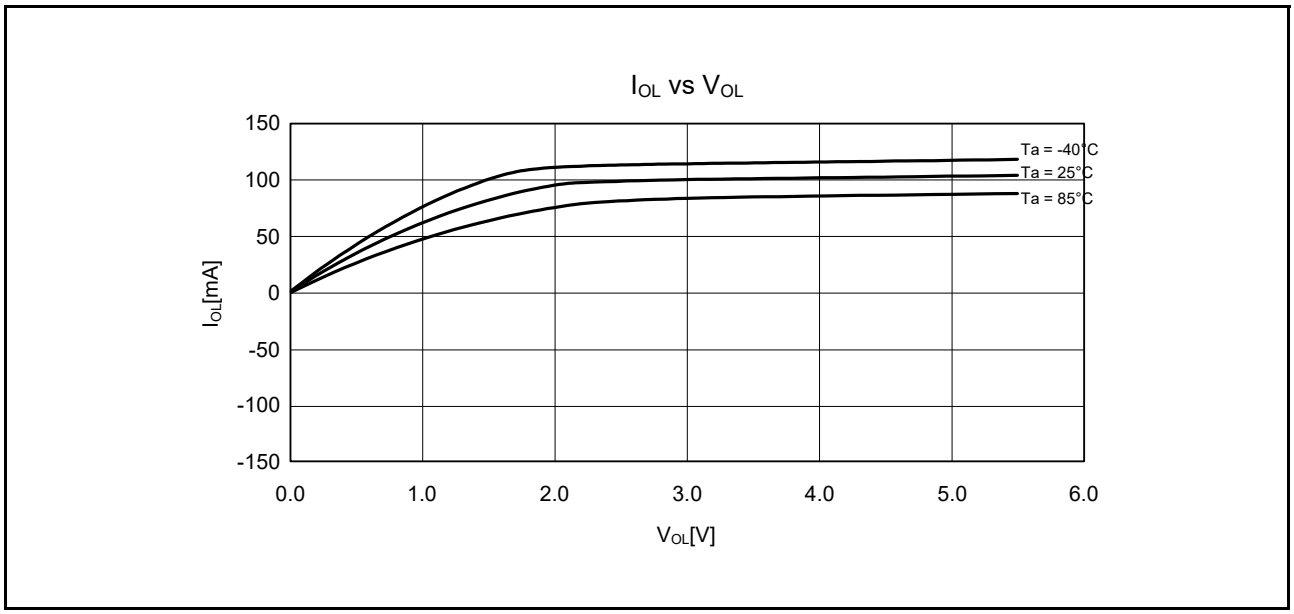


Figure 5.21 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 5.5 V (Reference Data)

5.3 AC Characteristics

5.3.1 Clock Timing

Table 5.14 Operating Frequency Value (High-Speed Operating Mode)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	min.	typ.	max.	Unit
Operating frequency	System clock (ICLK)	f_{max}	—	—	80	MHz
	FlashIF clock (FCLK)*1, *2		—	—	32	
	Peripheral module clock (PCLKA)		—	—	80	
	Peripheral module clock (PCLKB)		—	—	40	
	Peripheral module clock (PCLKD)		—	—	40	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.

Table 5.15 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	min.	typ.	max.	Unit
Operating frequency	System clock (ICLK)	f_{max}	—	—	12	MHz
	FlashIF clock (FCLK)*1, *2		—	—	12	
	Peripheral module clock (PCLKA)		—	—	12	
	Peripheral module clock (PCLKB)		—	—	12	
	Peripheral module clock (PCLKD)		—	—	12	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.

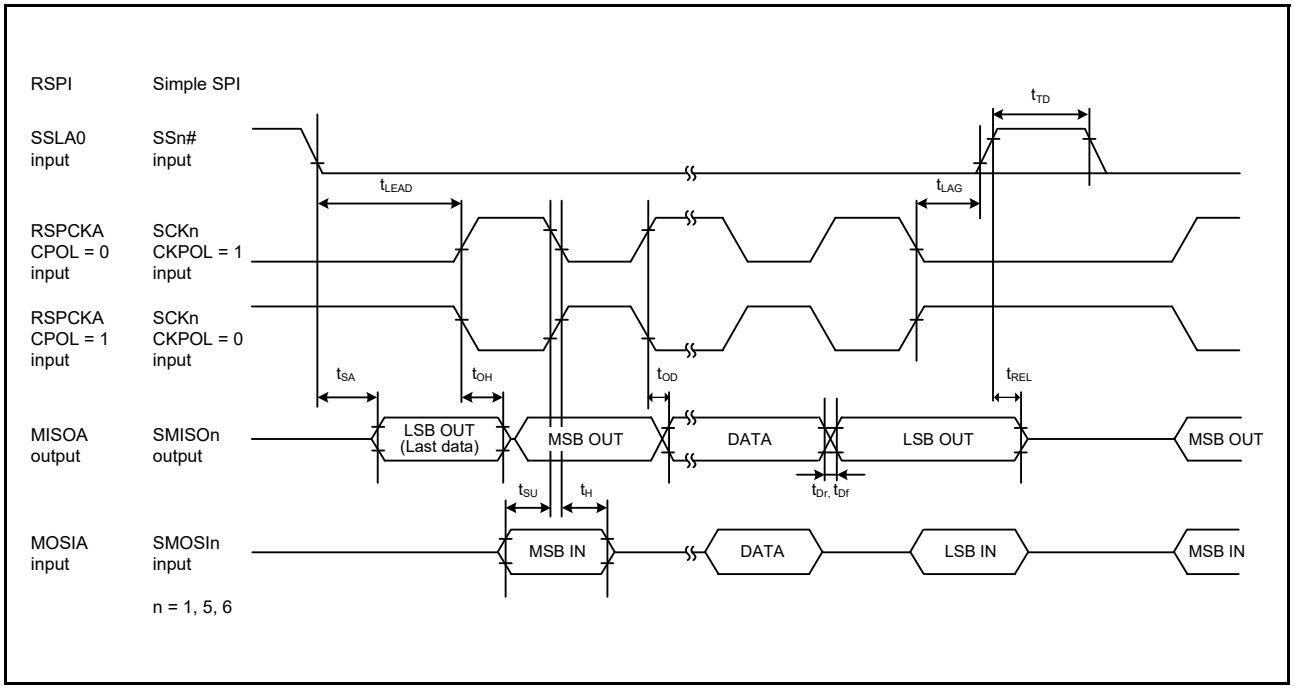
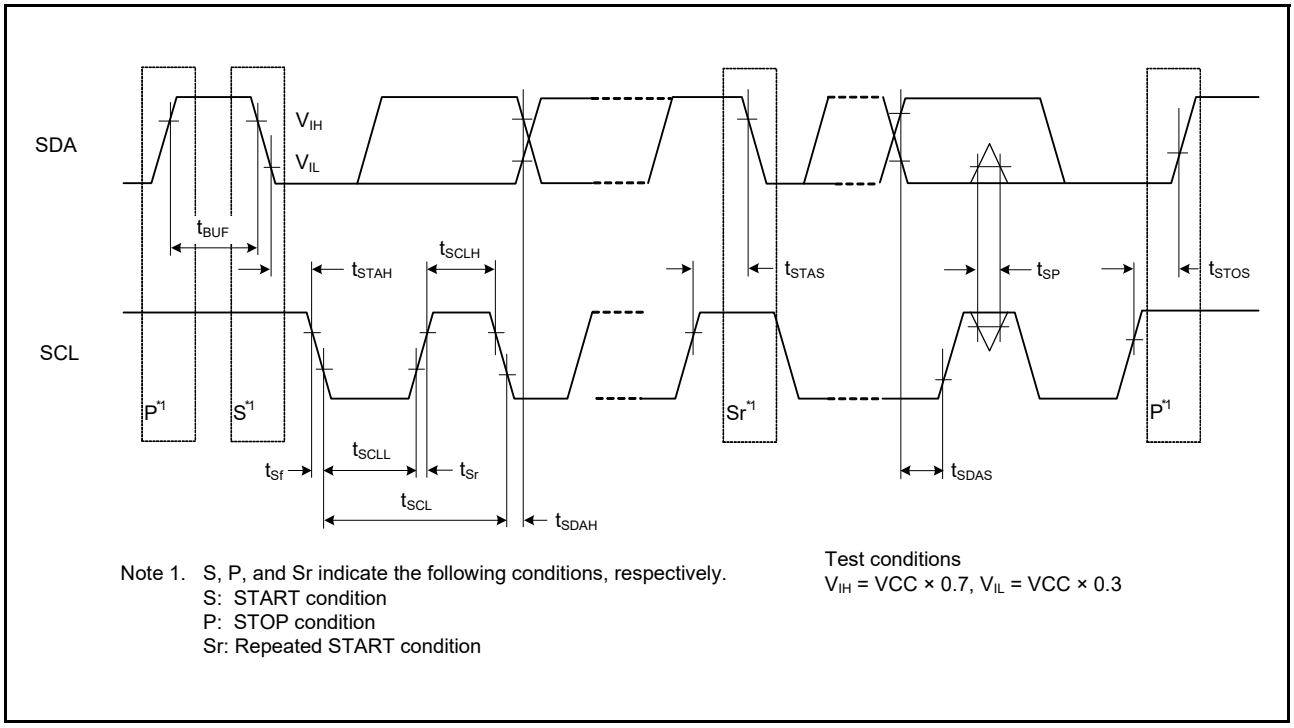


Figure 5.51 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0)



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: Repeated START condition

Test conditions
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3

Figure 5.52 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

5.7 D/A Conversion Characteristics

Table 5.34 Characteristics of D/A Conversion (Chip Version A)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	—	8	Bit	
Conversion time	t_{DCONV}	—	—	3.0	µs	
Absolute accuracy	—	—	—	±3.0	LSB	

Table 5.35 Characteristics of D/A Conversion (Chip Version B)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	—	8	Bit	
Conversion time	t_{DCONV}	—	—	3.0	µs	
Absolute accuracy	—	—	—	±3.0	LSB	
Output load resistance	—	4	—	—	MΩ	
Output load capacity	—	—	—	35	pF	
Output resistance	—	—	9.0	—	kΩ	

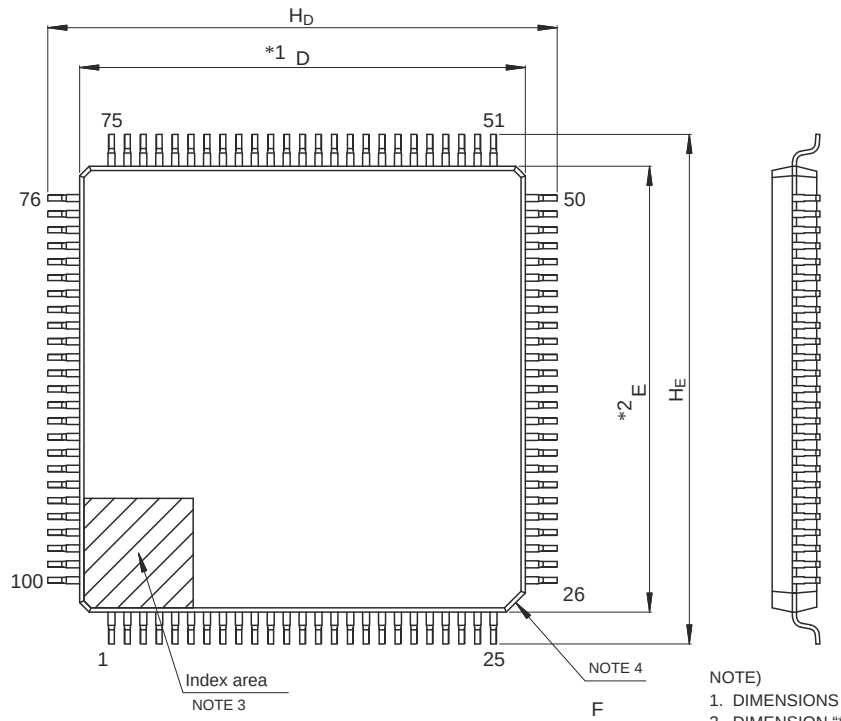
Note: When using ports 23 and 24 as DA0 and DA1 outputs, make sure that VCC ≥ DA output voltage.

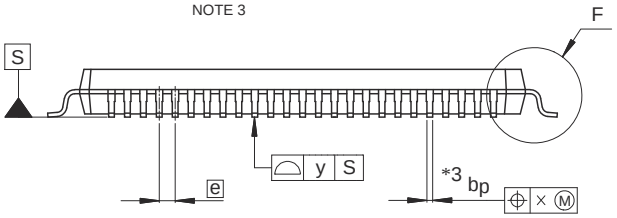
Appendix 1. Package Dimensions

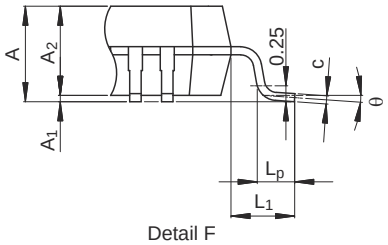
Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm







NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure A 100-Pin LFQFP (PLQP0100KB-B)