Renesas Electronics America Inc - R5F524TAADFN#31 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 17x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f524taadfn-31

Table 1.1 Outline of Specifications (3/4)

Classification	Module/Function	Description
Timers	General PWM timer (GPTB)	• 16 bits × 4 channels • Two channels can be cascaded and used as a 32-bit timer • Counting up or down (saw waves), or counting up and down (triangle waves) is selectable for each counter. • A count clock is selectable from 13 types (PCLK/1, PCLK/2, PCLK/4, PCLK/8, PCLK/16,PCLK/32, PCLK/64, PCLK/256, PCLK/1024, GTECLKA, GTECLKB, GTECLKC, and GTECLKD) for each channel. • Two I/O pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms. • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Synchronous operation of the several counters • Modes of synchronous operation (synchronized or displaced by a desired time to obtain relative phase shifts) • Generation of dead times in PWM operation • Through combination of three counters, generation of three-phased PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: output of the comparator detection, MTU3 count start, software, compare match • Noise filter function for signals on the Input capture, external trigger pins, and the external count clock pins • A/D converter start triggers can be generated
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Count clock: Dedicated low-speed on-chip oscillator for the IWDT-dedicated on-chip oscillator Frequency divided by 1, 16, 32, 64, 128, or 256
	8-bit timer (TMR)	• (8 bits × 2 channels) × 4 units • Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, and PCLK/8192) and an external clock can be selected • Pulse output and PWM output with any duty cycle are available • Two channels can be cascaded and used as a 16-bit timer • Generates A/D conversion start trigger • Generates baud rate clock for the SCI5 and SCI6
Communication functions	Serial communications interfaces (SCIg)	• 3 channels (channel 1, 5, and 6: SCIg) • SCIg Serial communications: asynchronous, clock synchronous, and smart-card interface On-chip baud rate generator allows selection of the desired bit rate Selection of LSB-first or MSB first transfer Average transfer rate clocks for SCI5 and SCI6 can be input from TMR timers Simple I^2C Simple SPI Multi-processor function Detection of the start bit: Level or edge is selectable. 9-bit transfer mode Bit rate modulation
	I^2C bus interface (RIICa)	• 1 channel • Communications formats: I^2C bus format/SMBus format • Master mode or slave mode selectable • Supports fast mode
	CAN module (RSCAN)	• Single channel • ISO11898-1 specifications compliant (standard and extended frames) • 16 message boxes
	Serial peripheral interface (RSPIb)	• 1 channel • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception

1.3 Block Diagram

Figure 1.2 shows a block diagram.

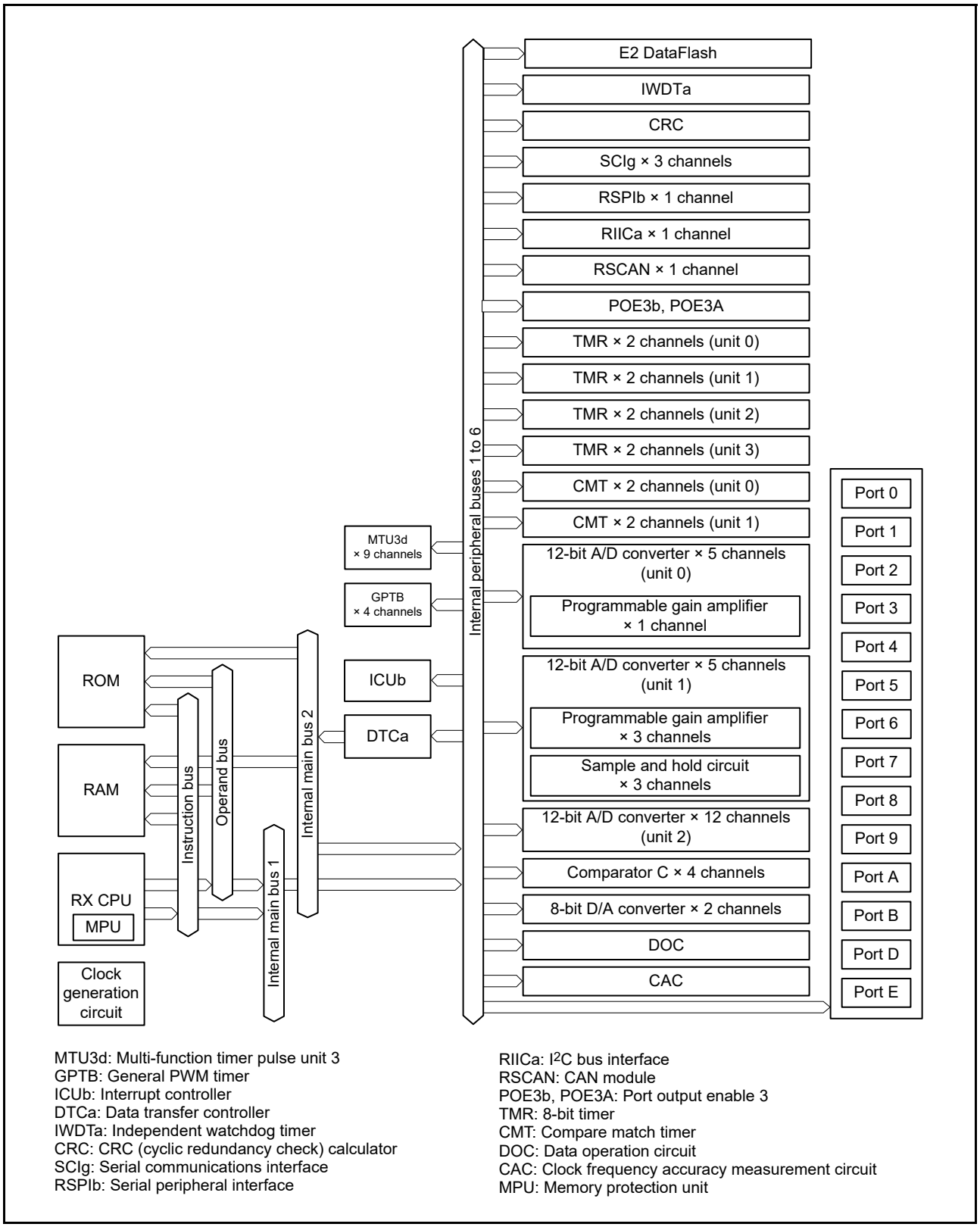


Figure 1.2 Block Diagram

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version B) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
94	AVSS0				
95	AVSS1				
96		P82	MTIC5U, MTIC5U#, TMO4	SCK6	
97		P81	MTIC5V, MTIC5V#, TMCI4	TXD6, SMOSI6, SSDA6	
98		P80	MTIC5W, MTIC5W#, TMRI4	RXD6, SMISO6, SSCL6	
99		P11	MTIOC3A, MTIOC3A#, MTCLKC, MTCLKC#, TMO3		IRQ1
100		P10	MTIOC9B, MTIOC9B#, MTCLKD, MTCLKD#, TMRI3, POE12#	CTS6#, RTS6#, SS6#	IRQ0

Table 1.6 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version A) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, CAC)	Communications (SCI, RSPI, RIIC)	Others
55		P72	MTIOC4A		
56		P71	MTIOC3B		
57		P70	POE0#		IRQ5
58		P33	MTIOC3A, MTCLKA, TMO0	SSLA3	
59		P32	MTIOC3C, MTCLKB, TMO6	SSLA2	
60	VCC				
61		P31	MTIOC0A, MTCLKC, TMRI6	SSLA1	IRQ6
62	VSS				
63		P30	MTIOC0B, MTCLKD, TMCI6	SSLA0	IRQ7, COMP3
64		P24	MTIC5U, TMCI2, TMO6	RSPCKA	COMP0
65		P23	MTIC5V, TMO2, CACREF	MOSIA	COMP1
66		P22	MTIC5W, TMRI2, TMO4	MISOA	ADTRG2#, COMP2
67		P21	MTCLKA, MTIOC9A, TMCI4		IRQ6, ADTRG1#, AN116, CVREFC1
68		P20	MTCLKB, MTIOC9C, TMRI4		IRQ7, ADTRG0#, AN016, CVREFC0
69		P65			AN205
70		P64			AN204
71	AVCC2				
72	VREF				
73	AVSS2				
74		P63			AN203, IRQ7
75		P62			AN202, IRQ6
76		P61			AN201, IRQ5
77		P60			AN200, IRQ4
78		P55			AN211, IRQ3
79		P54			AN210, IRQ2
80		P53			AN209, IRQ1
81		P52			AN208, IRQ0
82		P51			AN207
83		P50			AN206
84		P47			AN103
85		P46			AN102, CMPC12, CMPC13, CMPC30, CMPC31
86		P45			AN101, CMPC02, CMPC03, CMPC20, CMPC21
87		P44			AN100, CMPC10, CMPC11, CMPC32, CMPC33
88		P43			AN003
89		P42			AN002
90		P41			AN001
91		P40			AN000, CMPC00, CMPC01, CMPC22, CMPC23
92	AVCC1				
93	AVCC0				
94	AVSS0				
95	AVSS1				
96		P82	MTIC5U, TMO4	SCK6	
97		P81	MTIC5V, TMCI4	TXD6, SMOSI6, SSDA6	
98		P80	MTIC5W, TMRI4	RXD6, SMISO6, SSCL6	
99		P11	MTIOC3A, MTCLKC, TMO3		IRQ1
100		P10	MTIOC9B, MTCLKD, TMRI3, POE12#	CTS6#, RTS6#, SS6#	IRQ0

(9) Floating-point status word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

2.3 Accumulator

The accumulator (ACC0 or ACC1) is a 72-bit register used for DSP instructions. The accumulator is handled as a 96-bit register for reading and writing. At this time, when bits 95 to 72 of the accumulator are read, the value where the value of bit 71 is sign extended is read. Writing to bits 95 to 72 of the accumulator is ignored. ACC0 is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in ACC0 is modified by execution of the instruction.
Use the MVTACGU, MVTACHI, and MVTACLO instructions for writing to the accumulator. The MVTACGU, MVTACHI, and MVTACLO instructions write data to bits 95 to 64, the higher-order 32 bits (bits 63 to 32), and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions for reading data from the accumulator. The MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions read data from the guard bits (bits 95 to 64), higher-order 32 bits (bits 63 to 32), the middle 32 bits (bits 47 to 16), and the lower-order 32 bits (bits 31 to 0), respectively.

Table 4.1 List of I/O Registers (Address Order) (4/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 708Fh	ICU	Interrupt Request Register 143	IR143	8	8	2 ICLK
0008 7090h	ICU	Interrupt Request Register 144	IR144	8	8	2 ICLK
0008 7091h	ICU	Interrupt Request Register 145	IR145	8	8	2 ICLK
0008 7092h	ICU	Interrupt Request Register 146	IR146	8	8	2 ICLK
0008 7095h	ICU	Interrupt Request Register 149	IR149	8	8	2 ICLK
0008 7096h	ICU	Interrupt Request Register 150	IR150	8	8	2 ICLK
0008 7097h	ICU	Interrupt Request Register 151	IR151	8	8	2 ICLK
0008 7098h	ICU	Interrupt Request Register 152	IR152	8	8	2 ICLK
0008 7099h	ICU	Interrupt Request Register 153	IR153	8	8	2 ICLK
0008 709Fh	ICU	Interrupt Request Register 159	IR159	8	8	2 ICLK
0008 70A0h	ICU	Interrupt Request Register 160	IR160	8	8	2 ICLK
0008 70A1h	ICU	Interrupt Request Register 161	IR161	8	8	2 ICLK
0008 70A2h	ICU	Interrupt Request Register 162	IR162	8	8	2 ICLK
0008 70A3h	ICU	Interrupt Request Register 163	IR163	8	8	2 ICLK
0008 70A4h	ICU	Interrupt Request Register 164	IR164	8	8	2 ICLK
0008 70A5h	ICU	Interrupt Request Register 165	IR165	8	8	2 ICLK
0008 70A8h	ICU	Interrupt Request Register 168	IR168	8	8	2 ICLK
0008 70A9h	ICU	Interrupt Request Register 169	IR169	8	8	2 ICLK
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8	2 ICLK
0008 70ACh	ICU	Interrupt Request Register 172	IR172	8	8	2 ICLK
0008 70ADh	ICU	Interrupt Request Register 173	IR173	8	8	2 ICLK
0008 70AEh	ICU	Interrupt Request Register 174	IR174	8	8	2 ICLK
0008 70AFh	ICU	Interrupt Request Register 175	IR175	8	8	2 ICLK
0008 70B0h	ICU	Interrupt Request Register 176	IR176	8	8	2 ICLK
0008 70B1h	ICU	Interrupt Request Register 177	IR177	8	8	2 ICLK
0008 70B2h	ICU	Interrupt Request Register 178	IR178	8	8	2 ICLK
0008 70B3h	ICU	Interrupt Request Register 179	IR179	8	8	2 ICLK
0008 70B4h	ICU	Interrupt Request Register 180	IR180	8	8	2 ICLK
0008 70B5h	ICU	Interrupt Request Register 181	IR181	8	8	2 ICLK
0008 70B6h	ICU	Interrupt Request Register 182	IR182	8	8	2 ICLK
0008 70B7h	ICU	Interrupt Request Register 183	IR183	8	8	2 ICLK
0008 70B8h	ICU	Interrupt Request Register 184	IR184	8	8	2 ICLK
0008 70B9h	ICU	Interrupt Request Register 185	IR185	8	8	2 ICLK
0008 70BAh	ICU	Interrupt Request Register 186	IR186	8	8	2 ICLK
0008 70BBh	ICU	Interrupt Request Register 187	IR187	8	8	2 ICLK
0008 70BCh	ICU	Interrupt Request Register 188	IR188	8	8	2 ICLK
0008 70BDh	ICU	Interrupt Request Register 189	IR189	8	8	2 ICLK
0008 70BEh	ICU	Interrupt Request Register 190	IR190	8	8	2 ICLK
0008 70BFh	ICU	Interrupt Request Register 191	IR191	8	8	2 ICLK
0008 70C0h	ICU	Interrupt Request Register 192	IR192	8	8	2 ICLK
0008 70C1h	ICU	Interrupt Request Register 193	IR193	8	8	2 ICLK
0008 70C2h	ICU	Interrupt Request Register 194	IR194	8	8	2 ICLK
0008 70C3h	ICU	Interrupt Request Register 195	IR195	8	8	2 ICLK
0008 70C4h	ICU	Interrupt Request Register 196	IR196	8	8	2 ICLK
0008 70C5h	ICU	Interrupt Request Register 197	IR197	8	8	2 ICLK
0008 70CAh	ICU	Interrupt Request Register 202*2	IR202	8	8	2 ICLK
0008 70CBh	ICU	Interrupt Request Register 203*2	IR203	8	8	2 ICLK
0008 70CCh	ICU	Interrupt Request Register 204*2	IR204	8	8	2 ICLK
0008 70CDh	ICU	Interrupt Request Register 205*2	IR205	8	8	2 ICLK
0008 70CEh	ICU	Interrupt Request Register 206*2	IR206	8	8	2 ICLK
0008 70CFh	ICU	Interrupt Request Register 207*2	IR207	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (5/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 70D0h	ICU	Interrupt Request Register 208*2	IR208	8	8	2 ICLK
0008 70D1h	ICU	Interrupt Request Register 209*2	IR209	8	8	2 ICLK
0008 70D2h	ICU	Interrupt Request Register 210*2	IR210	8	8	2 ICLK
0008 70D3h	ICU	Interrupt Request Register 211*2	IR211	8	8	2 ICLK
0008 70D4h	ICU	Interrupt Request Register 212*2	IR212	8	8	2 ICLK
0008 70D5h	ICU	Interrupt Request Register 213*2	IR213	8	8	2 ICLK
0008 70D6h	ICU	Interrupt Request Register 214*2	IR214	8	8	2 ICLK
0008 70D7h	ICU	Interrupt Request Register 215*2	IR215	8	8	2 ICLK
0008 70D8h	ICU	Interrupt Request Register 216*2	IR216	8	8	2 ICLK
0008 70D9h	ICU	Interrupt Request Register 217*2	IR217	8	8	2 ICLK
0008 70DAh	ICU	Interrupt Request Register 218	IR218	8	8	2 ICLK
0008 70DBh	ICU	Interrupt Request Register 219	IR219	8	8	2 ICLK
0008 70DCh	ICU	Interrupt Request Register 220	IR220	8	8	2 ICLK
0008 70DDh	ICU	Interrupt Request Register 221	IR221	8	8	2 ICLK
0008 70DEh	ICU	Interrupt Request Register 222	IR222	8	8	2 ICLK
0008 70DFh	ICU	Interrupt Request Register 223	IR223	8	8	2 ICLK
0008 70E0h	ICU	Interrupt Request Register 224	IR224	8	8	2 ICLK
0008 70E1h	ICU	Interrupt Request Register 225	IR225	8	8	2 ICLK
0008 70E2h	ICU	Interrupt Request Register 226	IR226	8	8	2 ICLK
0008 70E3h	ICU	Interrupt Request Register 227	IR227	8	8	2 ICLK
0008 70E4h	ICU	Interrupt Request Register 228	IR228	8	8	2 ICLK
0008 70E5h	ICU	Interrupt Request Register 229	IR229	8	8	2 ICLK
0008 70EEh	ICU	Interrupt Request Register 238*2	IR238	8	8	2 ICLK
0008 70EFh	ICU	Interrupt Request Register 239*2	IR239	8	8	2 ICLK
0008 70F0h	ICU	Interrupt Request Register 240*2	IR240	8	8	2 ICLK
0008 70F1h	ICU	Interrupt Request Register 241*2	IR241	8	8	2 ICLK
0008 70F2h	ICU	Interrupt Request Register 242*2	IR242	8	8	2 ICLK
0008 70F3h	ICU	Interrupt Request Register 243*2	IR243	8	8	2 ICLK
0008 70F4h	ICU	Interrupt Request Register 244*2	IR244	8	8	2 ICLK
0008 70F6h	ICU	Interrupt Request Register 246	IR246	8	8	2 ICLK
0008 70F7h	ICU	Interrupt Request Register 247	IR247	8	8	2 ICLK
0008 70F8h	ICU	Interrupt Request Register 248	IR248	8	8	2 ICLK
0008 70F9h	ICU	Interrupt Request Register 249	IR249	8	8	2 ICLK
0008 711Bh	ICU	DTC Transfer Request Enable Register 027	DTCER027	8	8	2 ICLK
0008 711Ch	ICU	DTC Transfer Request Enable Register 028	DTCER028	8	8	2 ICLK
0008 711Dh	ICU	DTC Transfer Request Enable Register 029	DTCER029	8	8	2 ICLK
0008 711Eh	ICU	DTC Transfer Request Enable Register 030	DTCER030	8	8	2 ICLK
0008 711Fh	ICU	DTC Transfer Request Enable Register 031	DTCER031	8	8	2 ICLK
0008 712Dh	ICU	DTC Transfer Request Enable Register 045	DTCER045	8	8	2 ICLK
0008 712Eh	ICU	DTC Transfer Request Enable Register 046	DTCER046	8	8	2 ICLK
0008 7130h	ICU	DTC Transfer Request Enable Register 048*2	DTCER048	8	8	2 ICLK
0008 7131h	ICU	DTC Transfer Request Enable Register 049*2	DTCER049	8	8	2 ICLK
0008 7132h	ICU	DTC Transfer Request Enable Register 050*2	DTCER050	8	8	2 ICLK
0008 7133h	ICU	DTC Transfer Request Enable Register 051*2	DTCER051	8	8	2 ICLK
0008 7135h	ICU	DTC Transfer Request Enable Register 053*2	DTCER053	8	8	2 ICLK
0008 7136h	ICU	DTC Transfer Request Enable Register 054*2	DTCER054	8	8	2 ICLK
0008 7137h	ICU	DTC Transfer Request Enable Register 055*2	DTCER055	8	8	2 ICLK
0008 7138h	ICU	DTC Transfer Request Enable Register 056*2	DTCER056	8	8	2 ICLK
0008 713Bh	ICU	DTC Transfer Request Enable Register 059*2	DTCER059	8	8	2 ICLK
0008 7140h	ICU	DTC Transfer Request Enable Register 064	DTCER064	8	8	2 ICLK
0008 7141h	ICU	DTC Transfer Request Enable Register 065	DTCER065	8	8	2 ICLK
0008 7142h	ICU	DTC Transfer Request Enable Register 066	DTCER066	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (10/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 73BDh	ICU	Interrupt Source Priority Register 189	IPR189	8	8	2 ICLK
0008 73C0h	ICU	Interrupt Source Priority Register 192	IPR192	8	8	2 ICLK
0008 73C3h	ICU	Interrupt Source Priority Register 195	IPR195	8	8	2 ICLK
0008 73CAh	ICU	Interrupt Source Priority Register 202*2	IPR202	8	8	2 ICLK
0008 73CBh	ICU	Interrupt Source Priority Register 203*2	IPR203	8	8	2 ICLK
0008 73CCh	ICU	Interrupt Source Priority Register 204*2	IPR204	8	8	2 ICLK
0008 73CDh	ICU	Interrupt Source Priority Register 205*2	IPR205	8	8	2 ICLK
0008 73CEh	ICU	Interrupt Source Priority Register 206*2	IPR206	8	8	2 ICLK
0008 73CFh	ICU	Interrupt Source Priority Register 207*2	IPR207	8	8	2 ICLK
0008 73D0h	ICU	Interrupt Source Priority Register 208*2	IPR208	8	8	2 ICLK
0008 73D1h	ICU	Interrupt Source Priority Register 209*2	IPR209	8	8	2 ICLK
0008 73D2h	ICU	Interrupt Source Priority Register 210*2	IPR210	8	8	2 ICLK
0008 73D3h	ICU	Interrupt Source Priority Register 211*2	IPR211	8	8	2 ICLK
0008 73D4h	ICU	Interrupt Source Priority Register 212*2	IPR212	8	8	2 ICLK
0008 73D5h	ICU	Interrupt Source Priority Register 213*2	IPR213	8	8	2 ICLK
0008 73D6h	ICU	Interrupt Source Priority Register 214*2	IPR214	8	8	2 ICLK
0008 73D7h	ICU	Interrupt Source Priority Register 215*2	IPR215	8	8	2 ICLK
0008 73D8h	ICU	Interrupt Source Priority Register 216*2	IPR216	8	8	2 ICLK
0008 73D9h	ICU	Interrupt Source Priority Register 217*2	IPR217	8	8	2 ICLK
0008 73DAh	ICU	Interrupt Source Priority Register 218	IPR218	8	8	2 ICLK
0008 73DEh	ICU	Interrupt Source Priority Register 222	IPR222	8	8	2 ICLK
0008 73E2h	ICU	Interrupt Source Priority Register 226	IPR226	8	8	2 ICLK
0008 73EEh	ICU	Interrupt Source Priority Register 238*2	IPR238	8	8	2 ICLK
0008 73EFh	ICU	Interrupt Source Priority Register 239*2	IPR239	8	8	2 ICLK
0008 73F0h	ICU	Interrupt Source Priority Register 240*2	IPR240	8	8	2 ICLK
0008 73F1h	ICU	Interrupt Source Priority Register 241*2	IPR241	8	8	2 ICLK
0008 73F2h	ICU	Interrupt Source Priority Register 242*2	IPR242	8	8	2 ICLK
0008 73F3h	ICU	Interrupt Source Priority Register 243*2	IPR243	8	8	2 ICLK
0008 73F4h	ICU	Interrupt Source Priority Register 244*2	IPR244	8	8	2 ICLK
0008 73F6h	ICU	Interrupt Source Priority Register 246	IPR246	8	8	2 ICLK
0008 73F7h	ICU	Interrupt Source Priority Register 247	IPR247	8	8	2 ICLK
0008 73F8h	ICU	Interrupt Source Priority Register 248	IPR248	8	8	2 ICLK
0008 73F9h	ICU	Interrupt Source Priority Register 249	IPR249	8	8	2 ICLK
0008 7500h	ICU	IRQ Control Register 0	IRQCR0	8	8	2 ICLK
0008 7501h	ICU	IRQ Control Register 1	IRQCR1	8	8	2 ICLK
0008 7502h	ICU	IRQ Control Register 2	IRQCR2	8	8	2 ICLK
0008 7503h	ICU	IRQ Control Register 3	IRQCR3	8	8	2 ICLK
0008 7504h	ICU	IRQ Control Register 4	IRQCR4	8	8	2 ICLK
0008 7505h	ICU	IRQ Control Register 5	IRQCR5	8	8	2 ICLK
0008 7506h	ICU	IRQ Control Register 6	IRQCR6	8	8	2 ICLK
0008 7507h	ICU	IRQ Control Register 7	IRQCR7	8	8	2 ICLK
0008 7510h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK
0008 7514h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2 or 3 PCLKB
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB
0008 8004h	CMT0	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (19/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 C168h	MPC	P50 Pin Function Control Register	P50PFS	8	8	2 or 3 PCLKB
0008 C169h	MPC	P51 Pin Function Control Register	P51PFS	8	8	2 or 3 PCLKB
0008 C16Ah	MPC	P52 Pin Function Control Register	P52PFS	8	8	2 or 3 PCLKB
0008 C16Bh	MPC	P53 Pin Function Control Register	P53PFS	8	8	2 or 3 PCLKB
0008 C16Ch	MPC	P54 Pin Function Control Register	P54PFS	8	8	2 or 3 PCLKB
0008 C16Dh	MPC	P55 Pin Function Control Register	P55PFS	8	8	2 or 3 PCLKB
0008 C170h	MPC	P60 Pin Function Control Register	P60PFS	8	8	2 or 3 PCLKB
0008 C171h	MPC	P61 Pin Function Control Register	P61PFS	8	8	2 or 3 PCLKB
0008 C172h	MPC	P62 Pin Function Control Register	P62PFS	8	8	2 or 3 PCLKB
0008 C173h	MPC	P63 Pin Function Control Register	P63PFS	8	8	2 or 3 PCLKB
0008 C174h	MPC	P64 Pin Function Control Register	P64PFS	8	8	2 or 3 PCLKB
0008 C175h	MPC	P65 Pin Function Control Register	P65PFS	8	8	2 or 3 PCLKB
0008 C178h	MPC	P70 Pin Function Control Register	P70PFS	8	8	2 or 3 PCLKB
0008 C179h	MPC	P71 Pin Function Control Register	P71PFS	8	8	2 or 3 PCLKB
0008 C17Ah	MPC	P72 Pin Function Control Register	P72PFS	8	8	2 or 3 PCLKB
0008 C17Bh	MPC	P73 Pin Function Control Register	P73PFS	8	8	2 or 3 PCLKB
0008 C17Ch	MPC	P74 Pin Function Control Register	P74PFS	8	8	2 or 3 PCLKB
0008 C17Dh	MPC	P75 Pin Function Control Register	P75PFS	8	8	2 or 3 PCLKB
0008 C17Eh	MPC	P76 Pin Function Control Register	P76PFS	8	8	2 or 3 PCLKB
0008 C180h	MPC	P80 Pin Function Control Register	P80PFS	8	8	2 or 3 PCLKB
0008 C181h	MPC	P81 Pin Function Control Register	P81PFS	8	8	2 or 3 PCLKB
0008 C182h	MPC	P82 Pin Function Control Register	P82PFS	8	8	2 or 3 PCLKB
0008 C188h	MPC	P90 Pin Function Control Register	P90PFS	8	8	2 or 3 PCLKB
0008 C189h	MPC	P91 Pin Function Control Register	P91PFS	8	8	2 or 3 PCLKB
0008 C18Ah	MPC	P92 Pin Function Control Register	P92PFS	8	8	2 or 3 PCLKB
0008 C18Bh	MPC	P93 Pin Function Control Register	P93PFS	8	8	2 or 3 PCLKB
0008 C18Ch	MPC	P94 Pin Function Control Register	P94PFS	8	8	2 or 3 PCLKB
0008 C18Dh	MPC	P95 Pin Function Control Register	P95PFS	8	8	2 or 3 PCLKB
0008 C18Eh	MPC	P96 Pin Function Control Register	P96PFS	8	8	2 or 3 PCLKB
0008 C190h	MPC	PA0 Pin Function Control Register	PA0PFS	8	8	2 or 3 PCLKB
0008 C191h	MPC	PA1 Pin Function Control Register	PA1PFS	8	8	2 or 3 PCLKB
0008 C192h	MPC	PA2 Pin Function Control Register	PA2PFS	8	8	2 or 3 PCLKB
0008 C193h	MPC	PA3 Pin Function Control Register	PA3PFS	8	8	2 or 3 PCLKB
0008 C194h	MPC	PA4 Pin Function Control Register	PA4PFS	8	8	2 or 3 PCLKB
0008 C195h	MPC	PA5 Pin Function Control Register	PA5PFS	8	8	2 or 3 PCLKB
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2 or 3 PCLKB
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2 or 3 PCLKB
0008 C19Ah	MPC	PB2 Pin Function Control Register	PB2PFS	8	8	2 or 3 PCLKB
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2 or 3 PCLKB
0008 C19Ch	MPC	PB4 Pin Function Control Register	PB4PFS	8	8	2 or 3 PCLKB
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2 or 3 PCLKB
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2 or 3 PCLKB
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2 or 3 PCLKB
0008 C1A8h	MPC	PD0 Pin Function Control Register	PD0PFS	8	8	2 or 3 PCLKB
0008 C1A9h	MPC	PD1 Pin Function Control Register	PD1PFS	8	8	2 or 3 PCLKB
0008 C1AAh	MPC	PD2 Pin Function Control Register	PD2PFS	8	8	2 or 3 PCLKB
0008 C1ABh	MPC	PD3 Pin Function Control Register	PD3PFS	8	8	2 or 3 PCLKB
0008 C1ACh	MPC	PD4 Pin Function Control Register	PD4PFS	8	8	2 or 3 PCLKB
0008 C1ADh	MPC	PD5 Pin Function Control Register	PD5PFS	8	8	2 or 3 PCLKB
0008 C1AEh	MPC	PD6 Pin Function Control Register	PD6PFS	8	8	2 or 3 PCLKB
0008 C1AFh	MPC	PD7 Pin Function Control Register	PD7PFS	8	8	2 or 3 PCLKB
0008 C1B0h	MPC	PE0 Pin Function Control Register	PE0PFS	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (24/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
000A 83F8h	RSCAN	Receive Buffer Register 5CL*2	RMDF05	16	16	2 or 3 PCLKB
000A 83FAh	RSCAN	Receive Rule Entry Register 7BH*2	GAFLMH7	16	16	2 or 3 PCLKB
000A 83FAh	RSCAN	Receive Buffer Register 5CH*2	RMDF15	16	16	2 or 3 PCLKB
000A 83FCh	RSCAN	Receive Rule Entry Register 7CL*2	GAFLPL7	16	16	2 or 3 PCLKB
000A 83FCh	RSCAN	Receive Buffer Register 5DL*2	RMDF25	16	16	2 or 3 PCLKB
000A 83FEh	RSCAN	Receive Rule Entry Register 7CH*2	GAFLPH7	16	16	2 or 3 PCLKB
000A 83FEh	RSCAN	Receive Buffer Register 5DH*2	RMDF35	16	16	2 or 3 PCLKB
000A 8400h	RSCAN	Receive Rule Entry Register 8AL*2	GAFLIDL8	16	16	2 or 3 PCLKB
000A 8400h	RSCAN	Receive Buffer Register 6AL*2	RMIDL6	16	16	2 or 3 PCLKB
000A 8402h	RSCAN	Receive Rule Entry Register 8AH*2	GAFLIDH8	16	16	2 or 3 PCLKB
000A 8402h	RSCAN	Receive Buffer Register 6AH*2	RMIDH6	16	16	2 or 3 PCLKB
000A 8404h	RSCAN	Receive Rule Entry Register 8BL*2	GAFLML8	16	16	2 or 3 PCLKB
000A 8404h	RSCAN	Receive Buffer Register 6BL*2	RMTS6	16	16	2 or 3 PCLKB
000A 8406h	RSCAN	Receive Rule Entry Register 8BH*2	GAFLMH8	16	16	2 or 3 PCLKB
000A 8406h	RSCAN	Receive Buffer Register 6BH*2	RMPTR6	16	16	2 or 3 PCLKB
000A 8408h	RSCAN	Receive Rule Entry Register 8CL*2	GAFLPL8	16	16	2 or 3 PCLKB
000A 8408h	RSCAN	Receive Buffer Register 6CL*2	RMDF06	16	16	2 or 3 PCLKB
000A 840Ah	RSCAN	Receive Rule Entry Register 8CH*2	GAFLPH8	16	16	2 or 3 PCLKB
000A 840Ah	RSCAN	Receive Buffer Register 6CH*2	RMDF16	16	16	2 or 3 PCLKB
000A 840Ch	RSCAN	Receive Rule Entry Register 9AL*2	GAFLIDL9	16	16	2 or 3 PCLKB
000A 840Ch	RSCAN	Receive Buffer Register 6DL*2	RMDF26	16	16	2 or 3 PCLKB
000A 840Eh	RSCAN	Receive Rule Entry Register 9AH*2	GAFLIDH9	16	16	2 or 3 PCLKB
000A 840Eh	RSCAN	Receive Buffer Register 6DH*2	RMDF36	16	16	2 or 3 PCLKB
000A 8410h	RSCAN	Receive Rule Entry Register 9BL*2	GAFLML9	16	16	2 or 3 PCLKB
000A 8410h	RSCAN	Receive Buffer Register 7AL*2	RMIDL7	16	16	2 or 3 PCLKB
000A 8412h	RSCAN	Receive Rule Entry Register 9BH*2	GAFLMH9	16	16	2 or 3 PCLKB
000A 8412h	RSCAN	Receive Buffer Register 7AH*2	RMIDH7	16	16	2 or 3 PCLKB
000A 8414h	RSCAN	Receive Rule Entry Register 9CL*2	GAFLPL9	16	16	2 or 3 PCLKB
000A 8414h	RSCAN	Receive Buffer Register 7BL*2	RMTS7	16	16	2 or 3 PCLKB
000A 8416h	RSCAN	Receive Rule Entry Register 9CH*2	GAFLPH9	16	16	2 or 3 PCLKB
000A 8416h	RSCAN	Receive Buffer Register 7BH*2	RMPTR7	16	16	2 or 3 PCLKB
000A 8418h	RSCAN	Receive Rule Entry Register 10AL*2	GAFLIDL10	16	16	2 or 3 PCLKB
000A 8418h	RSCAN	Receive Buffer Register 7CL*2	RMDF07	16	16	2 or 3 PCLKB
000A 841Ah	RSCAN	Receive Rule Entry Register 10AH*2	GAFLIDH10	16	16	2 or 3 PCLKB
000A 841Ah	RSCAN	Receive Buffer Register 7CH*2	RMDF17	16	16	2 or 3 PCLKB
000A 841Ch	RSCAN	Receive Rule Entry Register 10BL*2	GAFLML10	16	16	2 or 3 PCLKB
000A 841Ch	RSCAN	Receive Buffer Register 7DL*2	RMDF27	16	16	2 or 3 PCLKB
000A 841Eh	RSCAN	Receive Rule Entry Register 10BH*2	GAFLMH10	16	16	2 or 3 PCLKB
000A 841Eh	RSCAN	Receive Buffer Register 7DH*2	RMDF37	16	16	2 or 3 PCLKB
000A 8420h	RSCAN	Receive Rule Entry Register 10CL*2	GAFLPL10	16	16	2 or 3 PCLKB
000A 8420h	RSCAN	Receive Buffer Register 8AL*2	RMIDL8	16	16	2 or 3 PCLKB
000A 8422h	RSCAN	Receive Rule Entry Register 10CH*2	GAFLPH10	16	16	2 or 3 PCLKB
000A 8422h	RSCAN	Receive Buffer Register 8AH*2	RMIDH8	16	16	2 or 3 PCLKB
000A 8424h	RSCAN	Receive Rule Entry Register 11AL*2	GAFLIDL11	16	16	2 or 3 PCLKB
000A 8424h	RSCAN	Receive Buffer Register 8BL*2	RMTS8	16	16	2 or 3 PCLKB
000A 8426h	RSCAN	Receive Rule Entry Register 11AH*2	GAFLIDH11	16	16	2 or 3 PCLKB
000A 8426h	RSCAN	Receive Buffer Register 8BH*2	RMPTR8	16	16	2 or 3 PCLKB
000A 8428h	RSCAN	Receive Rule Entry Register 11BL*2	GAFLML11	16	16	2 or 3 PCLKB
000A 8428h	RSCAN	Receive Buffer Register 8CL*2	RMDF08	16	16	2 or 3 PCLKB
000A 842Ah	RSCAN	Receive Rule Entry Register 11BH*2	GAFLMH11	16	16	2 or 3 PCLKB
000A 842Ah	RSCAN	Receive Buffer Register 8CH*2	RMDF18	16	16	2 or 3 PCLKB
000A 842Ch	RSCAN	Receive Rule Entry Register 11CL*2	GAFLPL11	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (28/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000A 8614h	RSCAN	RAM Test Register 74*2	RPGACC74	16	16	2 or 3 PCLKB
000A 8616h	RSCAN0	Transmit Buffer Register 1BH*2	TMPTR1	16	16	2 or 3 PCLKB
000A 8616h	RSCAN	RAM Test Register 75*2	RPGACC75	16	16	2 or 3 PCLKB
000A 8618h	RSCAN0	Transmit Buffer Register 1CL*2	TMDF01	16	16	2 or 3 PCLKB
000A 8618h	RSCAN	RAM Test Register 76*2	RPGACC76	16	16	2 or 3 PCLKB
000A 861Ah	RSCAN0	Transmit Buffer Register 1CH*2	TMDF11	16	16	2 or 3 PCLKB
000A 861Ah	RSCAN	RAM Test Register 77*2	RPGACC77	16	16	2 or 3 PCLKB
000A 861Ch	RSCAN0	Transmit Buffer Register 1DL*2	TMDF21	16	16	2 or 3 PCLKB
000A 861Ch	RSCAN	RAM Test Register 78*2	RPGACC78	16	16	2 or 3 PCLKB
000A 861Eh	RSCAN0	Transmit Buffer Register 1DH*2	TMDF31	16	16	2 or 3 PCLKB
000A 861Eh	RSCAN	RAM Test Register 79*2	RPGACC79	16	16	2 or 3 PCLKB
000A 8620h	RSCAN0	Transmit Buffer Register 2AL*2	TMIDL2	16	16	2 or 3 PCLKB
000A 8620h	RSCAN	RAM Test Register 80*2	RPGACC80	16	16	2 or 3 PCLKB
000A 8622h	RSCAN0	Transmit Buffer Register 2AH*2	TMIDH2	16	16	2 or 3 PCLKB
000A 8622h	RSCAN	RAM Test Register 81*2	RPGACC81	16	16	2 or 3 PCLKB
000A 8624h	RSCAN	RAM Test Register 82*2	RPGACC82	16	16	2 or 3 PCLKB
000A 8626h	RSCAN0	Transmit Buffer Register 2BH*2	TMPTR2	16	16	2 or 3 PCLKB
000A 8626h	RSCAN	RAM Test Register 83*2	RPGACC83	16	16	2 or 3 PCLKB
000A 8628h	RSCAN0	Transmit Buffer Register 2CL*2	TMDF02	16	16	2 or 3 PCLKB
000A 8628h	RSCAN	RAM Test Register 84*2	RPGACC84	16	16	2 or 3 PCLKB
000A 862Ah	RSCAN0	Transmit Buffer Register 2CH*2	TMDF12	16	16	2 or 3 PCLKB
000A 862Ah	RSCAN	RAM Test Register 85*2	RPGACC85	16	16	2 or 3 PCLKB
000A 862Ch	RSCAN0	Transmit Buffer Register 2DL*2	TMDF22	16	16	2 or 3 PCLKB
000A 862Ch	RSCAN	RAM Test Register 86*2	RPGACC86	16	16	2 or 3 PCLKB
000A 862Eh	RSCAN0	Transmit Buffer Register 2DH*2	TMDF32	16	16	2 or 3 PCLKB
000A 862Eh	RSCAN	RAM Test Register 87*2	RPGACC87	16	16	2 or 3 PCLKB
000A 8630h	RSCAN0	Transmit Buffer Register 3AL*2	TMIDL3	16	16	2 or 3 PCLKB
000A 8630h	RSCAN	RAM Test Register 88*2	RPGACC88	16	16	2 or 3 PCLKB
000A 8632h	RSCAN0	Transmit Buffer Register 3AH*2	TMIDH3	16	16	2 or 3 PCLKB
000A 8632h	RSCAN	RAM Test Register 89*2	RPGACC89	16	16	2 or 3 PCLKB
000A 8634h	RSCAN	RAM Test Register 90*2	RPGACC90	16	16	2 or 3 PCLKB
000A 8636h	RSCAN0	Transmit Buffer Register 3BH*2	TMPTR3	16	16	2 or 3 PCLKB
000A 8636h	RSCAN	RAM Test Register 91*2	RPGACC91	16	16	2 or 3 PCLKB
000A 8638h	RSCAN0	Transmit Buffer Register 3CL*2	TMDF03	16	16	2 or 3 PCLKB
000A 8638h	RSCAN	RAM Test Register 92*2	RPGACC92	16	16	2 or 3 PCLKB
000A 863Ah	RSCAN0	Transmit Buffer Register 3CH*2	TMDF13	16	16	2 or 3 PCLKB
000A 863Ah	RSCAN	RAM Test Register 93*2	RPGACC93	16	16	2 or 3 PCLKB
000A 863Ch	RSCAN0	Transmit Buffer Register 3DL*2	TMDF23	16	16	2 or 3 PCLKB
000A 863Ch	RSCAN	RAM Test Register 94*2	RPGACC94	16	16	2 or 3 PCLKB
000A 863Eh	RSCAN0	Transmit Buffer Register 3DH*2	TMDF33	16	16	2 or 3 PCLKB
000A 863Eh	RSCAN	RAM Test Register 95*2	RPGACC95	16	16	2 or 3 PCLKB
000A 8640h to 000A 867Eh	RSCAN	RAM Test Register 96 to 127*2	RPGACC96 to 127	16	16	2 or 3 PCLKB
000A 8680h	RSCAN0	Transmit History Buffer Access Register*2	THLACC0	16	16	2 or 3 PCLKB
000C 1200h	MTU3	Timer Control Register	TCR	8	8, 16, 32	4 or 5 PCLKA
000C 1201h	MTU4	Timer Control Register	TCR	8	8	4 or 5 PCLKA
000C 1202h	MTU3	Timer Mode Register 1	TMDR1	8	8, 16	4 or 5 PCLKA
000C 1203h	MTU4	Timer Mode Register 1	TMDR1	8	8	4 or 5 PCLKA
000C 1204h	MTU3	Timer I/O Control Register H	TIORH	8	8, 16, 32	4 or 5 PCLKA
000C 1205h	MTU3	Timer I/O Control Register L	TIORL	8	8	4 or 5 PCLKA
000C 1206h	MTU4	Timer I/O Control Register H	TIORH	8	8, 16	4 or 5 PCLKA
000C 1207h	MTU4	Timer I/O Control Register L	TIORL	8	8	4 or 5 PCLKA

5.2 DC Characteristics

Table 5.3 DC Characteristics (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)	V_{IH}	VCC × 0.7	—	5.8	V	
	Ports B1, B2 (5 V tolerant)		VCC × 0.8	—	5.8		
	Ports 00 to 02, ports 10, 11, ports 20 to 24, ports 30 to 33, 36, 37, ports 70 to 76, ports 80 to 82, ports 90 to 96, ports A0 to A5, port B0, ports B3 to B7, ports D0 to D7, ports E0 to E5, RES#		VCC × 0.8	—	VCC + 0.3		
	Ports 40 to 47, ports 50 to 55, ports 60 to 65		VREF × 0.8	—	VREF + 0.3		
	RIIC input pin (except for SMBus)	V_{IL}	–0.3	—	VCC × 0.3		
	Ports 40 to 47, ports 50 to 55, ports 60 to 65		–0.3	—	VREF × 0.2		
	Other than RIIC input pin, Other than ports 40 to 47, 50 to 55, or 60 to 65		–0.3	—	VCC × 0.2		
	RIIC input pin (except for SMBus)	ΔV_T	VCC × 0.05	—	—		
	Ports 40 to 47, ports 50 to 55, ports 60 to 65		VREF × 0.1	—	—		
	Other than RIIC input pin, Other than ports 40 to 47, 50 to 55, or 60 to 65		VCC × 0.1	—	—		
Input level voltage (except for Schmitt trigger input pins)	MD	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL (external clock input)		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (SMBus)		2.1	—	VCC + 0.3		VCC ≤ 5.2 V
	MD	V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL (external clock input)		–0.3	—	VCC × 0.2		
	RIIC input pin (SMBus)		–0.3	—	0.8		VCC ≤ 5.2 V

Table 5.6 DC Characteristics (4)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item			Symbol	Chip Version A		Chip Version B		Unit	Test Conditions
				Typ.*3	Max.	Typ.*3	Max.		
Supply current*1	Software standby mode*2	T_a = 25°C	I_{CC}	1.0	55.0	1.5	15.0	µA	
		T_a = 55°C		1.5	60.0	3.0	38.0		
		T_a = 85°C		5.5	260.0	13.0	135.0		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 5 V.

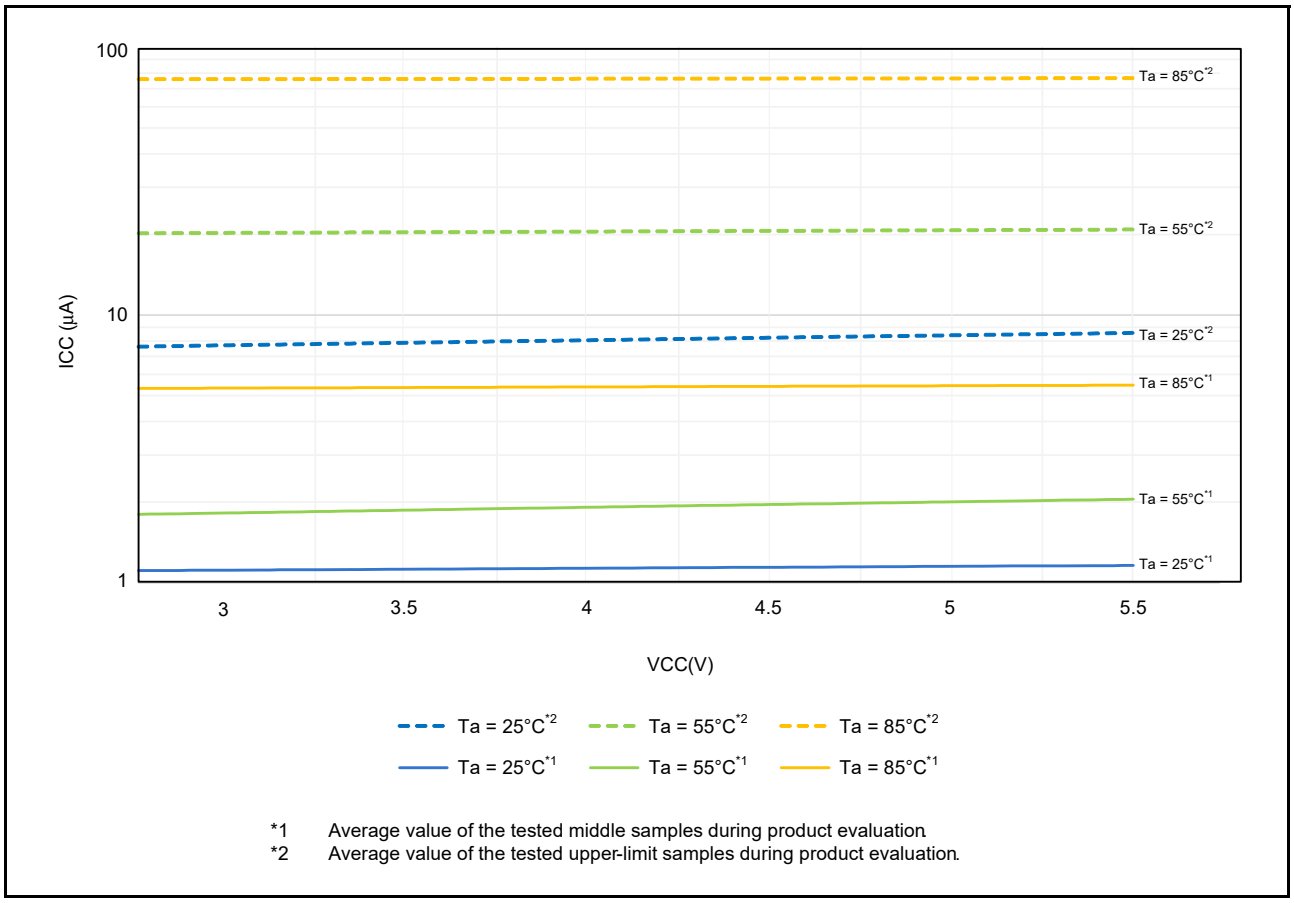


Figure 5.1 Voltage Dependency in Software Standby Mode (Chip Version A) (Reference Data)

Table 5.10 DC Characteristics (8)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

The ripple voltage must meet the allowable ripple frequency $f_{r\,(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (2.7 V). When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_{r\,(VCC)}$	—	—	10	kHz	Figure 5.5 $V_{r\,(VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 5.5 $V_{r\,(VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 5.5 $V_{r\,(VCC)} \leq VCC \times 0.06$
Allowable voltage change rising/falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

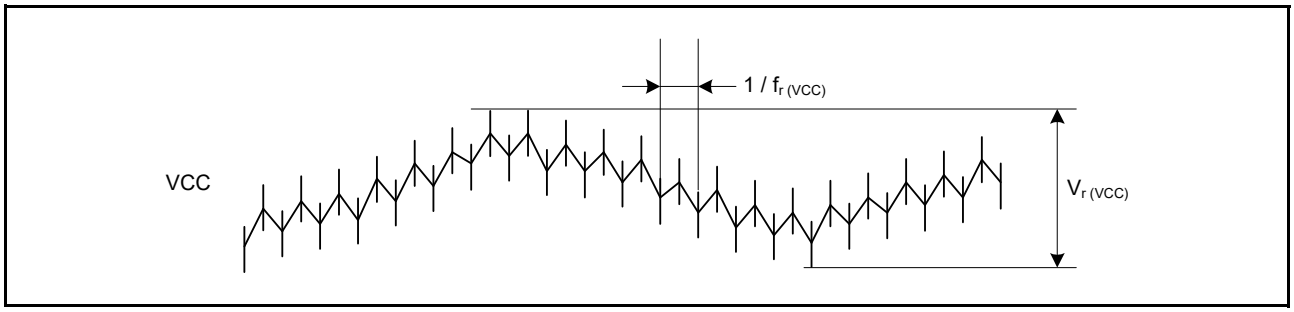


Figure 5.5 Ripple Waveform

Table 5.11 DC Characteristics (9)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Permissible error of VCL pin external capacitance	C_{VCL}	3.3	4.7	6.1	µF	

Note: The recommended capacitance is 4.7 µF. Variations in connected capacitors should be within the above range.

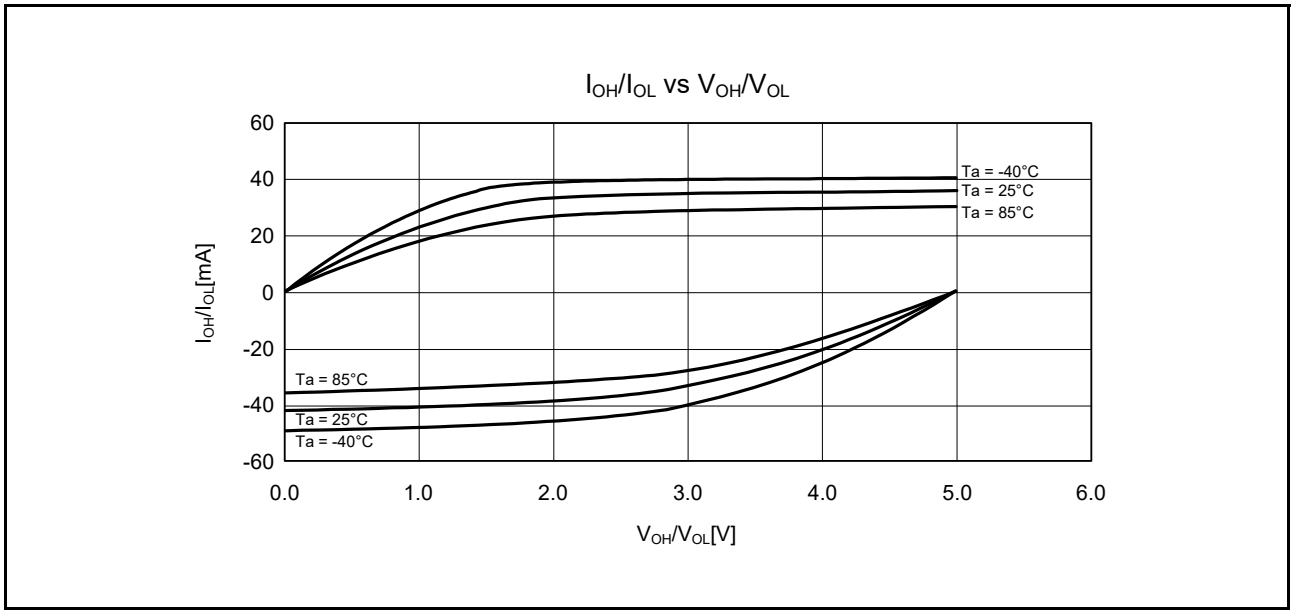


Figure 5.8 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.0 V when Normal Output is Selected (Reference Data)**

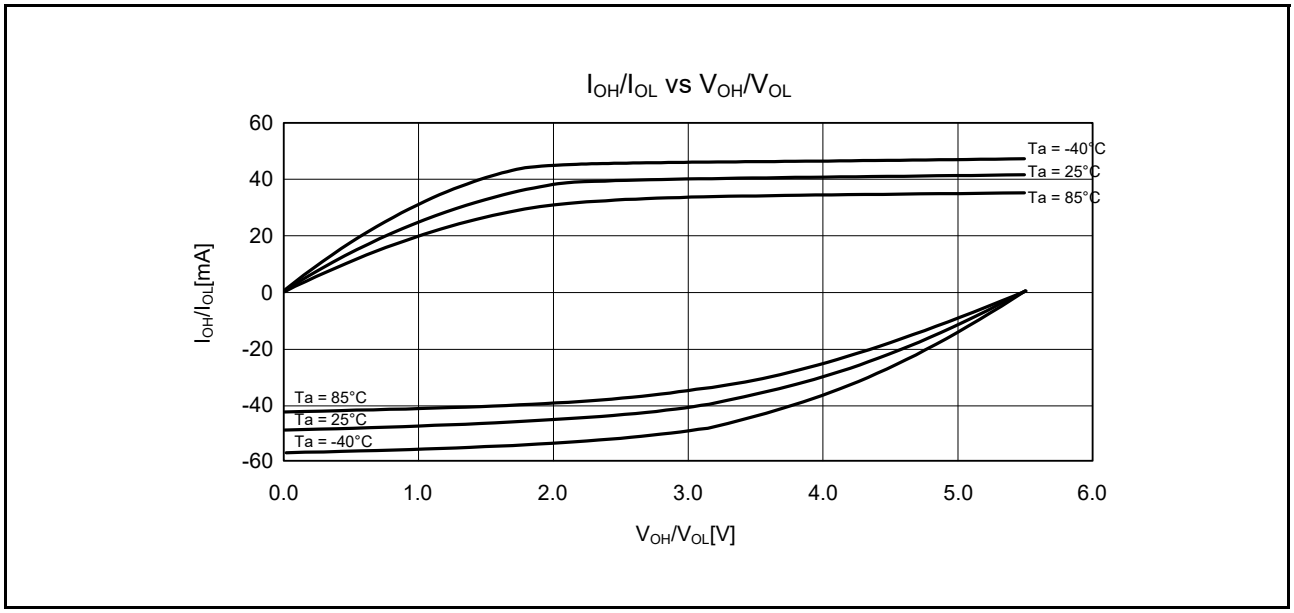


Figure 5.9 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.5 V when Normal Output is Selected (Reference Data)**

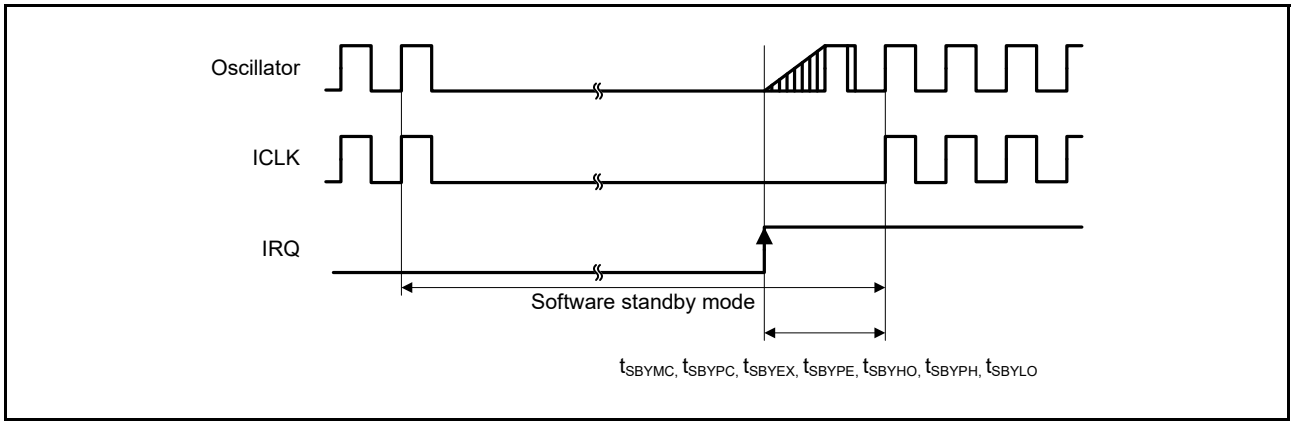


Figure 5.32 Software Standby Mode Recovery Timing

Table 5.20 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	t_{DSLP}	—	2	3.5	µs	Figure 5.33
	Middle-speed mode*3	t_{DSLP}	—	3	4	µs	

Note 1. Oscillators continue oscillating in deep sleep mode.
Note 2. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are 32 MHz.
Note 3. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are 12 MHz.

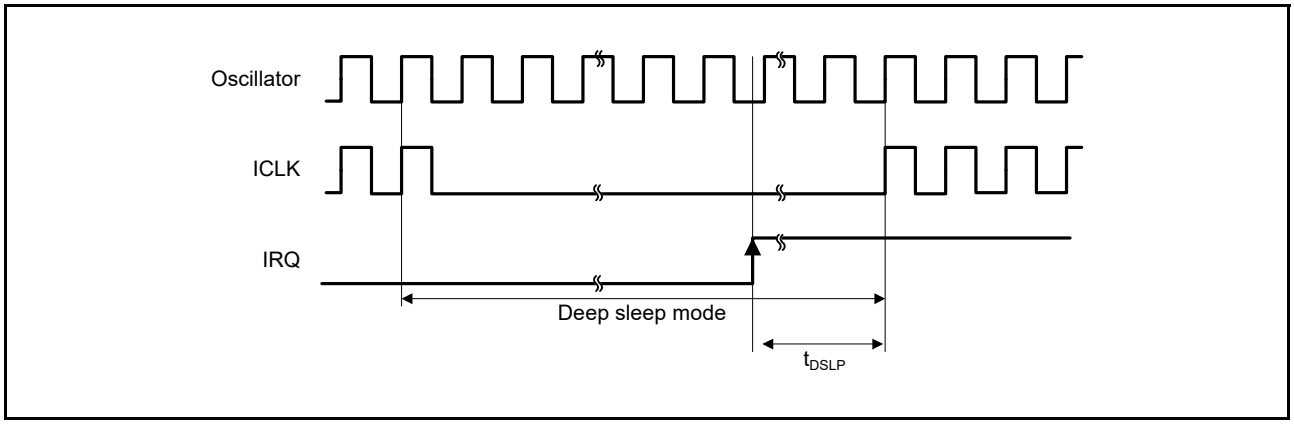


Figure 5.33 Deep Sleep Mode Recovery Timing

Table 5.21 Operating Mode Transition Time

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Mode before Transition	Mode after Transition	ICLK Frequency	Transition Time			Unit
			Min.	Typ.	Max.	
High-speed operating mode	Middle-speed operating modes	8 MHz	—	10	—	µs
Middle-speed operating modes	High-speed operating mode	8 MHz	—	37.5	—	µs

Note: Values when the frequencies of PCLKA, PCLKB, PCLKD, and FCLK are not divided.

5.3.4 Control Signal Timing

Table 5.22 Control Signal Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled (NMIFLTE.NFLTEN = 0)	$t_{Pcyc} \times 2 \le 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled (NMIFLTE.NFLTEN = 1)	$t_{NMICK} \times 3 \le 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled (IRQFLTE0.FLTENi = 0)	$t_{Pcyc} \times 2 \le 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled (IRQFLTE0.FLTENi = 1)	$t_{IRQCK} \times 3 \le 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in software standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

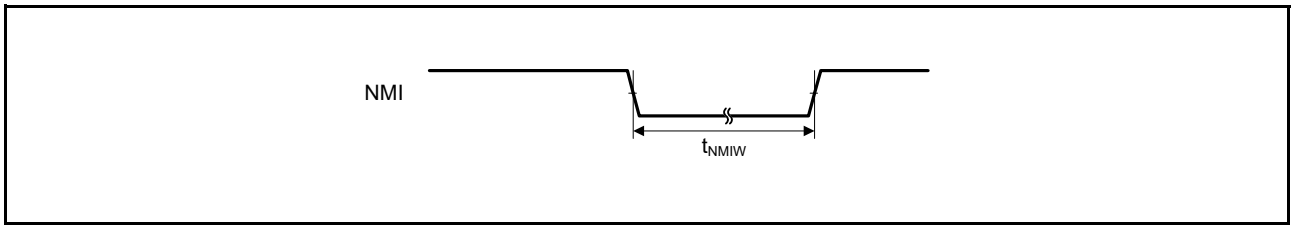


Figure 5.34 NMI Interrupt Input Timing

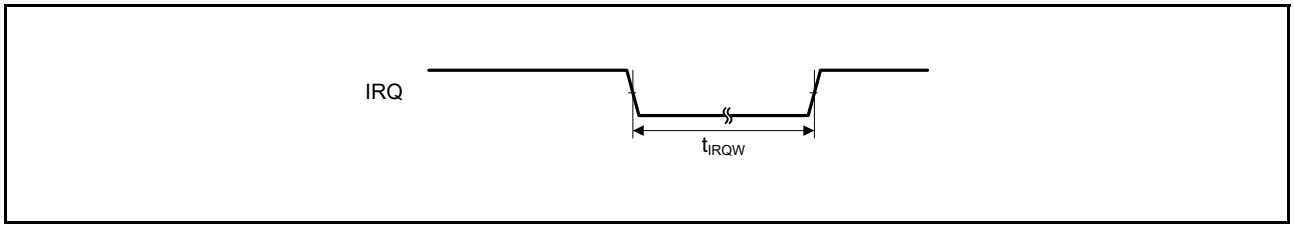


Figure 5.35 IRQ Interrupt Input Timing

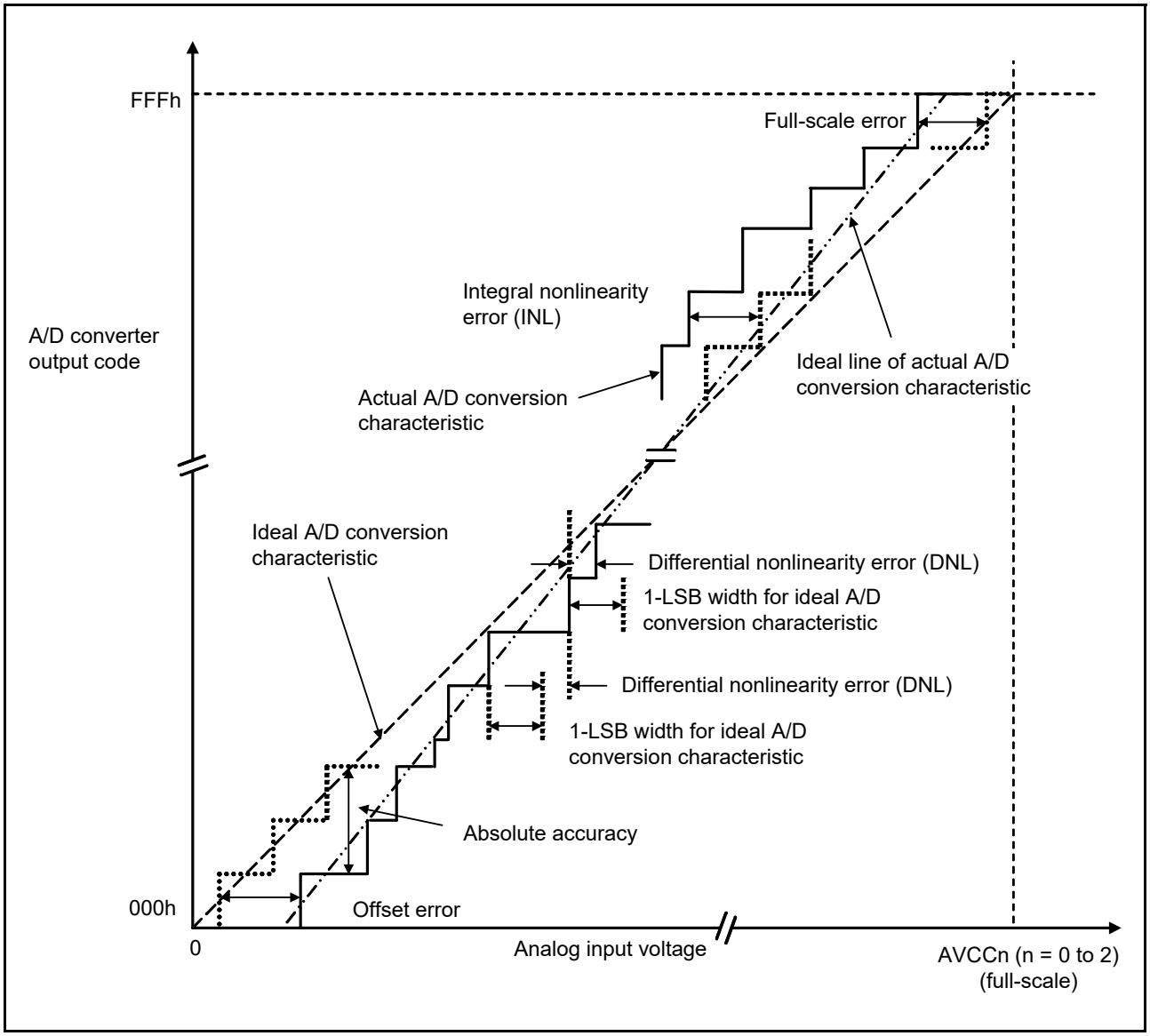


Figure 5.53 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

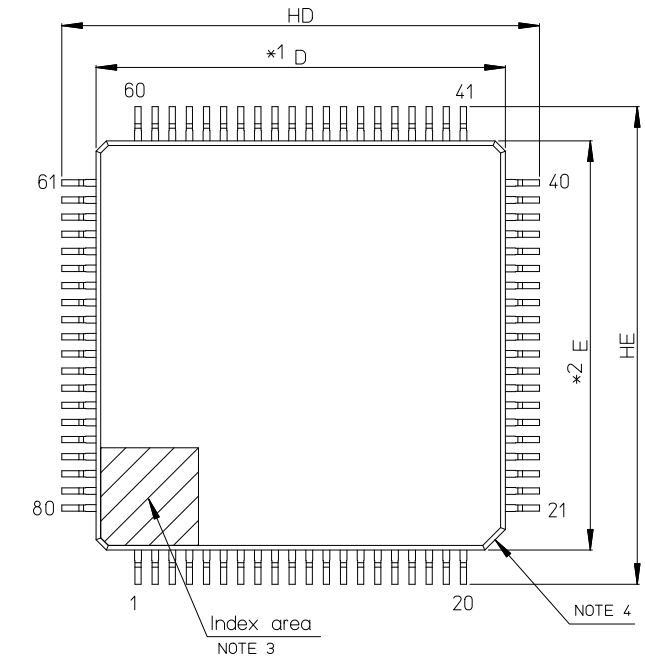
Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (AVCCn (n = 0 to 2)) is 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

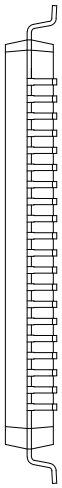
If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

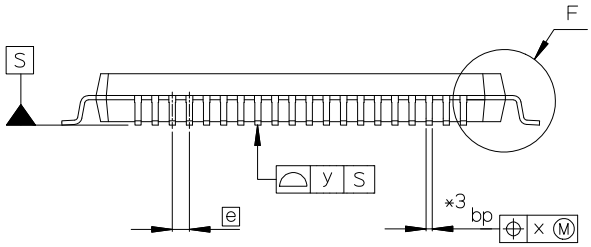
Integral nonlinearity error (INL)

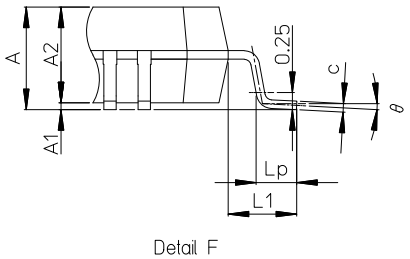
Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP80-12x12-0.50	PLQP0080KB-B	——	0.5g









Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A2	——	1.4	——
HD	13.8	14.0	14.2
HE	13.8	14.0	14.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.15	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

Figure C 80-Pin LFQFP (PLQP0080KB-B)

REVISION HISTORY	RX24T Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Nov 30, 2015	—	First edition, issued	
2.00	Apr 14, 2017	All	Chip version B, added The name of the previous product, changed to chip version A according to the above The specification of the HOCO, added The 64-pin package, added The specification of the voltage detection 0 level select bit, changed	TN-RX*-A171A/E
		5. Electrical Characteristics		
		—	The characteristics of HOCO-/GPT-/RSCAN-related and chip version B, added	
		72	Table 5.3 DC Characteristics (1): ports 36 and 37, added	
		78	Table 5.8 DC Characteristics (6), changed	
		100	Table 5.25 Timing of On-Chip Peripheral Modules (3), changed	TN-RX*-A170A/E
		115	Table 5.34 Characteristics of D/A Conversion (Chip Version A), changed	TN-RX*-A170A/E
		125	Figure 5.63 Connecting Capacitors (64 Pins), added	
		Appendix 1. Package Dimensions		
		126	Figure A 100-Pin LFQFP (PLQP0100KB-B), package part number, changed	
		128	Figure C 80-Pin LFQFP (PLQP0080KB-B), package part number, changed	
		129	Figure D 64-Pin LFQFP (PLQP0064KB-C), added	